



Article

# A High-Voltage-Isolated MEMS Quad–Solenoid Transformer with Specific Insulation Barriers for Miniaturized Galvanically Isolated Power Applications

Changnan Chen <sup>1,2</sup> , Pichao Pan <sup>1,2</sup>, Jiebin Gu <sup>1</sup> and Xinxin Li <sup>1,2,\*</sup>

<sup>1</sup> State Key Laboratory of Transducer Technology, Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, Shanghai 200050, China; ccn@mail.sim.ac.cn (C.C.); panpichao@mail.sim.ac.cn (P.P.); j.gu@mail.sim.ac.cn (J.G.)

<sup>2</sup> University of Chinese Academy of Sciences, Beijing 100049, China

\* Correspondence: xxli@mail.sim.ac.cn; Tel.: +86-21-6213-1794

**Abstract:** The paper reports on high voltage (HV)-isolated MEMS quad–solenoid transformers for compact isolated gate drivers and bias power supplies. The component is wafer-level fabricated via a novel MEMS micro-casting technique, where the tightly coupled quad–solenoid chip consists of monolithically integrated 3D inductive coils and an inserted ferrite magnetic core for high-efficiency isolated power transmission through electromagnetic coupling. The proposed HV-isolated transformer demonstrates a high inductance value of 743.2 nH, along with a small DC resistance of only 0.39 Ω in a compact footprint of 6 mm<sup>2</sup>, making it achieve a very high inductance integration density (123.9 nH/mm<sup>2</sup>) and the ratio of  $L/R$  (1906 nH/Ω). More importantly, with embedded ultra-thick serpentine-shaped (S-shaped) SiO<sub>2</sub> isolation barriers that completely separate the primary and secondary windings, an over 2 kV breakdown voltage is obtained. In addition, the HV-isolated transformer chips exhibit a superior power transfer efficiency of over 80% and ultra-high dual-phase saturation current of 1.4 A, thereby covering most practical cases in isolated, integrated bias power supplies such as high-efficiency high-voltage-isolated gate driver solutions.



**Citation:** Chen, C.; Pan, P.; Gu, J.; Li, X. A High-Voltage-Isolated MEMS Quad–Solenoid Transformer with Specific Insulation Barriers for Miniaturized Galvanically Isolated Power Applications. *Micromachines* **2024**, *15*, 228. <https://doi.org/10.3390/mi15020228>

Academic Editor: Aiqun Liu

Received: 10 January 2024

Revised: 29 January 2024

Accepted: 30 January 2024

Published: 31 January 2024



**Copyright:** © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (<https://creativecommons.org/licenses/by/4.0/>).

## 1. Introduction

With the newly emerging dense-power, high voltage-level applications such as electric vehicles (EVs) [1], fast-charging uninterruptible power supplies (UPSs) [2], and renewable energy microgrids [3,4] rapidly evolving, the energy density, high-power handling capability, and robustness of the highly miniaturized power converters utilized in these applications have become more critical. Recent advancements in wide-bandgap (WBG) semiconductor material-based devices, including gallium nitride (GaN) high electron-mobility transistors and silicon carbide (SiC) metal–oxide–semiconductor field-effect transistors (MOSFETs) which show superior electric and thermal characteristics [5], have largely helped eliminate the bottleneck of power modules by dramatically maximizing the converter efficiency and power density at the higher switching frequencies and operating voltages [6]. However, in WBG switching device-based power converter applications, electric components in the low-voltage domain are susceptible to voltage surges, ground drift, and leakage current introduced from power MOSFETs in the high-voltage domain, which can potentially cause a breakdown of integrated control circuits [7,8]. Therefore, as the interface between the low-voltage controller and the high-voltage power stage, the integrated micro-transformers that power the gate drivers through embedded galvanic isolation barriers [9] to control the energy flow in WBG switching devices are required to protect against large potential differences, which can be as high as 800 V [10]. Moreover,

safety regulations for electronics and human-operated equipment always require galvanic isolations [11], since high-voltage electric contact accidents can trigger electric shock and potentially cause fatal ventricular fibrillation.

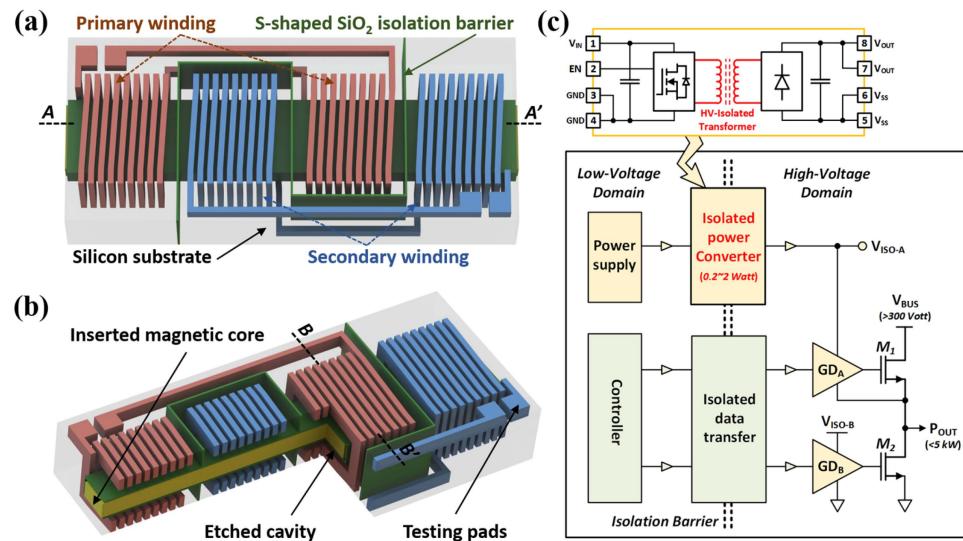
Traditionally, optocouplers and enameled wire-wound discrete transformers have been adopted for isolated data transfer [12] and isolated power conversion [13], respectively, in order to provide full isolation. However, these discrete devices, which are bulky and unable to be integrated on-chip, are failing to meet the emerging demands for the miniaturization and integration of dense-power systems. With the rapid development of advanced electronic packaging and MEMS microfabrication technology, on-chip integrated micro-transformers with minimal footprint for compact galvanically isolated gate driver applications are highly desired. Unfortunately, integrating transformers monolithically and achieving high-voltage isolation above 2 kV while maintaining high-power transfer efficiency is still challenging due to the thickness of insulating materials and the structurally constrained coupling coefficient. For example, monolithic air-core transformers with planar interleaved coupling coils, which are simple to micromachine, have been implemented for isolated power transfer in [14–16] but are restricted with lower isolation voltage ratings of only 20 V, 200 V, and 380 V, respectively. The limitations are attributed to the incomplete galvanic isolation between the coupling coils and the substrate, as well as the thinness and low dielectric strength of the dielectric layer used as an isolation barrier. In addition, the relatively limited inductance integration density (e.g., 8.0 nH/mm<sup>2</sup> [17]) that the monolithic air-core transformers can offer restricts the periodic magnetic energy storage, and thus leads to a higher operating frequency of above 100 MHz, thereby degrading the system efficiency through substantial switching and rectification losses. Efforts have been made to increase the inductance value of micro-transformers by wrapping high-permeability magnetic materials outside the racetrack-shaped coupling coils [18,19] or by electroplating thin-film magnetic cores inside solenoidal coils [20,21], both of which multiply the fabrication complexity. Additionally, subsequent high-temperature processes pose inherent degradation in the permeability of these pre-deposited magnetic cores, which are already limited in thickness (e.g., only 3 μm thick in [22] and 6 μm thick in [20]), resulting in inadequate magnetic flux enhancement and, thus, limited inductance increments, and making them unfavorable for further improvements in efficiency and integration.

Therefore, aiming to significantly enhance the galvanic isolation capability and inductance integration density of monolithically integrated micro-transformers in a targeted operating frequency of a few megahertz, in this paper, one kind of novel structure design of three-dimensional quad-solenoid coupling coils with serpentine-shaped (S-shaped) ultra-thick SiO<sub>2</sub> isolation barriers and unique fabrication processes for high-voltage-isolated silicon-integrated micro-transformers are proposed.

## 2. Design and Modeling

### 2.1. Structural Design of the High-Voltage-Isolated Transformer Device

The detailed structure design and the isolated power transfer functionalities of the proposed high-voltage-isolated MEMS quad-solenoid transformer for compact galvanically isolated gate driver applications are schematically shown in Figure 1. Two sets of primary and secondary coupling coils are embedded inside the high-resistance silicon substrate in the form of a comb-like interleaved arrangement. Specifically, the primary and secondary windings are composed of series-connected dual solenoids, respectively, so together, they form a tightly coupled quad-solenoid structure to enable high-efficiency isolated power transmission at the targeted operating frequency of around 3 MHz through electromagnetic coupling. In addition, as indicated in Figure 1a, ultra-thick S-shaped SiO<sub>2</sub> isolation barriers with high dielectric strength completely separate the primary and secondary windings from the high-resistance silicon substrate on which they are embedded, thus ensuring high-voltage isolation.



**Figure 1.** (a) Schematic three-dimensional illustrations of the proposed quad-solenoid HV-isolated transformer chip and its (b) cross-sectional view, demonstrating the inserted ferrite magnetic core. (c) Simplified electrical architecture of fully isolated gate driver solutions with integrated isolated data and power transfer.

As for the metallization of three-dimensional solenoidal coupling coils, traditionally, the use of multiple photolithography and micro-electroplating is the only way to form such complex multilayer metal structures with through-silicon vias (TSVs) connecting the upper and lower metal grooves, inevitably introducing high contact resistance between the metal layers. As an alternative to the time-consuming micro-electroplating process, the molten alloy MEMS micro-casting technique [23] was first developed by our group, aiming to enable advanced IC packaging with dense vertical electric interconnections [24]. Herein, this novel Zn-Al alloy micro-casting process is further optimized to facilitate the rapid metallization of a three-dimensional high-density solenoidal structure within the pre-etched silicon-mold wafers. Benefiting from the micro-casted thick-metal structures with high aspect ratios, the silicon-embedded solenoidal windings take advantage of the high coil density and ultra-low DC resistance, which further increases the quality factor (*Q*-factor). The MEMS micromachining process for the formation of silicon-mold wafers and the scheme of the subsequent micro-casting process are detailed in Section 3. Additionally, as shown in Figure 1b, the coupling solenoidal windings in the HV-isolated transformer take full advantage of the effective magnetic flux enhancement introduced by the inserted high-permeability 200 micron-thick ferrite magnetic core to significantly increase the inductance values and largely eliminate leakage inductance. Therefore, a high inductance integration density and coupling coefficient are ensured. In addition, the unclosed magnetic core configuration allows for a high saturation current of the HV-isolated transformer.

## 2.2. Device Modeling

The inductance of the coupling solenoidal coils in the designed HV-isolated transformer chips with an inserted ferrite magnetic core can be analytically quantified from the combination of air core inductance,  $L_{air}$ , and the inductance increment introduced from the magnetic core,  $\Delta L$ , based on the following equations [25]:

$$L_{mag} = L_{air} + \Delta L \quad (1)$$

where the air core inductance,  $L_{air}$ , can be further obtained based on the equation in [26] as

$$L_{air} = \frac{\mu_0 \mu_r \text{air} N^2 S}{l} \quad (2)$$

where  $\mu_{r\_air}$  is the relative permeability of air,  $l$  represents the axial length of the solenoidal coils, and  $S$  is the inner cross-sectional area of the solenoidal coils. The total number of turns of the coupling primary or secondary windings in the 1:1 transformer is written as  $N$ . Since the inductive windings are composed of series-connected dual solenoids, the above equation can be rewritten as

$$L_{air} = \frac{\mu_0 \mu_{r\_air} N_1^2 S}{l_1} + \frac{\mu_0 \mu_{r\_air} N_2^2 S}{l_2} \quad (3)$$

The numbers of turns of individual windings in the series-connected dual solenoids are  $N_1$  and  $N_2$ , respectively; and the axial lengths are  $l_1$  and  $l_2$ , respectively. In addition, the magnetic core-introduced inductance increment,  $\Delta L$ , can be approximated by [25]

$$\Delta L = \frac{\mu_0 \mu_{rc} N^2 w_{mag} t_{mag}}{l_{mag} [1 + N_d(\mu_{rc} - 1)]} = \frac{\mu_0 \mu_{eff} N^2 w_{mag} t_{mag}}{l_{mag}}, \quad \mu_{eff} = \frac{\mu_{rc}}{[1 + N_d(\mu_{rc} - 1)]} \quad (4)$$

where  $\mu_{rc}$  is the relative permeability of the inserted magnetic core; and  $w_{mag}$ ,  $t_{mag}$ , and  $l_{mag}$  are the core's width, thickness, and length, respectively. Since the demagnetizing field inside the finite-sized magnetic core will effectively reduce the core's relative permeability, the demagnetizing factor  $N_d$ , proposed by D.-X. Chen in [27], with its numerical solutions available in [28], is adopted to characterize the effective permeability,  $\mu_{eff}$ , more accurately. Considering the series-connected inductive winding structure, Equation (4) can then be expressed as

$$\Delta L = \frac{\mu_0 \mu_{eff} (N_1^2 + N_2^2) w_{mag} t_{mag}}{l_{mag}}. \quad (5)$$

Magnetic power loss is introduced by inserting a magnetic core inside the coils, which increases the total resistance,  $R$ , of the inductive windings in the HV-isolated transformer chips. Based on the classical theory of electromagnetism, the energy stored inside the core,  $E_{mag}$ , and that of the magnetic power loss,  $P_{mag}$ , are related to the real and imaginary parts of the permeability of the magnetic material used, respectively [29].

$$E_{mag} = \frac{1}{2} \iiint \mu' |H|^2 dV \quad (6)$$

$$P_{mag} = \iiint \omega \mu'' |H|^2 dV. \quad (7)$$

According to Lee's assumption [30], if the real and imaginary parts of permeability are uniform inside the magnetic core, then  $P_{mag}$  can be estimated as

$$P_{mag} \approx 2\omega \left( \frac{\mu''}{\mu'} \right) E_{mag}, \quad E_{mag} = \frac{1}{2} \Delta L \cdot I^2. \quad (8)$$

Based on Joule's law,  $P_{mag}$  can also be expressed as Equation (9), in which  $R_{mag}$  represents the resistance contributed by magnetic power loss:

$$P_{mag} = R_{mag} I^2. \quad (9)$$

Therefore, the total resistance,  $R$ , of the inductive windings in the HV-isolated transformer chip, which consists of  $R_{mag}$  and air-core wingding resistance,  $R_w$ , is given as

$$R = R_w + R_{mag} = R_w + \omega \left( \frac{\mu''}{\mu'} \right) \Delta L. \quad (10)$$

Based on the above equations, the inductance value  $L_{air}$ ,  $L_{mag}$ , and total resistance ( $R$ ) of the inductive windings are calculated as 105.9 nH, 770.6 nH, and 1.15 Ω, respectively, at a lower frequency of 3 MHz, for the designed device, with its geometry parameters listed in

Table 1. In addition, when the operating frequency is well below its self-resonant frequency, the Q-factor can be expressed as  $Q = \omega L_{mag}/R$  [31] and is subsequently calculated as 12.6@3MHz.

**Table 1.** Summary of design parameters for HV-isolated quad–solenoid transformer chips.

Parameters	Primary Winding	Secondary Winding
Number of turns ( $N_1 + N_2$ )	18 (9 + 9)	18 (9 + 9)
Metal width	60 $\mu m$	60 $\mu m$
Metal depth	100 $\mu m$	100 $\mu m$
Gap between adjacent turns	40 $\mu m$	40 $\mu m$
Coil inner height	520 $\mu m$	520 $\mu m$
Coil inner width	900 $\mu m$	900 $\mu m$
Parameters	Inserted thin-film ferrite magnetic core	
Max relative permeability (at 3 MHz)	185 (real part, $\mu'$ ); 13 (imaginary part, $\mu''$ )	
Length of the magnetic core	5100 $\mu m$	
Width of the magnetic core	700 $\mu m$	
Thickness of the magnetic core	200 $\mu m$	

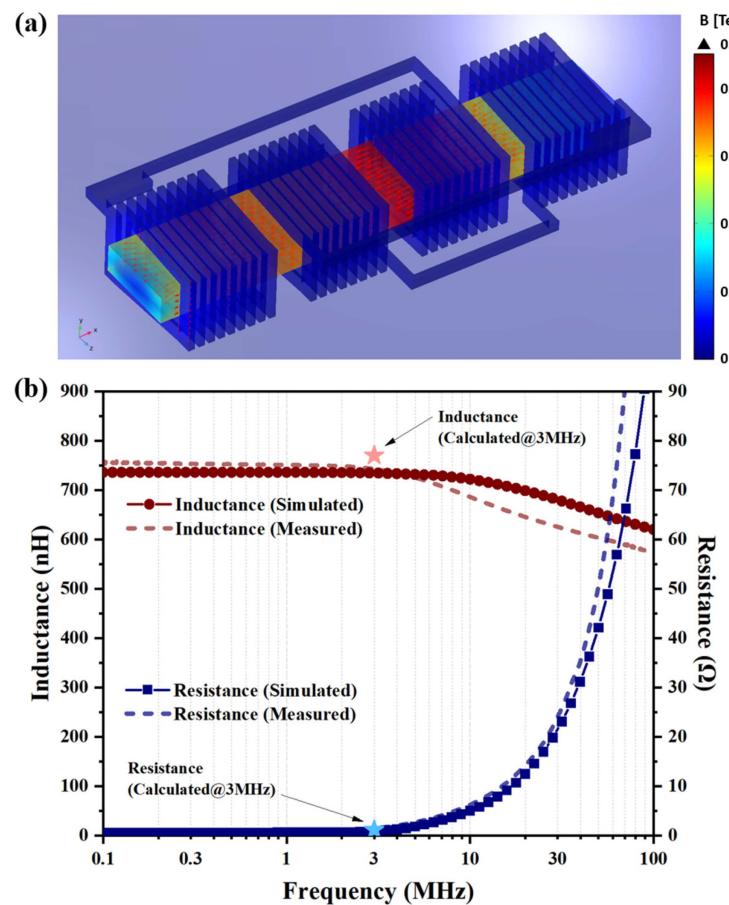
To fully validate the device design and the above analytical calculations, finite element simulations were conducted by using COMSOL Multiphysics 5.5 software with the magnetic field module in the frequency domain. First, the structure of the HV-isolated transformer was modeled as a two-port network and driven by a 3 MHz excitation current, with an amplitude of 1 A through the one lumped port which connects the primary windings.

As shown in Figure 2a, when primary winding is excited, an intense magnetic field occurs inside the embedded magnetic core, with a maximum magnetic flux density of around 0.225 T, which is well below the saturation magnetic flux density of ferrite magnetic material, implying a higher current loading capability. Then, by applying excitations through two lumped ports sequentially, the two-port impedance matrix, which contains the inductance value and resistance of the transformer, is simulated over frequency. As plotted in Figure 2b, the finite element simulated inductance ( $L$ ) and resistance ( $R$ ) are consistent with the calculations from the design model, and they both show satisfactory agreement with the subsequent measured results in a wide frequency range, from 100 kHz to 100 MHz.

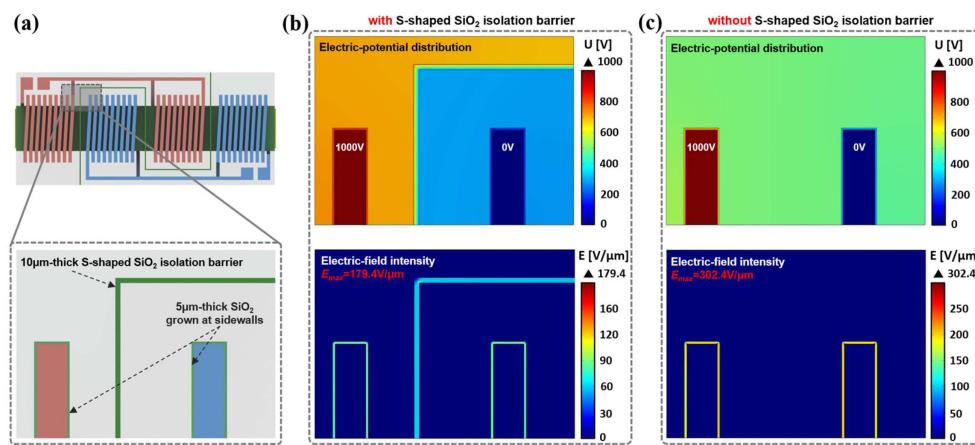
The theoretical dielectric strength of typical insulator materials is compared in Table 2. SiO<sub>2</sub> is preferred, as it provides an enormous dielectric strength of around 500 V/ $\mu m$  and superior mechanical stability. Shown in Figure 3a are the partially enlarged schematics demonstrating the designed structure of hybrid dielectric layers consisting of 10  $\mu m$  thick S-shaped SiO<sub>2</sub> isolation barriers and a 5  $\mu m$  thick insulating layer grown at the silicon sidewalls.

**Table 2.** Comparison of the dielectric strength of different types of insulator materials.

	Epoxy	Polyimide	BCB	LPCVD TEOS SiO <sub>2</sub>	Thermal SiO <sub>2</sub>
Dielectric strength	11.7 V/ $\mu m$ [32]	300 V/ $\mu m$ [33]	320 V/ $\mu m$ [34]	500 V/ $\mu m$ [35]	500 V/ $\mu m$ [36]



**Figure 2.** (a) Magnetic flux density colormap of the designed HV-isolated transformer chip under a 3 MHz excitation current, with an amplitude of 1 A loading on the primary windings. (b) Comparisons of inductance ( $L$ ) and resistance ( $R$ ) between calculations, finite element simulations, and subsequent measured results.



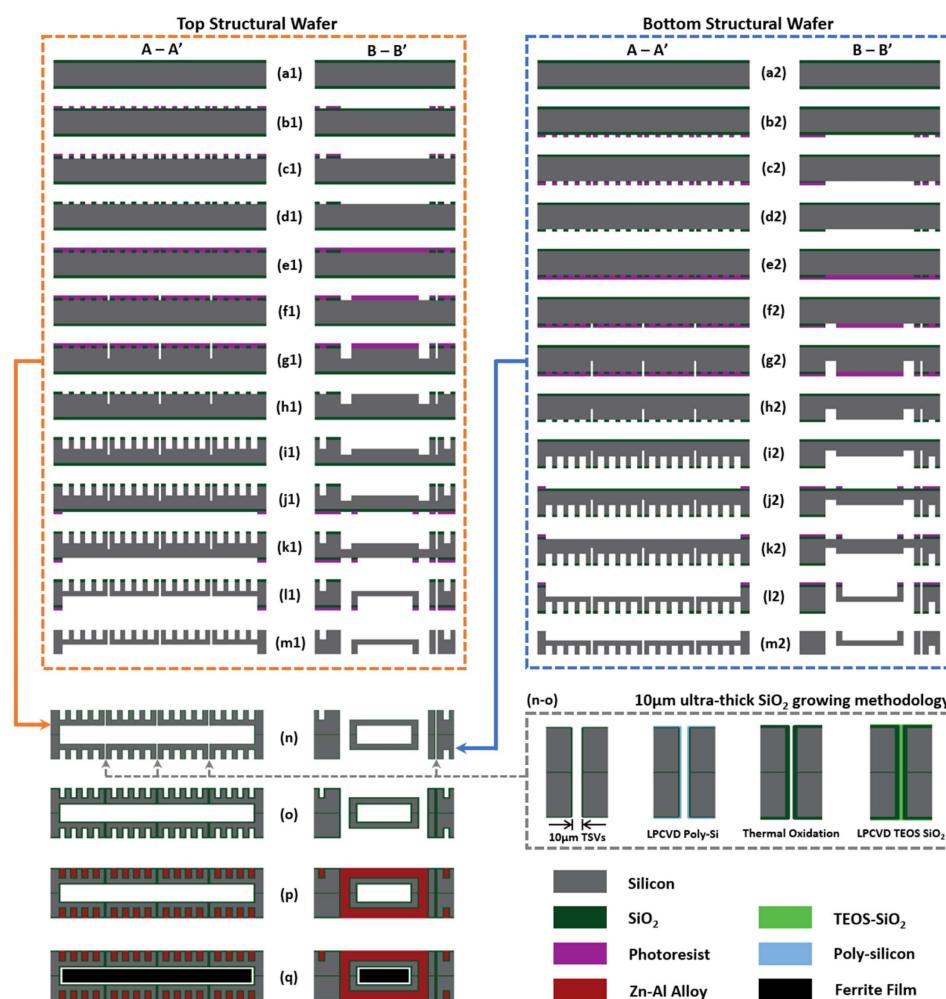
**Figure 3.** (a) Partially enlarged schematics demonstrating the  $\text{SiO}_2$  isolation barrier and the insulating layer grown at the sidewalls. (b) Finite element simulations of electric-potential distribution and electric-field intensity in HV-isolated transformer with embedded S-shaped isolation barrier and (c) the one without S-shaped isolation barrier under the application of 1000 V bias voltage.

The maximum electric-field intensity was then simulated to evaluate the theoretical breakdown voltage for the HV-isolated transformer under the bias voltage loading conditions. As shown in Figure 3b, when a 1000 V bias voltage is loaded on one side of an

HV-isolated transformer with an integrated S-shaped isolation barrier, a well-controlled maximum electric-field intensity of  $179.4 \text{ V}/\mu\text{m}$  in the dielectric layer is found. As a comparison, under the same bias voltage loading condition, when the S-shaped isolation barrier is removed (as shown in Figure 3c), an increased maximum electric-field intensity of  $302.4 \text{ V}/\mu\text{m}$  is observed. Accordingly, based on the theoretical dielectric strength of  $\text{SiO}_2$ , an ultra-high breakdown voltage of 2787.1 V is estimated for the HV-isolated transformer with the embedded S-shaped isolation barrier, which is about 70% higher than the 1653.4 V breakdown voltage for the transformer without an S-shaped isolation barrier.

### 3. Fabrication

According to Figure 4 (the cutting planes A-A' and B-B' are indicated in Figure 1a,b), the fabrication process flow for the HV-isolated transformer chips contains two main stages, involving the structural wafers MEMS micromachining processes and the subsequent wafer-level MEMS micro-casting process for the metallization of three-dimensional high-density solenoidal structure within the aligned and bonded silicon structural wafers. Detailed fabrication steps are outlined as follows:



**Figure 4.** Fabrication processes flow for the HV-isolated transformers. (a1–m1) Top structural wafer and (a2–m2) bottom structural wafer formation by multiple photolithography and deep-RIE. (n–o) Silicon bonding and 10  $\mu\text{m}$  thick  $\text{SiO}_2$  growing and filling inside the TSVs. (p) Molten alloy injecting via MEMS micro-casting process and (q) ferrite magnetic core inserting.

(a1–d1) For the preparation of the top structural wafer, a 1  $\mu\text{m}$  thick  $\text{SiO}_2$  hard mask is first thermally grown on a 360  $\mu\text{m}$  thick, 4-inch high-resistance ( $10,000 \Omega\cdot\text{cm}$ ) silicon wafer and then patterned by using a front-side photolithography and  $\text{SiO}_2$  dry-etching process.

(e1–f1) The composite mask that defines the etching windows for both the S-shaped through-silicon vias measuring 10  $\mu\text{m}$  in width and the vertical interconnection vias is formed after overlay photolithography on the patterned  $\text{SiO}_2$  layer.

(g1) The defined S-shaped vias, as well as the vertical interconnection vias, are then partially etched utilizing the deep reactive ion etching (deep-RIE) process.

(h1–i1) After the removal of the photoresist, deep-RIE is processed again to form the front-side horizontal grooves of the solenoidal cavities. Meanwhile, the S-shaped vias and the vertical interconnection vias are etched simultaneously.

(j1–k1) A double-side aligned photolithography and  $\text{SiO}_2$  dry-etching process is performed to pattern the backside of the  $\text{SiO}_2$  hard mask.

(l1–m1) With both patterned photoresist and  $\text{SiO}_2$  as etching masks, the cavity for magnetic core insertion is formed, and the vertical vias are etched through during the final deep-RIE process on the top structural wafer. After that, the photoresist and the  $\text{SiO}_2$  hard mask are removed.

(a2–m2) The bottom structural wafer is micromachined through the similar MEMS processes.

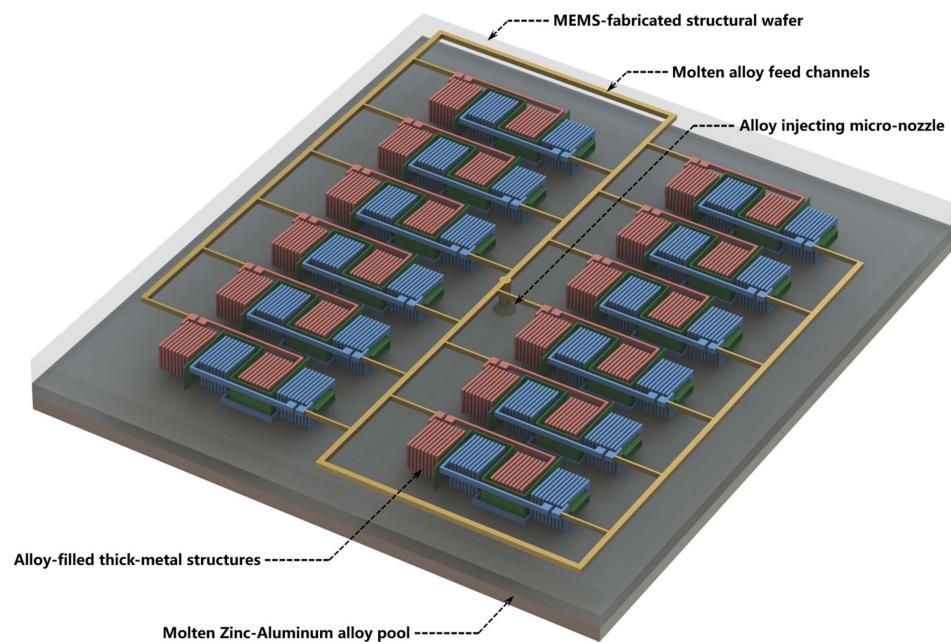
(n) After the etching for both the top and bottom structural wafers, 2  $\mu\text{m}$  thick  $\text{SiO}_2$  layers are uniformly grown on the surface, as well as on the silicon sidewalls, of the structural wafers. Then, silicon-to-silicon direct hydrophilic bonding is carried out for the two aligned structural wafers and subsequently annealed in an oxygen atmosphere.

(o) Using the low-pressure chemical vapor deposition (LPCVD) process, 2  $\mu\text{m}$  thick Poly-Si is uniformly deposited on both the surface and the sidewalls, followed by the application of a thermal oxidation process to fully convert the deposited Poly-Si into a thick  $\text{SiO}_2$  layer. Subsequently, 1  $\mu\text{m}$  thick tetraethyl orthosilicate (TEOS) LPCVD  $\text{SiO}_2$  is deposited to finish filling the S-shaped vias.

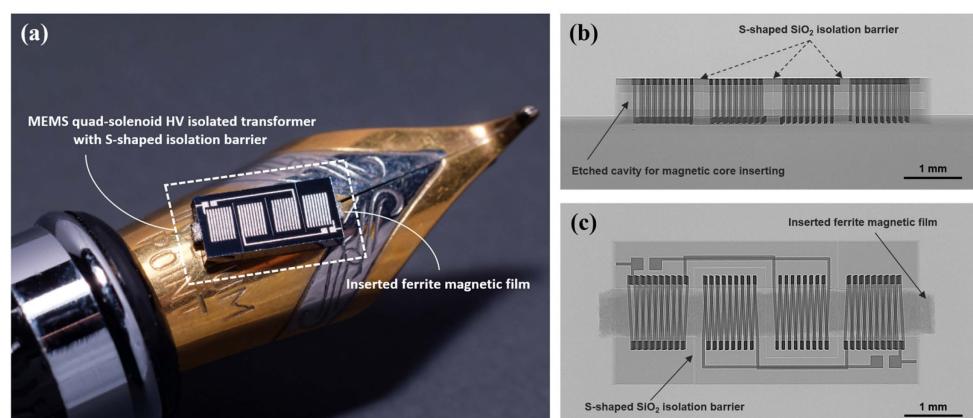
(p) During the MEMS micro-casting process, micro-nozzles from above the liquid alloy pool are aligned with the inlet vias in the casting micro-mold. The molten Zn-Al alloy is then injected under exerting pressure through the micro-nozzles and guided by the alloy feed channels (see Figure 5) into the solenoidal cavities. As the exerting pressure slowly decreases under a specific rate to reach the rupture pressure of the liquid molten alloy bridge which is connecting the casting mold with the alloy pool, the alloy-filled thick-metal structures will then be pinched off from the micro-nozzles and then solidified inside the structural wafers under natural cooling.

The fabricated quad-solenoid HV-isolated transformer chip is shown in Figure 6. Figure 6a is the macro-photograph of the transformer chip, which is saw-diced from a 4-inch wafer. The silicon-embedded solenoidal coupling coils occupy a tiny footprint of 6  $\text{mm}^2$ . Metal pads placed on each side of the chip are formed simultaneously during the micro-casting process, and they are designed for probe testing and the subsequent wire bonding.

Figure 6b is the X-ray perspective micrograph front view of the fabricated HV-isolated transformer chip, where a pre-etched cavity for magnetic core insertion centered in the silicon substrate can be clearly seen. From the X-ray perspective top view, which is shown in Figure 6c, a 200  $\mu\text{m}$  thick ferrite magnetic core with a width of 700  $\mu\text{m}$  and a length of 5100  $\mu\text{m}$  is inserted into the pre-etched cavity. The S-shaped  $\text{SiO}_2$  isolation barriers completely separate the primary and secondary windings from the high-resistance silicon substrate.



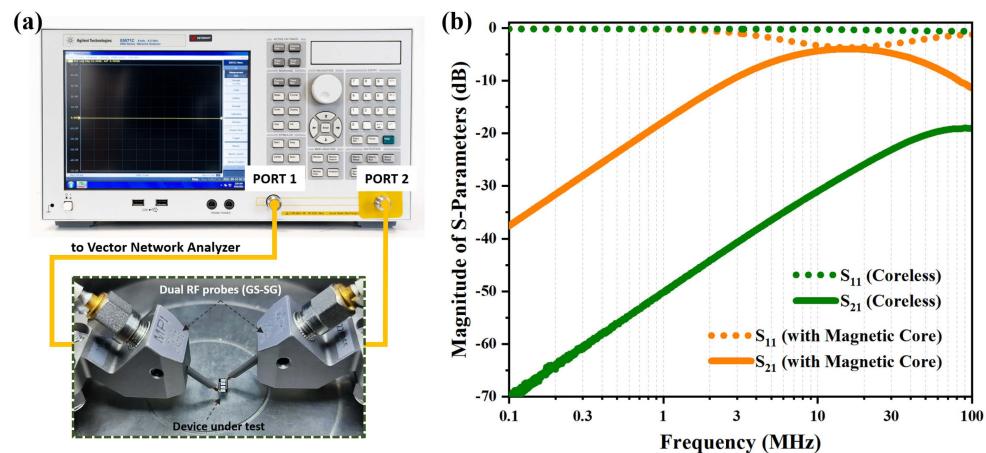
**Figure 5.** Partially enlarged schematics demonstrating the wafer-level batch formation for the three-dimensional thick-metal structures embedded inside the MEMS-fabricated 4-inch structural wafers during the developed Zn-Al molten alloy MEMS micro-casting process.



**Figure 6.** (a) Close-up view of the fabricated quad-solenoid HV-isolated transformer chip placed on a pen tip. (b) X-ray perspective micrograph showing the front view of the transformer chip. (c) X-ray perspective micrograph top view of the transformer chip with inserted magnetic core.

#### 4. Testing Results

In order to further characterize the electromagnetic performance of the fabricated quad-solenoid HV-isolated transformer, including inductance integration density, coupling coefficient, and power transfer efficiency, two-port scattering parameters (*S*-parameters) of the chips were first measured and extracted. The measurement setup is shown in Figure 7a; the testing pads from primary and secondary windings are connected to the vector network analyzer through dual RF probes and coaxial cables. Prior to the measurement, standard SOLT calibrations, which include the short, open, load, and through calibration, are applied to effectively eliminate the effects of parasitic parameters. As plotted in Figure 7b, the extracted two-port *S*-parameters of the HV-isolated transformers with inserted ferrite magnetic core and the one without magnetic core were collected together.



**Figure 7.** (a) Illustrations of the two-port scattering parameters ( $S$ -parameters) measurement setup for the fabricated HV-isolated transformers using a vector network analyzer (VNA) with a pair of RF probes. (b) The extracted two-port  $S$ -parameters of the HV-isolated transformers with an inserted ferrite magnetic core (orange line) and the one without a magnetic core (green line).

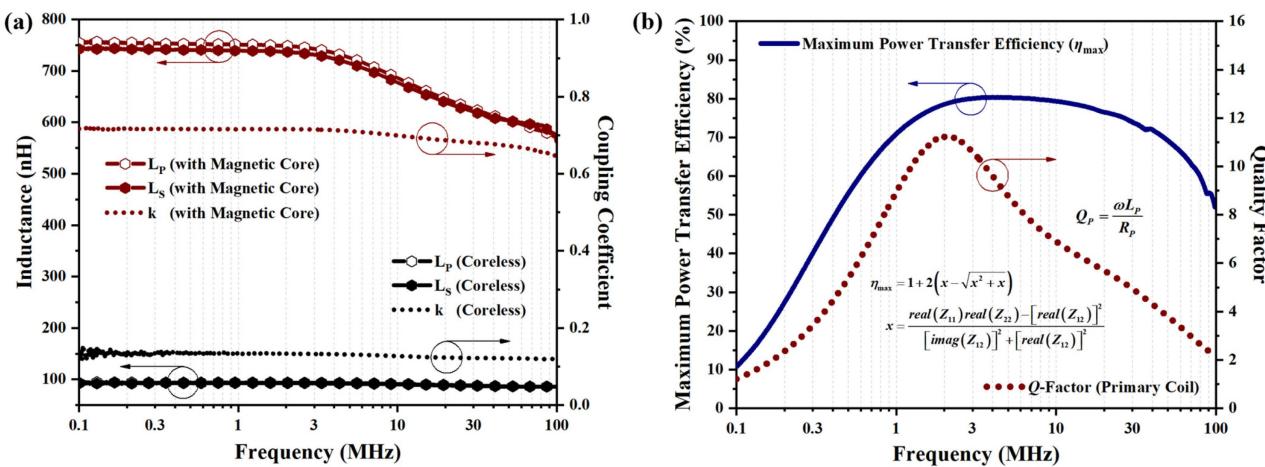
By converting the measured  $S$ -parameters to the impedance  $Z$ -matrix [37], the frequency-dependent inductance values,  $L$ , and the coupling coefficient  $k$  of the coupling coils in the transformer chips can then be extracted as follows:

$$L_P = \text{imag}(Z_{11})/\omega, L_S = \text{imag}(Z_{22})/\omega \quad (11)$$

$$k = \text{imag}(Z_{12})/\sqrt{\text{imag}(Z_{11}) \times \text{imag}(Z_{22})} = L_M/\sqrt{L_P \times L_S} \quad (12)$$

where  $L_P$ ,  $L_S$ , and  $L_M$  represent the measured primary inductance, secondary inductance, and mutual inductance of the coupling coils, respectively. In Figure 8a, the extracted inductance values, as well as the coupling coefficient from the HV-isolated transformer with inserted magnetic core, are plotted and compared with the coreless one. Benefiting from the inserted magnetic core, enormous increments in  $L_P$ ,  $L_S$ , and  $k$  are obtained, with the measurements improved from 93.3 nH, 92.1 nH, and 0.13 to 743.2 nH, 731.6 nH, and 0.72, respectively, at a targeted frequency of 3 MHz. Since the three-dimensional dense solenoidal coil structure occupies a tiny footprint of  $6 \text{ mm}^2$ , its inductance integration density reaches 123.9 nH/mm $^2$ , which is well above the value that the previously reported monolithic transformer can offer [20,38–41]. In addition, attributed to the high depth-to-width ratio of the thick-metal coil structure formed by the MEMS micro-casting process, an extremely low DC resistance of only  $0.39 \Omega$  is measured by the four-probe method for the HV-isolated transformer. Thus, combined with the measured inductance value, an ultra-high inductance-to-resistance ratio ( $L/R$ ) of over 1900 nH/ $\Omega$  is achieved.

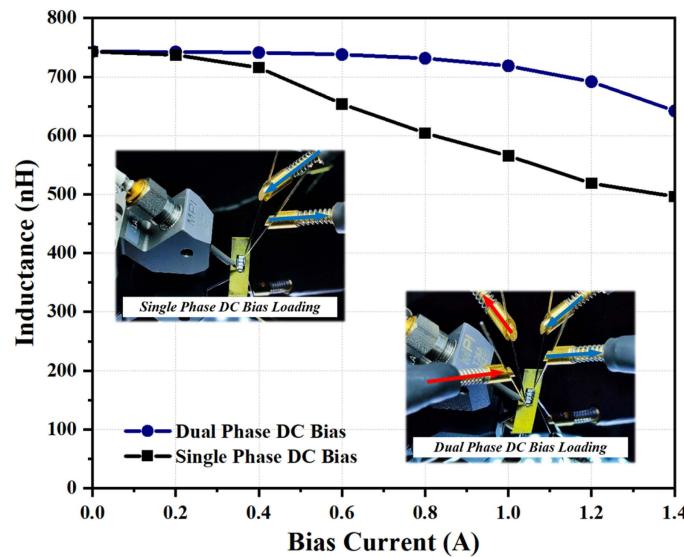
Plotted in Figure 8b are the measured  $Q$ -factor and the achieved maximum power transfer efficiency  $\eta_{max}$  versus frequency for the HV-isolated transformer with inserted ferrite magnetic core. It can be seen that high  $Q$ -factor performance is obtained and reaches its peak of 11.2 at 2.1 MHz. At higher frequencies, the increase in AC resistance caused by the skin effect and eddy current losses in the magnetic core leads to a certain decrease in the  $Q$ -factor. The achieved peak  $Q$ -factor surpasses that of conventional single-layer planar monolithic transformers, which exhibit a  $Q$ -factor of only 7.8 [19]. As an essential figure of merit, the maximum power transfer efficiency is adopted to evaluate the efficiency of the HV-isolated transformer, and it is extracted from the impedance  $Z$ -matrix by Kiat T. Ng's methods [42]. As shown in Figure 8b, a superior  $\eta_{max}$  performance for the HV-isolated transformer of over 70% at a wide range of frequencies is achieved. At the targeted frequency of 3 MHz, the maximum power transfer efficiency even exceeds 80%, which implies a minimal capacitive power loss and a well-controlled eddy current loss in both the silicon substrate and in ferrite magnetic core.



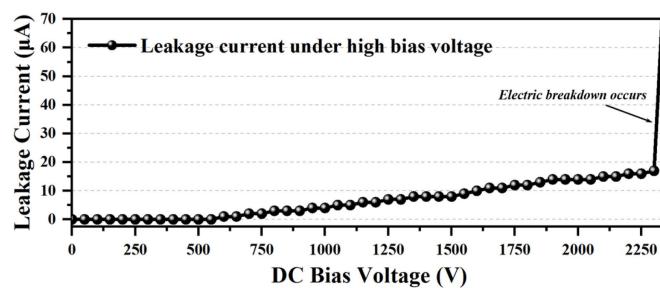
**Figure 8.** (a) Extracted frequency-dependent inductance values, as well as the coupling coefficient of the coupling coils in the fabricated HV-isolated transformer chips from the measured S-parameters. (b) Measured quality factor (Q-factor) and the achieved maximum power transfer efficiency versus frequency for the HV-isolated transformer with inserted ferrite magnetic core.

To assess the saturation current,  $I_{sat}$ , of the transformer, its inductance values at 3 MHz as a function of DC bias current are measured and plotted in Figure 9. Under dual-phase DC bias currents loading condition, since the magnetic fluxes generated by the balanced dual phase bias currents will be largely canceled with each other [43], an ultra-high saturation current of over 1.4 A is measured when the inductance value of the transformer chip drops to 80% of its initial value. Meanwhile, under the single-phase DC bias current loading condition, the measured saturation current is 0.8 A, which is still double the saturation current reported in [7]. Furthermore, the insulation strength of the fabricated HV-isolated transformer chip is also measured through the breakdown voltage test, as the breakdown voltage of a transformer device indicates the maximum voltage it can withstand [20]. As shown in Figure 10, the transformer survived under fatally high DC bias voltage applied between the terminal from primary and secondary windings with a value of 2300 V during the breakdown voltage test. The measured withstand voltage is about 20% lower than the 2787.1 V predicted by the previous finite element simulation results, presumably caused by the fact that the actual dielectric strength of the SiO<sub>2</sub> isolation barrier formed by thermal oxidation and oxidized LPCVD polysilicon is slightly lower than the material's theoretical dielectric strength. Nevertheless, such a high withstand voltage of 2300 V is sufficient to cover most practical applications.

The detailed parameters of the proposed high-voltage-isolated MEMS quad-solenoid transformers are compared with those of previously reported monolithically integrated transformers in Table 3. Thanks to the novel structural design and the newly developed MEMS micro-casting technique, our devices not only achieve a higher inductance integration density and inductance to resistance ratio but can also provide better maximum power transfer efficiency in lower operating frequencies.



**Figure 9.** Measured inductance values of the HV-isolated transformer at 3 MHz with DC bias currents loading at primary and/or secondary windings. The insets demonstrate the probing setup.



**Figure 10.** The measured leakage current as a function of high DC bias voltage applied between the primary and secondary windings in the HV-isolated transformer.

**Table 3.** Detailed comparisons between the proposed monolithically integrated HV-isolated transformers with previously reported related works.

Parameter	[38]	[39]	[40]	[41]	[20]	This Work
Magnetic core	Non	Yes	Yes	Non	Yes	Yes
Insulating materials	BCB	BCB	SiO <sub>2</sub>	SiO <sub>2</sub>	PI	SiO <sub>2</sub>
Frequency (MHz)	10	20	14	10	70	3
Inductance (nH)	159	80	114.9	113	47	743.2
Inductance density (nH/mm <sup>2</sup> )	79.5	22.85	8.64	56.5	10.44	123.9
Coupling coefficient	0.64	N/A	0.70	0.65	0.65	0.72
DC resistance (Ω)	0.4	0.34	0.15	0.31	0.5	0.39
L/R (nH/Ω)	398	235	766	360	94	1906
Isolation voltage (V)	4500	N/A	N/A	1050	500	2300
Max power transfer efficiency	70%	37%	N/A	70%	68%	80%

## 5. Conclusions

High-voltage-isolated MEMS quad-solenoid transformers with S-shaped SiO<sub>2</sub> isolation barriers were designed, simulated, and wafer-level batch fabricated for compact isolated gate driver solutions in this study. Attributed to the silicon-embedded thick-metal dense coupling coil structures metalized through the MEMS micro-casting process, a high Q-factor of up to 11.2 and one of the highest inductance integration densities among the

monolithically integrated transformers of  $123.9 \text{ nH/mm}^2$  were achieved. With the embedded  $10 \mu\text{m}$  thick S-shaped  $\text{SiO}_2$  insulating barriers, the maximum electric-field intensity in the insulating dielectric layers from the transformer can be well controlled and, thus, allow for a higher withstand voltage of 2300 V, which was measured in the preliminary breakdown voltage test. Moreover, the developed transformers are characterized by superior power transfer efficiencies of over 80% and also exhibit a high saturation current under both single- or dual-phase DC bias loading conditions. Therefore, the superior electromagnetic performances combined with the achieved high saturation current and withstand voltage allow the devices to be well integrated into the miniaturized galvanically isolated gate driver solutions with highly improved power densities and efficiencies.

**Author Contributions:** C.C. contributed to the investigation, design, simulation, and fabrication of the proposed device; P.P. contributed to the device testing; J.G. contributed to the fabrication methodology; and X.L. contributed to the research idea and project supervision. All authors have read and agreed to the published version of the manuscript.

**Funding:** This research was funded by the National Science Foundation of China (No. 61834007).

**Data Availability Statement:** The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

**Acknowledgments:** The authors appreciate the financial support from the National Science Foundation of China Projects (61834007, 62074151, 62227815) and the National Key Research and Development Program of the Ministry of Science and Technology of China (2021YFB3200800).

**Conflicts of Interest:** The authors declare no conflict of interest.

## References

1. Husain, I.; Ozpineci, B.; Islam, M.S.; Gürpinar, E.; Su, G.J.; Yu, W.; Chowdhury, S.; Xue, L.; Rahman, D.; Sahu, R. Electric Drive Technology Trends, Challenges, and Opportunities for Future Electric Vehicles. *Proc. IEEE* **2021**, *109*, 1039–1059. [[CrossRef](#)]
2. Sato, E.K.; Kinoshita, M.; Sanada, K. Double DC-DC converter for uninterruptible power supply applications. In Proceedings of the 2010 International Power Electronics Conference—ECCE ASIA, Sapporo, Japan, 21–24 June 2010; pp. 635–642.
3. Gayithri, C.; Dhanalakshmi, R. Analysis of power quality on a renewable energy micro grid conversion system with current and power controller. In Proceedings of the 2016 International Conference on Advanced Communication Control and Computing Technologies (ICACCCT), Ramanathapuram, India, 25–27 May 2016; pp. 449–453.
4. Saeed, M.H.; Fangzong, W.; Kalwar, B.A.; Iqbal, S. A Review on Microgrids’ Challenges & Perspectives. *IEEE Access* **2021**, *9*, 166502–166517. [[CrossRef](#)]
5. Millán, J.; Godignon, P.; Perpiñà, X.; Pérez-Tomás, A.; Rebollo, J. A Survey of Wide Bandgap Power Semiconductor Devices. *IEEE Trans. Power Electron.* **2014**, *29*, 2155–2163. [[CrossRef](#)]
6. Gürpinar, E.; Chowdhury, S.; Ozpineci, B.; Fan, W. Graphite-Embedded High-Performance Insulated Metal Substrate for Wide-Bandgap Power Modules. *IEEE Trans. Power Electron.* **2021**, *36*, 114–128. [[CrossRef](#)]
7. Wang, N.; Miftakhutdinov, R.; Kulkarni, S.; O’Mathuna, C. High Efficiency on Si-Integrated Microtransformers for Isolated Power Conversion Applications. *IEEE Trans. Power Electron.* **2015**, *30*, 5746–5754. [[CrossRef](#)]
8. Ragonese, E.; Parisi, A.; Spina, N.; Palmisano, G. Fully Integrated Galvanically Isolated DC-DC Converters Based on Inductive Coupling. In Proceedings of the Applications in Electronics Pervading Industry; Environment and Society: Cham, Switzerland, 2019; pp. 335–341.
9. Ragonese, E.; Spina, N.; Castorina, A.; Lombardo, P.; Greco, N.; Parisi, A.; Palmisano, G. A Fully Integrated Galvanically Isolated DC-DC Converter With Data Communication. *IEEE Trans. Circuits Syst. Regul. Pap.* **2018**, *65*, 1432–1441. [[CrossRef](#)]
10. Ma, S.; Zhao, T.; Chen, B. 4A isolated half-bridge gate driver with 4.5V to 18V output drive voltage. In Proceedings of the 2014 IEEE Applied Power Electronics Conference and Exposition—APEC, Fort Worth, TX, USA, 16–20 March 2014; pp. 1490–1493. [[CrossRef](#)]
11. Ragonese, E.; Spina, N.; Parisi, A.; Palmisano, G. An Experimental Comparison of Galvanically Isolated DC-DC Converters: Isolation Technology and Integration Approach. *Electronics* **2021**, *10*, 1186. [[CrossRef](#)]
12. Panov, Y.; Jovanovic, M.M. Small-signal analysis and control design of isolated power supplies with optocoupler feedback. *IEEE Trans. Power Electron.* **2005**, *20*, 823–832. [[CrossRef](#)]
13. Garcia, J.; Saeed, S.; Gürpinar, E.; Castellazzi, A.; Garcia, P. Self-Powering High Frequency Modulated SiC Power MOSFET Isolated Gate Driver. *IEEE Trans. Ind. Appl.* **2019**, *55*, 3967–3977. [[CrossRef](#)]
14. Wu, R.; Sin, J.K.O.; Hui, S.Y. A novel silicon-embedded coreless transformer for isolated DC-DC converter application. In Proceedings of the 2011 IEEE 23rd International Symposium on Power Semiconductor Devices and ICs, San Diego, CA, USA, 23–26 May 2011; pp. 352–355.

15. Khan, F.; Zhu, Y.; Lu, J.; Pal, J.; Dao, D.V. Micromachined Coreless Single-Layer Transformer Without Crossovers. *IEEE Magn. Lett.* **2015**, *6*, 6500404. [[CrossRef](#)]
16. Wu, R.; Liao, N.; Fang, X.; Sin, J.K.O. A silicon-embedded transformer for high-efficiency, high-isolation, and low-frequency on-chip power transfer. *IEEE Trans. Electron Devices* **2015**, *62*, 220–223. [[CrossRef](#)]
17. Chen, B. Fully integrated isolated DC-DC converter using micro-transformers. In Proceedings of the 2008 Twenty-Third Annual IEEE Applied Power Electronics Conference and Exposition—APEC, Austin, TX, USA, 24–28 February 2008; pp. 335–338. [[CrossRef](#)]
18. Feeney, C.; Yu, J.; Peng, S.; Ye, T.; Yang, S.; Wang, N. Thin Film Magnetic Core Microinductor With Stacked Windings. *IEEE Trans. Electron Devices* **2021**, *68*, 4237–4241. [[CrossRef](#)]
19. Cheng, M.; Liu, L.; Liao, Z.; Yu, J.; Peng, S.; Zhang, Z.; Ye, T.; Wang, N. On Silicon-Integrated Micro-Transformers and Their Applications in Quasi-Resonant Flyback Converters. *IEEE Trans. Magn.* **2022**, *58*, 8401209. [[CrossRef](#)]
20. Mundotiya, B.M.; Dinulovic, D.; Rissing, L.; Wurz, M.C. Fabrication and characterization of a Ni-Fe-W core microtransformer for high-frequency power applications. *Sen. Actuators A Phys.* **2017**, *267*, 42–47. [[CrossRef](#)]
21. Ahmed, M.Z.; Bhuyan, M.S.; Islam, A.K.M.T.; Majlis, B.Y. Design and Fabrication of a MEMS 3D Micro-transformer for Low Frequency Applications. *Asian J. Sci. Res.* **2015**, *8*, 237–244. [[CrossRef](#)]
22. Xing, X.; Sun, N.X.; Chen, B. High-bandwidth low-insertion loss solenoid transformers using FeCoB multilayers. *IEEE Trans. Power Electron.* **2013**, *28*, 4395–4401. [[CrossRef](#)]
23. Gu, J.; Liu, B.; Chen, G.; Li, X. Study of a through-silicon/substrate via filling method based on the combinative effect of capillary action and liquid bridge rupture. *J. Micromech. Microeng.* **2016**, *26*, 075009. [[CrossRef](#)]
24. Gu, J.; Liu, B.; Yang, H.; Li, X. A metal micro-casting method for through-silicon Via (TSV) fabrication. In Proceedings of the 2017 IEEE Electron Devices Technology and Manufacturing Conference (EDTM), Toyama, Japan, 28 February–2 March 2017; pp. 211–212.
25. Lee, D.W.; Wang, S.X. Effects of geometries on permeability spectra of CoTaZr magnetic cores for high frequency applications. *J. Appl. Phys.* **2008**, *103*, 07E907. [[CrossRef](#)]
26. Jun-Bo, Y.; Bon-Kee, K.; Chul-Hi, H.; Euisik, Y.; Kwyro, L.; Choong-Ki, K. High-performance electroplated solenoid-type integrated inductor (SI2) for RF applications using simple 3D surface micromachining technology. In Proceedings of the International Electron Devices Meeting 1998. Technical Digest (Cat. No.98CH36217), San Francisco, CA, USA, 6–9 December 1998; pp. 544–547.
27. Chen, D.X.; Brug, J.A.; Goldfarb, R.B. Demagnetizing factors for cylinders. *IEEE Trans. Magn.* **1991**, *27*, 3601–3619. [[CrossRef](#)]
28. Chen, D.X.; Pardo, E.; Sanchez, A. Demagnetizing factors of rectangular prisms and ellipsoids. *IEEE Trans. Magn.* **2002**, *38*, 1742–1752. [[CrossRef](#)]
29. Harrington, R.F. *Time-Harmonic Electromagnetic Fields*; McGraw-Hill: New York, NY, USA, 1961.
30. Lee, D.W.; Hwang, K.P.; Wang, S.X. Fabrication and Analysis of High-Performance Integrated Solenoid Inductor With Magnetic Core. *IEEE Trans. Magn.* **2008**, *44*, 4089–4095. [[CrossRef](#)]
31. Reatti, A.; Kazimierczuk, M.K. Comparison of various methods for calculating the AC resistance of inductors. *IEEE Trans. Magn.* **2002**, *38*, 1512–1518. [[CrossRef](#)]
32. Guevara-Morales, A.; Taylor, A.C. Mechanical and dielectric properties of epoxy-clay nanocomposites. *J. Mater. Sci.* **2014**, *49*, 1574–1584. [[CrossRef](#)]
33. Muramoto, Y.; Shimizu, N.; Fukuma, M.; Nagao, M. Effect of space charge on conduction current and breakdown of polyimide films. In Proceedings of the 8th IEEE International Conference on Solid Dielectrics, Toulouse, France, 5–9 July 2004; pp. 41–44.
34. Modafe, A.; Ghalichehian, N.; Kleber, B.; Ghodssi, R. Electrical characterization of BCB for electrostatic microelectromechanical devices. In Proceedings of the Symposium on Micro- and Nanosystems held at the 2003 MRS Fall Meeting, Boston, MA, USA, 1–3 December 2004; pp. 305–310.
35. Rojas, S.; Modelli, A.; Wu, W.S.; Borghesi, A.; Pivac, B. Properties of Silicon Dioxide Films Prepared by Low-Pressure Chemical Vapor-Deposition from Tetraethylorthosilicate. *J. Vac. Sci. Technol. B* **1990**, *8*, 1177–1184. [[CrossRef](#)]
36. Ghodssi, R.; Lin, P. *MEMS Materials and Processes Handbook*; Springer Science & Business Media: Berlin, Germany, 2011; Volume 1.
37. Frickey, D.A. Conversions Between S, Z, Y, h, ABCD, and T Parameters which are Valid for Complex Source and Load Impedances. *IEEE Trans. Microw. Theory Tech.* **1994**, *42*, 205–211. [[CrossRef](#)]
38. Wu, R.; Liao, N.; Fang, X.; Cai, J.; Wang, Q.; Sin, J.K.O. A 3D Assembled Silicon-Embedded Transformer for 10-MHz, Ultra-High-Isolation, Compact Chip-to-Chip Power Transfer. *IEEE Electron Device Lett.* **2017**, *38*, 356–358. [[CrossRef](#)]
39. Wang, N.; Kulkarni, S.; Jamieson, B.; Rohan, J.; Casey, D.; Roy, S.; Mathuna, C.O. High efficiency Si integrated micro-transformers using stacked copper windings for power conversion applications. In Proceedings of the 2012 Twenty-Seventh Annual IEEE Applied Power Electronics Conference and Exposition (APEC), Orlando, FL, USA, 5–9 February 2012; pp. 411–416.
40. Li, H.; Zhu, K.; Lei, K.; Xu, T.; Wu, H. Integrated MEMS Toroidal Transformer With Ni-Zn Ferrite Core for Power Supply on Chip. *IEEE Trans. Power Electron.* **2022**, *37*, 10075–10080. [[CrossRef](#)]
41. Wu, R.; Liao, N.; Fang, X.; Sin, J.K.O. A Novel Double-Side Silicon-Embedded Transformer for 10-MHz, 1-kV-Isolation, Compact Power Transfer Applications. *IEEE Trans. Electron Devices* **2016**, *63*, 4542–4545. [[CrossRef](#)]

42. Ng, K.T.; Rejaei, B.; Burghartz, J.N. Substrate effects in monolithic RF transformers on silicon. *IEEE Trans. Microw. Theory Tech.* **2002**, *50*, 377–383. [[CrossRef](#)]
43. He, Y.; Wu, R.; Zhong, Z.; Zhang, H.; Bai, F. On-Chip Coupled Solenoid Inductors for Integrated Power Conversion. *IEEE Trans. Electron Devices* **2021**, *68*, 6292–6295. [[CrossRef](#)]

**Disclaimer/Publisher’s Note:** The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.