

Review

Current Understanding of Bias-Temperature Instabilities in GaN MIS Transistors for Power Switching Applications

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Received: 30 November 2020; Accepted: 14 December 2020; Published: 18 December 2020



Abstract: GaN-based high-electron mobility transistors (HEMTs) have brought unprecedented performance in terms of power, frequency, and efficiency. Application of metal-insulator-semiconductor (MIS) gate structure has enabled further development of these devices by improving the gate leakage characteristics, gate controllability, and stability, and offered several approaches to achieve E-mode operation desired for switching devices. Yet, bias-temperature instabilities (BTI) in GaN MIS transistors represent one of the major concerns. This paper reviews BTI in D- and E-mode GaN MISHEMTs and fully recess-gate E-mode devices (MISFETs). Special attention is given to discussion of existing models describing the defects distribution in the GaN-based MIS gate structures as well as related trapping mechanisms responsible for threshold voltage instabilities. Selected technological approaches for improving the dielectric/III-N interfaces and techniques for BTI investigation in GaN MISHEMTs and MISFETs are also outlined.

Keywords: GaN transistors; MIS/MOS; MISHEMT; MISFET; PBTI; NBTI; threshold voltage instability; interface traps; oxide traps

1. Introduction

A combination of wide band gap (3.4 eV), high breakdown electric field (3 MV/cm), decent thermal conductivity (>1.5 W/cmK), and high saturation velocity ($\sim 10^7$ cm/s) of electrons makes GaN an ideal material for high-power semiconductor devices [1–3]. Indeed, GaN-based high electron-mobility transistors (HEMTs) with high cut-off frequency and high breakdown voltage (V_{BD}) enabled development of new generation of power amplifiers implemented in wireless communication, satellite, and radar systems commercially available already a decade ago [4]. More recently, GaN HEMTs have been also applied as switching devices for power converters. Despite relatively immature technology, the state-of-the-art GaN switching devices have shown lower ON-state resistance (R_{ON}) for given V_{BD} compared to current power devices based on Si [5–7]. Intensive R&D effort in the last decade paved the way to emerging of highly efficient and compact GaN-based power converters in the market [8]. However, the issues related to stability and reliability of GaN power switching devices hamper a more dramatic commercial success of this technology. To take advantage of outstanding properties of GaN material, a key task is to gain a fundamental understanding of the parasitic and degradation mechanisms that negatively affect the performance and long-term reliable operation of these devices. This represents a rather difficult task, keeping in mind the unique properties of GaN-based materials (wide-band gap nature, piezoelectricity) and high electric field combined with dissipating power of the operating devices. In addition, GaN heterostructures for lateral transistors are grown on foreign substrates. Therefore, a variety of extended defects are present in the device active region.

GaN HEMTs with Schottky-barrier gates often suffer from relatively large gate leakage current (I_G) [9]. An effective way to suppress the excessive I_G is to employ metal-insulator-semiconductor

(MIS) gate structure. MISHEMTs with largely suppressed I_G as compared to Schottky-gated devices has been reported by many groups using various gate dielectrics including Al_2O_3 , Si_3N_4 , SiO_2 , AlN , HfO_2 , and others [9]. By suppressing I_G in particular at forward bias, MISHEMTs with improved gate controllability and stability under DC as well as RF operation have been reported [10]. In addition, MIS gate structure offer several approaches to achieve E-mode transistor operation, which is highly desired for switching devices. Proposed E-mode concepts are based on increased gate capacitance using partial [11] or full barrier recessing [12] and/or introduction of sufficiently high negative charge at the dielectric/barrier interface [13] or in the dielectric layer itself [14]. Yet, dielectric/barrier interface in the MIS gate structure inevitably contains interfacial defect levels that can interact with free electrons from the 2DEG channel or metal electrode [15–18]. Depending on the distribution of these traps, MISHEMTs suffer from threshold voltage (V_{TH}) stability issues, known as bias temperature instability (BTI) in the literature.

BTI represents a reliability issue, manifested by the change of the transistor's V_{TH} under applied gate bias, resulting in the change of the drain current (I_D) and transconductance (g_m) of the device. It is generally enhanced by the stress voltage and temperature. BTI effects can be recoverable at less severe conditions and originate from the trapping effects. In the harsher conditions, new traps in the gate stack (typically interface states) can be also formed [19], leading to permanent change of V_{TH} . In BTI test, either positive (PBTI) or negative (NBTI) bias is applied on the gate electrode (while the source and drain electrodes are grounded, i.e., $V_{DS} = 0$) at elevated temperature and change of the electrical parameters during both, stressing and recovery period is monitored.

In GaN MISHEMTs, BTI represents one of the biggest reliability concerns. This is due to relatively high density of traps located in the gate stack, being a consequence of unavailability of high-quality native oxides for GaN-based semiconductors and complexity of the dielectric/III-N interfaces. As a result, considerable BTI with V_{TH} instabilities ranging from 100 mV up to several V have been commonly reported for GaN MISHEMTs in the literature [20,21]. For D-mode MISHEMTs, NBTI is expected to be a major concern as the device is commonly biased in OFF-state with $V_{GS} < 0$. Indeed, several researchers have reported NBTI to induce negative V_{TH} drift strongly enhanced by temperature [21]. Although PBTI may be considered less problematic in these devices, many studies have been devoted to PBTI investigations in D-mode MISHEMTs with an aim to analyze the underlying mechanism of V_{TH} drift [22]. The dynamics of the PBTI in GaN MISHEMTs was found to differ from that known for Si metal-oxide-semiconductor field-effect transistors (MOSFET), mostly because of coaction of different trapping states in the gate stack, nontrivial defect dynamics, and electron transport over the existing barrier affecting the trapping dynamic [23]. For E-mode MISHEMTs, PBTI is clearly the major concern as the positive V_{GS} drives the device into ON-state. Dramatic V_{TH} drifts upon PBTI testing has been reported in the literature [24]. In addition, specific designs for achieving E-mode behavior for MISHEMTs, such as application of InGaN/AlGaIn double barrier layer, have been shown to result in a unique mechanism of PBTI [25]. GaN transistors with fully recessed barrier (also known as recessed gate hybrid MISHEMTs [26]) represent a special design of E-mode GaN devices, referred here to as GaN MISFETs. A complete etching-away of the barrier layer under the gate greatly simplifies the interpretation of the BTI data. Available studies investigating BTI in GaN MISFETs consistently indicate that both PBTI and NBTI need to be concerned. Moreover, it seems that dielectric bulk traps with specific distribution play a major role affecting the PBTI as well as NBTI behavior [27,28].

Up to now, BTI has been reviewed separately for D-mode MISHEMTs [21,23] and E-mode GaN MISFETs [29]. Intention of this review is to provide a full picture of BTI phenomenon in GaN MIS-gated switching transistors, based on most recent reports on D- and E-mode GaN MISHEMTs as well as E-mode GaN MISFETs. In particular, we focus on the existing models for origin of defect states present in the GaN MIS gate stacks and the underlying physics of their capture and emission processes leading to V_{TH} drift. The paper is organized as follows: In Section 2, we will describe the device concepts, existing models for trap distribution in different MIS gate structures, related trapping mechanisms, and the methods used for BTI investigation. In Sections 3 and 4, we will review most recent studies of

BTI in GaN MISHEMTs and MISFETs, respectively. Finally, the summary and prospects will be given in Section 5.

2. Devices, Models, and Methods

2.1. GaN MISHEMTs and MISFETs

The schematic of a lateral GaN MISHEMT is depicted in Figure 1a. The device concept employs the effect of polarization charges at the heterointerface between the GaN channel and a thin barrier layer (AlGaN, AlInN, AlN), originating from the difference between spontaneous and/or piezoelectric polarization of these layers. This essentially fixed charge gives rise to formation of 2-dimensional electron gas (2DEG) with a high density of free electrons ($\sim 0.8\text{--}3 \times 10^{13} \text{ cm}^{-2}$) in the GaN channel [30]. In contrast to Schottky barrier gate, the insulated gate ensures the suppression of the excessive gate leakage and extends the gate voltage span towards the positive values. Gate dielectric/barrier/GaN MIS structure includes two interfaces that in general contain fixed polarization charge as well as defect states, which can exchange their charge with the carrier reservoirs in the 2DEG and metal electrode.

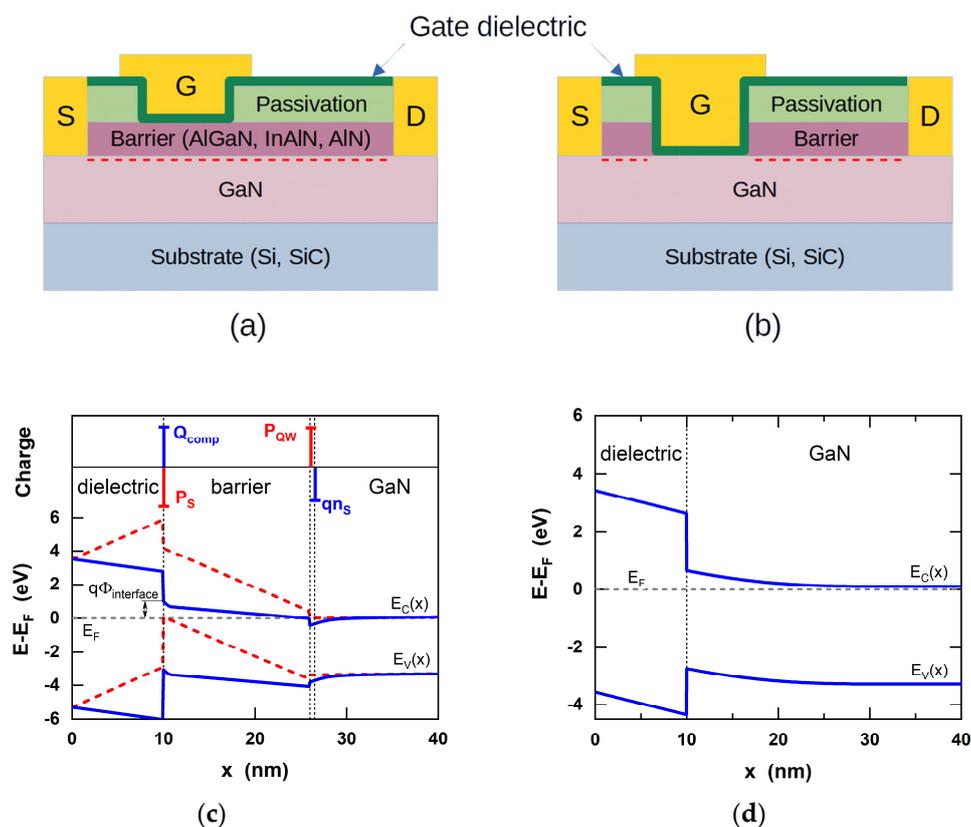


Figure 1. The schematic of the lateral GaN metal-insulator-semiconductor high-electron mobility transistors (MISHEMT) (a) and fully barrier recess-gate MIS field effect transistor (MISFET) (b) with corresponding band-diagrams across the gate structure (c,d). In (c), interface potential $\Phi_{interface}$ is defined and also charge distributions with fully compensated (solid blue lines) and uncompensated (dashed red lines) surface polarization charge P_S are depicted.

The band diagram of MISHEMT across the gate structure is shown in Figure 1c for heterostructure with Ga-face polarity [30]. Note that the electrically neutral dielectric/barrier interface is implicitly assumed in this model. This means that the negative polarization charge located at the surface of the barrier (P_S) is assumed to be fully compensated by some charge of similar density and opposite polarity (Q_{comp}), i.e., $P_S + Q_{comp} \approx 0$. Otherwise, uncompensated P_S would rise the bands at the interface and deplete the 2DEG channel (shown by the dashed lines in Figure 1c), which is in clear contrast to

commonly observed behavior of GaN MISHEMTs. The origin and nature of the compensating charge is not fully clear yet and remains the subject of debate. It is commonly accepted that P_S is compensated by surface donor states with a single level [31] or distribution of levels [32] with the density well above 10^{13} cm^{-2} , also providing free electrons into 2DEG, as originally proposed by Ibbetson et al. [31]. In MISHEMT structure, these surface donor states should act as interface states and contribute to PBTI [33]. Alternatively, acceptor-like interface states causing PBTI may coexist with the donor states defining the 2DEG density [23]. However, the lack of correlation between evaluated interface state density and P_S observed by several researchers [34–37] led to introduction of other models for origin of Q_{comp} . These models assume fixed charge formed by the ionized donor states between conduction band (CB) edges of the barrier and the dielectric layer [35,38,39], or the near-interface traps located spatially in the dielectric and energetically below the barrier CB edge [34]. Recently, Ber et al. [37] proposed a surface polarization self-compensation mechanism. The authors speculated that in contrast to ordered arrangement of ions at the epitaxial barrier/GaN interface, displacement of less rigid surface ions may be responsible for P_S self-compensation effect [37].

2.1.1. E-Mode GaN MIS Transistors

Due to the equilibrium population of 2DEG in the GaN channel, GaN MISHEMTs are inherently D-mode devices. Considering the converter topology and its safe operation, it is strongly desirable to implement the switching devices with E-mode transistors with sufficiently high positive V_{TH} [40]. This requirement ensures the robustness of the switch against the unwanted random turn-on and avoid hazardous voltage on the terminals in the case of control electronics failure. There are two fundamental approaches for achieving E-mode operation of GaN MISHEMTs: (i) introduction of sufficiently high (density $> 1.8 \times 10^{13} \text{ cm}^{-2}$ [41]) of negative interface charge ($Q_{interface}$) leading to increase of the interface potential ($\Phi_{interface}$, see Figure 1c) and (ii) increasing of the gate capacitance, preferably by decreasing of the barrier thickness [42]. Processing of the E-mode MISHEMTs using the first approach have been reported by employing F plasma treatment (fluorination) underneath the gate [14], control over the $Q_{interface}$ [43–46], and polarization engineering concept using InGaN/AlGaN barrier double-layer [13].

Using the second approach, preparation of E-mode GaN MISHEMTs with partially recess-barrier under the gate have been reported [47,48]. In the limiting case, the barrier under the gate can be fully recessed (Figure 1b), which provides E-mode transistor operation [12,48–51]. The band structure exemplified in Figure 1d shows that the electrons under the gate are depleted and interrupt the conductive channel between the source and drain access regions (Figure 1b). As this device connects in series the recessed MIS channel with two access regions having a low resistance due to the presence of 2DEG, it is often referred to as GaN recess-gate hybrid MISHEMTs [49,50] or MISFETs [12,52] in the literature. In this review, we will refer to these devices as GaN MISFETs. In contrast to inversion type Si MOSFETs, GaN MISFETs are majority carrier transistors. R_{ON} is given by relatively low access resistances and the intrinsic channel resistance, proportional to the gate length and the GaN channel mobility, which is a strong function of the dielectric/GaN interface quality.

2.1.2. Gate Materials and Technologies

The main requirements of an MIS gate structure are suppression of the gate leakage even at forward bias and its stability at different operating conditions. In addition, the process technology needs to be robust and limits the resulting V_{TH} dispersion. For an optimal design of the gate structure, it is necessary to consider the bandgap, band offsets, dielectric constant, breakdown field, and chemical stability of the dielectric with III-N semiconductor. For suppression of the gate leakage current, a dielectric with large band offsets in respect to GaN needs to be selected. Although the dielectrics with high permittivity (high- k dielectrics) allow fabrication of transistors with high g_m , the general tradeoff between bandgap and dielectric constant restricts the applicability of several high- k dielectrics for GaN MISHEMTs [9]. Importantly, the defects in the dielectric and its interface with semiconductor affects the V_{TH} stability and, in the case of GaN MISFETs, also channel mobility [26].

In addition to the selection of the gate dielectric, it is as well necessary to adopt a suitable technology including the III-N surface pre-treatment, gate dielectric deposition method, and MIS gate post-treatment. Several high- k dielectrics such as HfO_2 , ZrO_2 , GdScO_3 , Ta_2O_5 , LaLuO_3 , La_2O_3 , MgCaO , TiO_2 [53–59], etc. have been applied as the gate dielectrics in GaN MISHEMTs. However, nowadays, Al_2O_3 (and Al-based oxides), SiO_2 , and SiN_x are most commonly used dielectrics materials. Al_2O_3 has relatively large band gap (6.7–7.0 [60]), high breakdown field (~ 10 MV/cm) and sufficiently large band offset in respect to AlGaN/GaN. It is typically grown by atomic layer deposition (ALD) using various oxidation agents (H_2O [15,61], O_2 -plasma [62], O_3 [63]) at moderate temperatures ranging from 100 to 300 °C. High-quality ALD Al_2O_3 gate dielectrics for GaN MISHEMTs and MISFETs have been reported by several groups, exhibiting low gate leakage current, nearly theoretical breakdown field, and excellent interface properties [61,64–67]. Growth of Al_2O_3 using MOCVD at higher temperatures (600 °C) has been also reported [55]. In order to improve the thermal stability of Al_2O_3 beyond 800 °C, application of aluminum oxynitride (AlON) and $\text{Al}_2\text{O}_3/\text{SiO}_2$ nanolaminates grown by ALD has been demonstrated [68,69].

Despite its lower dielectric constant (3.9), SiO_2 has the highest band gap (~ 9 eV) among other dielectrics. It is typically deposited by plasma-enhanced chemical vapor deposition (PECVD) with subsequent post-deposition annealing (PDA). High-quality SiO_2 gate dielectrics with breakdown field reaching 11 MV/cm [70] have been applied to GaN MISHEMTs [71] and MISFETs [72] with excellent electrical properties. Although SiN_x has been primarily used as the passivation layer in GaN HEMTs, several groups reported its application as the gate dielectric [27,73–75]. SiN_x can be grown by in-situ MOCVD, PECVD [73,74], low-pressure CVD, and plasma-enhanced ALD [27,75]. Although MISFETs with SiN_x exhibit good dielectric/GaN interface quality [73], MISHEMTs often show relatively high gate leakage at forward bias due to small CB offset [76]. This issue has been overcome by e.g., deposition of the $\text{SiN}_x/\text{Al}_2\text{O}_3$ dielectric bilayer [77]. Finally, the quality of dielectric-III/N interface can be improved by surface pre-treatment such as Cl_2 -based inductively coupled plasma etching [61], in-situ remote plasma treatment [78], application of AlN interlayer [79], or the gate metal post-treatment [80].

2.2. Modeling of Defect States in the Gate Stack

BTI is dominantly affected by the dynamics of various trapping states in the gate stack. In the following, we will summarize current understanding of the defect's origin, their nature and spatial distribution in GaN MIS gate structure. We will also describe the most relevant empirical models of the defect states and the observed BTI behavior proposed in the literature.

2.2.1. Interface Traps

Interface traps (IT) represent allowed states in the semiconductor bandgap located at its interface with the dielectric, as depicted in Figure 2a. In general, IT can be divided into intrinsic states of the semiconductor surface and extrinsic interface defects. Intrinsic interface states are associated with the surface reconstruction of the crystal termination and, for III-N surfaces, they are most likely formed by the vacancies and dangling bonds [81]. Extrinsic interface defects originate from adsorbed foreign atoms, sub-oxides, and structural imperfections and in general depends upon semiconductor surface cleaning, dielectric material, and the method of its deposition. Although several IT models have been proposed in the literature (for more comprehensive review see, e.g., Eller et al. [82]), no specific IT model exist for dielectric/III-N interfaces. Yet, several researchers [16,76,83] adopted disorder-induced gap state (DIGS) model proposed by Hasegawa et al. [84], originally introduced for III-V MIS structures. The model assumes existence of several monolayers thick disordered layer at the semiconductor surface with distortion of lengths and angles of the local bonds. This leads to formation of continuum of IT states energetically distributed with typical U-shape within the semiconductor bandgap $D_{IT}(E_{IT})$ (depicted in Figure 2b). Here, acceptor-like (anti-bonding) trap states and donor-like (bonding) trap states are divided by charge neutrality level (E_{CNL}) [84]. Although it is challenging to experimentally distinguish between response of IT and other traps in the gate stack, relatively high D_{IT} in the range

of 10^{12} – 10^{13} $\text{eV}^{-1}\text{cm}^{-2}$ has been consistently reported for GaN MISHEMT structures using various methods, including capacitance–voltage (CV) method [17,85], photo-assisted CV [18], C-transients [16], deep-level transient spectroscopy (DLTS) [86], and AC admittance (C- ω , G- ω) techniques [15,78]. However, special care must be taken in the interpretation of these techniques for D_{IT} evaluation as the gate bias and temperature dependence of the barrier conductivity can affect the frequency response of the MISHEMT gate admittance even without the presence of IT [87].

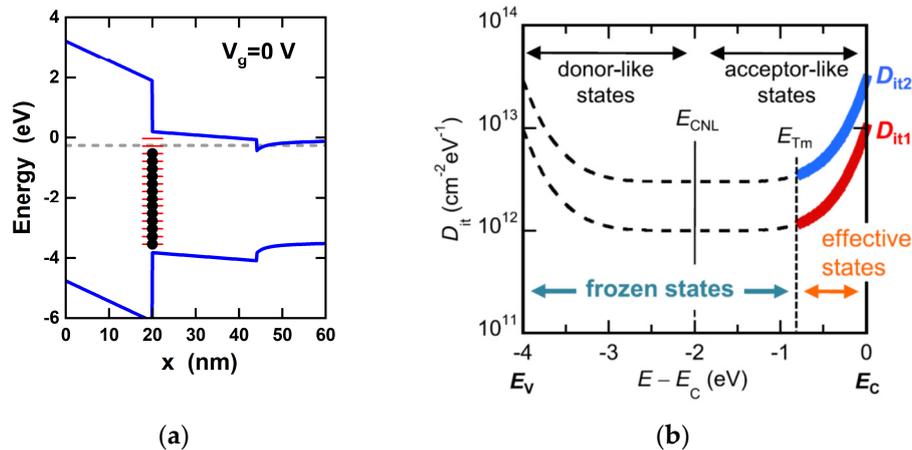


Figure 2. (a) Schematic illustration of interface traps in $\text{Al}_2\text{O}_3/\text{AlGaIn}/\text{GaN}$ MIS heterostructure. (b) Example of two U-shape D_{IT} energy distributions at $\text{Al}_2\text{O}_3/\text{AlGaIn}$ interface used for capacitance–voltage (CV) simulations, highlighting interface traps in the upper part of the bandgap that affect the CV stretch-out. Panel (b) reprinted from [15], with the permission of AIP Publishing. Copyright © 2020 AIP.

A wide band gap nature of GaN based semiconductors needs to be also considered in evaluation of D_{IT} energy distribution in GaN MIS heterostructures. First, due to extremely low density of holes in GaN, hole capture/emission can be readily neglected. Second, IT with a wide range of energies in the semiconductor band gap are characterized by extremely wide range of time responses. Using classical Shockley–Read–Hall (SRH) theory, capture and emission processes can be described in terms of capture and emission time constants [88]

$$\tau_C = \frac{1}{nv_{TH}\sigma}, \quad (1)$$

$$\tau_E = \frac{1}{N_C v_{TH} \sigma} \exp\left(\frac{E_C - E_{IT}}{k_B T}\right) \quad (2)$$

where n , N_C , v_{TH} , σ , $E_C - E_{IT}$, k_B , and T are the concentration of electrons and effective density of states at the conduction band, the thermal velocity of electrons, the capture cross-section and IT energy position measured from the CB bottom, the Boltzmann constant, and temperature, respectively. While τ_C depends only on σ and the number of free electrons available for capture, τ_E also depends exponentially on E_{IT} , because trapped electron must gain enough thermal energy to be transferred to CB. As pointed out by Miczek et al. [88], only shallower IT with $E_C - E < \sim 1$ eV (assuming $\sigma = 10^{-16}$ cm^2 and room temperature) are capable to emit electrons into conduction band of the semiconductor within 100 s, i.e., practical time for CV measurements. For IT with $E_C - E > \sim 1$ eV, however, V_G -induced Fermi level movement below the trap level towards the valence band (VB) does not change their occupation and these traps remain frozen, as depicted in Figure 2b [15]. This implies a fundamental limitation for application of standard capacitance and admittance methods used for $D_{IT}(E_{IT})$ determination.

IT represents one of the major concerns in relation to BTI in GaN MISHEMTs. In fact, relatively large variation in reported D_{IT} ranging from 10^{11} up to 10^{13} $\text{eV}^{-2}\text{cm}^{-2}$ can be found in the literature. Yet, recently, Hashizume et al. [80] has reported ALD-grown $\text{Al}_2\text{O}_3/\text{GaN-on-GaN}$ MIS structures with superior interface quality, as documented by D_{IT} on the level of 10^{10} $\text{eV}^{-2}\text{cm}^{-2}$. This illustrates that combination of high-quality GaN channel region, optimized ALD process, careful surface pre-treatment,

and post-deposition annealing can provide dielectric/GaN interface with quality similar to that of SiO₂/Si interface.

2.2.2. Disorder-Induced Gap States in the Gate Dielectric

Existence of DIGS in the gate dielectric has been proposed by Matys et al. [89] in order to describe complex PBTI and NBTI behavior of Al₂O₃/AlGaIn/GaN MISHEMT structures. Similar to DIGS model discussed above, U-shaped energy distribution of DIGS that exponentially decay toward the dielectric bulk (up to 4 nm) from its interface with the barrier is assumed in this model. The density of DIGS, their energy, and spatial distribution depend upon nature and degree of the disorder introduced upon the gate dielectric technology. It can be expressed as [90]

$$N_{DIGS}(E, x) = N_0 \exp\left(\left|\frac{E - E_{CNL}}{E_{0d,0a}}\right|^{n_{d,a}}\right) \exp\left(-\frac{x}{x_l}\right) \quad (3)$$

where N_0 is the DIGS minimum density, E_{0d}/E_{0a} and n_d/n_a describe the energy shape of the donor/acceptor-like branch, respectively, and x_l describes the DIGS spatial distribution. The capture and emission behavior of DIGS is then described by SRH statistics and tunneling-assisted processes with x -dependent capture cross-section expressed as [91]

$$\sigma(x) = \sigma_0 \exp(-x/x_0). \quad (4)$$

In Equation (4), σ_0 is the electron capture cross-section of the states at the interface and x_0 is the tunneling decay length given by $x_0 = \hbar / \sqrt{2m_e \Delta E_C}$, where m_e is the effective mass of the electron and ΔE_C is the CB offset at the dielectric/barrier interface.

In addition to the energy distribution, the introduction of spatial distribution of trap states provides another time and gate voltage dependent component into the trapping/de-trapping behavior. Let us illustrate the impact of DIGS on a CV hysteresis measurement. Under forward sweep toward positive V_G , DIGS located deeper in the dielectric are progressively populated. For reverse sweep toward negative V_G , when the Fermi level moves towards the AlGaIn VB, shallower DIGS near the interface are quickly emitted into the CB, however, DIGS located deeper in the dielectric remain populated due to slower tunneling-controlled emission process. The negative DIGS charge remains stored a sufficiently long time in respect to the V_G sweeping rate, which can explain unexpected CV hysteresis in the spill-over regime (discussed in more detail in Section 2.3.1).

2.2.3. Dielectric Bulk Traps and 'Border' Traps

Dielectric bulk (or more often oxide) traps (OT) are the defect states in the dielectric band gap that are able to change the charge state due to tunneling of carriers from the electrodes, i.e., semiconductor CB/VB and the gate metal. They are responsible for leakage current degradation and breakdown as well as V_{TH} instabilities in MISHEMTs and MISFETs. For oxide gate dielectrics, OTs are commonly associated with oxygen vacancies (V_O), being a prevalent native defect in thin oxide films deposited on semiconductors [92]. It has been predicted theoretically that V_O point defect and C impurity in Al₂O₃ and HfO₂ show several charge states in contact with GaN and can therefore act as effective trapping states for both, electrons and holes [93,94]. Indeed, OT trapping has been suggested to affect BTI in GaN MISHEMTs [16,95] and plays a major role in BTI of MISHFETs, as will be discussed in more detail in Sections 3 and 4.

In a simple approach, OT with relatively low density can be modelled as a single defect levels E_T distributed in the dielectric with activation energy given by transition between the E_T and the CB/VB. However, a more complex defect configurations can exist in amorphous dielectric layers. A detailed

analysis of PBTI behavior in GaN MISFETs with SiN_x and Al₂O₃ dielectrics observed by Wu et al. [27] was found to be well modeled by using the Gaussian distribution of OT in the form

$$D_{OT}(E, x) = \frac{D_{OT0}}{\sigma_t \sqrt{2\pi}} \exp\left(-\frac{E - \mu_t(x)}{2\sigma_t^2}\right) \quad (5)$$

where E is the energy within the dielectric band gap, x is the spatial position inside the dielectric layer, D_{OT0} is the peak OT density, μ_t and σ_t are the mean and the standard deviations of the Gaussian distributions. The dependence of μ_t on x , having a form of exponential decay $\exp(-x/x_0)$, translates the tunneling into the energy distribution effect. Such OT band models are exemplified in Figure 3a for SiN/GaN and Al₂O₃/GaN MISHFETs together with corresponding OT energy distributions [27]. Note that apart from mean energy position μ_t , also spread of the distribution σ_t affect the resulting PBTI, determining the accessibility of electrons from the GaN conduction band for trapping/de-trapping process at positive V_G . This empirical model can effectively describe the observed power-law dependence of V_{TH} transients on voltage and temperature during both stress and recovery periods upon PBTI [27]. Furthermore, OT band model has been shown to be effective also in description of PBTI and NBTI in GaN MISHFETs [28]. NBTI for both MISHEMTs and MISHFETs can be also affected by injection of electrons from the metal electrode into OT at the metal/dielectric interface, leading to positive V_{TH} shift under negative bias stress [16].

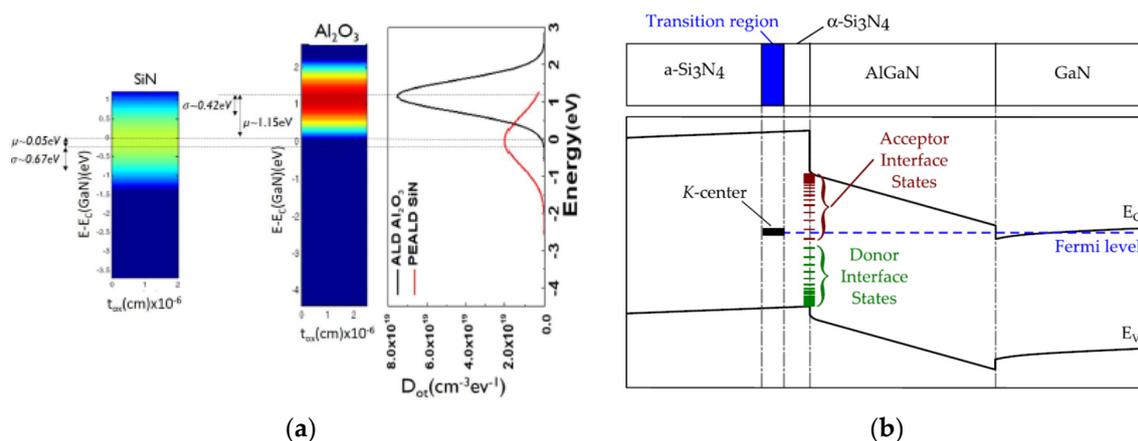


Figure 3. (a) Oxide trap (OT) defect band models in the SiN_x/Al₂O₃ gate dielectric (left) and the energy distribution of the gate dielectric defects for to two different gate dielectrics (right). Copyright © 2020 IEEE. Reprinted, with permission, from Ref. [27]. (b) BT model for the Fermi level pinning due to K-centers inside the silicon nitride. At the Si₃N₄/(Al)GaN interface, a U-shaped distribution of IT and one discrete donor level (BT). Copyright © 2020 AIP. Reprinted from [34], with permission from AIP.

Border traps (BTs, also called near-interface OT or slow traps) represent a special case of oxide traps, physically separated from the interface with the semiconductor. BTs, therefore, exchange the charge only with the semiconductor and with a much slower rate than IT. The physical separation of BTs can be provided by an ultra-thin (comparable to tunneling distance of the electrons) high-quality dielectric in contact with the semiconductor. The presence of a BT has been suggested by Bakeroot et al. [34], who studied 2DEG origin in GaN MISHEMTs with in-situ grown SiN dielectric. BT were proposed to form at the transition between a thin nanocrystalline and amorphous SiN layers depicted in the band diagram shown in Figure 3b. These BTs are assumed to originate from Si dangling bonds also called K-centers [96], energetically located in the middle of the band gap. Trapping/de-trapping processes associated with BT are dominantly affected by tunneling effects with weak temperature dependence and thus show some distinct features as compared to those related to IT and OT. Special distinction between BT and IT trapping/de-trapping can be observed from the measurement of CV hysteresis. While IT lead to typical stretch-out of the CV characteristics when Fermi level is moving close to

semiconductor conduction band, signature of BT effect is manifested by increased hysteresis without apparent CV stretch-out. An example of such behavior has been identified by Zhu et al. [97] in Al₂O₃/AlGaIn/GaN MISHEMTs.

2.2.4. Effects of Trapping Dynamics

The models discussed above can describe IT and OT occupancy at a given time instant and statistically consider Coulombic potential of the trapping states described by the value of capture cross-section. However, they do not account for effects originating from kinetics of the capture and emission processes, recently reviewed by Ostermaier et al. [23]. These effects can be explained in terms of non-radiative multi-phonon (NMP) relaxation model introduced by Henry and Lang [98] as well as cascade mechanism proposed by Lax [99] developed for IT at the SiO₂/Si interface. Change of the defect charge state leads to change of its atomic arrangement, referred to as lattice relaxation. According to the NMP model, an electron in the conduction band needs to overcome a potential barrier E_b (by acquiring vibrational energy from the lattice) in order to be captured by an empty defect. E_b is defined as the energy barrier between total electronic energy for the initial state before capture and the final state after capture. This means that capture process is also temperature activated, leading to temperature-dependent $\sigma = \sigma_0 \exp(-E_b/k_B T)$. For emission process, the electron needs to overcome the energy barrier given by $\Delta E_T + E_b$. The validity of the lattice relaxation model for dielectric/III-N interfaces has been supported by analyzing the capture cross-section of IT in MISHEMT structures with different dielectrics and barrier compositions reported by Matys et al. [18]. The observed increase in σ (ranging from 10^{-19} to 10^{-16} cm⁻²) with the barrier lattice mismatch to GaN channel has been explained by NMP as well as cascade model. Such behavior was attributed to stronger lattice distortion at the dielectric/barrier interface due to larger strain in the barrier [18].

Multi-charge state of defects also affects the capture-emission dynamics [23]. As an example, let us assume a defect with two stable configurations after capturing one or two electrons, corresponding to states 1 and 2, respectively. Following the NMP model, in transition of the defect from state 2 to state 1 (representing electron emission), an electron needs to overcome the barrier given by the crossing point of the total electronic energy for state 2 and state 1, ΔE_{2-1} . For transfer of defect from state 1 to unoccupied state (also representing electron emission), an electron needs to overcome the barrier of $\Delta E_T + E_b$ discussed in the previous paragraph. The electron emission process from the same defect then provides two activation energies. Furthermore, the applied electric field in the oxide alter the transition barrier for both processes, leading to voltage dependent response of the emission processes. These effects are referred to as second order dynamics effect [23] and has been intensively studied for the SiO₂/Si interface [100,101]. Presence of multi-charge state IT in GaN MISHFET structure has been recently suggested by Taoka et al. [102]. The authors analyzed capture cross-section of IT in Al₂O₃/GaN MOS structures and observed much lower values of σ (in the range of 10^{-17} – 10^{-19} cm²) compared to that for SiO₂/Si interface (10^{-16} – 10^{-15} cm²), which was attributed to existence of multi-charge state nature of IT at the Al₂O₃/GaN interface [102].

2.2.5. Pictorial View of V_{TH} Instabilities in GaN MISHEMTs

Before we review recent BTI studies of GaN MISHEMTs, it is useful to outline the processes responsible for V_{TH} instabilities in these devices. Figure 4a–c depict the band diagram across the gate structure in the equilibrium (a) and under application of positive and negative V_G (b–c). In this simplified picture, only IT and OT are considered. We note that despite distinct differences, trapping/de-trapping mechanisms of OT, dielectric DIGS and BT share a common feature of tunneling effects affecting the traps occupancy. Further, trapping states in the III-N epitaxial layer are neglected. As depicted in the band diagram shown in Figure 4a, all traps below the Fermi level are occupied in the equilibrium. When certain positive bias is applied to the gate (referred in the following to as $V_{G,spill}$) in PBTI test, electrons from the channel “spill-over” into the barrier conduction band (Figure 4b). These free electrons are captured by empty IT and also by OT, when OT energy level or energy band

become aligned with the barrier CB edge (Figure 4b). As a result, V_{TH} shifts into positive direction regardless of the traps' nature (i.e., donor- or acceptor-like traps). The stress-induced V_{TH} drift can be monitored electrical techniques described in the next section, giving the information on the electron capture by IT and OT. After stressing period, the recovery of the device biased at $V_{GS} = 0$ typically shows negative V_{TH} shift eventually approaching its pre-stressing value. The V_{TH} recovery transients acquired for different positive stressing bias and temperatures can be then used to characterize the trap emission kinetics [20].

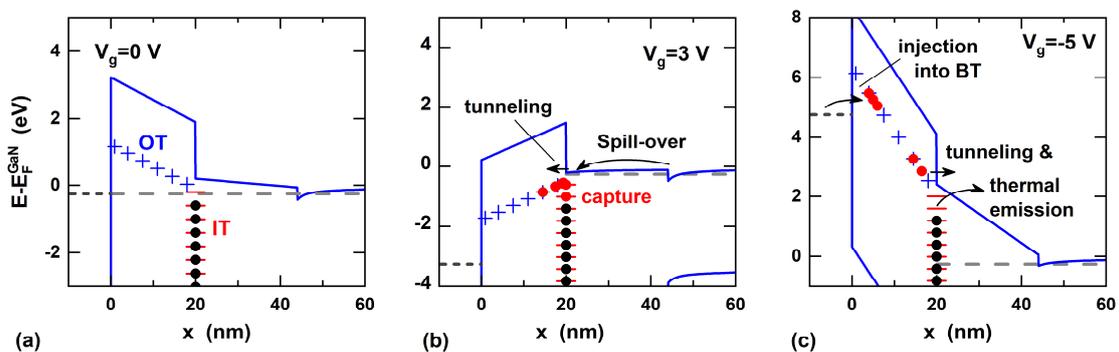


Figure 4. (a) Schematic cross-sectional band diagrams of MISHEMT under the gate showing an example of dielectric/barrier interface traps (ITs) and oxide traps (OTs) distributed in the dielectric layer in thermal equilibrium (a) and under positive (b) and negative (c) V_G applied and possible capture and emission processes inducing different V_{TH} shifts (b,c).

In typical NBTI test, negative V_{GS} is applied on the gate and stress-induced V_{TH} shift is monitored. Band diagram under negative V_{GS} is depicted in Figure 4c. Most commonly, NBTI results in negative drift of V_{TH} , which is attributed to field-enhanced electron emission from both, IT and OT located close to the dielectric/barrier interface. Similar to recovery process after PBTI, stress-induced V_{TH} shift at different stressing voltages and temperatures is used to characterize NBTI kinetics. In addition, if the OT level or band coincide with the metal Fermi level, electrons from the metal can be injected into OT, giving rise to a positive V_{TH} drift (Figure 4c). Metal electrons injection counteracts the V_{TH} drift induced by electron emission from IT and OT localized close to the interface [16]. Due to electrostatics, this effect has much weaker impact on the V_{TH} shift as compared to IT and OT capture/emission, yet, the coaction of processes depicted in Figure 4c has been reported to result in negligible apparent GaN MIS capacitor CV hysteresis at elevated temperatures [16].

Due to extremely wide range of trap time constants in GaN devices, it is practically difficult to achieve trap occupation corresponding to thermal equilibrium (such as that depicted in Figure 4a) for repetitive BTI testing. For NBTI in particular, pre-stress trap occupation has a strong impact on the resulting V_{TH} instability, as the V_{TH} drift measured on virgin sample can largely differ from that of the successive measurement. It is therefore important to establish a reference condition before any BTI investigation. Commonly used approach is the application of some de-trapping step either by application of low negative V_G stress [103] or light exposure (microscope of UV light) of the sample [28] followed by resting the sample in unbiased condition for sufficient time. The sample bake-out at 100–150 °C for 30 min is also very effective pre-testing procedure [19].

2.3. BTI Measurement Techniques

BTI evaluation can be performed using different testing methods. The simplest PBTI test represents the measurement of double-sweep $I_D - V_{GS}$ characteristics of transistor or CV traces of large-area MIS capacitor with increasing positive gate bias, where V_{TH} hysteresis between forward and reverse sweep is evaluated. While the former characteristics are commonly performed for initial screening of the V_{TH} instability, CV measurements have been also used for deeper study of traps distribution in MISHEMT gate stacks [41,89,97]. For a more comprehensive investigation of BTI behavior in GaN transistors,

a variety of stress-measure techniques has been employed. Here, positive/negative V_{GS} is applied during stressing period, which is typically followed by recovery period ($V_{GS} = 0$). During both periods, device parameters such as V_{TH} , g_m , and R_{ON} are monitored via short sampling or measurement sequences interrupting the stressing/recovery [20,28,75]. These techniques provide a comprehensive information on capture and emission kinetics of the device. Standard tests such as high temperature gate bias (HTGB) and high temperature reverse bias (HTRB), stressing the device at negative V_G and in the OFF state, have been also employed for NBTI investigation of GaN MISHEMTs [104,105]. In addition, novel NBTI test conditions tailored for GaN switching devices were developed, including High Temperature Source Current (HTSC) with semi-ON state applied during stressing period [105] and ON/OFF switching stressing [106]. Due to their importance in deeper analysis of BTI mechanisms, in the following, we will discuss some aspects of the CV hysteresis measurements of GaN MISHEMT structures and stress-measure techniques used for BTI investigation in the literature.

2.3.1. Capacitance Techniques

Despite its simple implementation, the main advantage of the capacitance techniques is that they offer straightforward information on the dynamic of charge distribution in the gate structure. When applied to large-area test diode structure, they are insensitive to parasitic surface and thermal effects compared to transistor IV measurements, reducing the data interpretation into essentially 1D problem. On the other hand, capacitance meters generally offer slower reaction time compared to current measurements (unless dedicated fast meters employed, e.g., for DLTS are used) and accuracy of capacitance measurement is limited by the onset of excessive gate leakage current. In the simplest approach, PBTI can be evaluated from double-sweep CV measurement exemplified in Figure 5 for $Al_2O_3/AlGaIn/GaN$ MIS heterostructure [107]. Typically, V_G is swept from negative to positive voltages in forward direction and backward in the reverse direction for given temperature. From set of the CV sweeps performed for increased maximum positive V_G ($V_{G,max}$), CV hysteresis at 2DEG depletion part (ΔV_{TH}) is extracted. For high-quality gate oxides, also CV hysteresis ($\Delta V_{G,spill}$) and stretch-out in the spill-over region can be evaluated [107]. Note the higher $\Delta V_{G,spill}$ compared to ΔV_{TH} . This is caused by partial emission of IT and/or OT populated at positive V_G during the subsequent backward sweep. Traps with shorter τ_E than the time it takes to sweep the V_G from $V_{G,max}$ to V_{TH} therefore do not contribute to apparent ΔV_{TH} [41]. In addition to a strong dependence on $V_{G,max}$, resulting ΔV_{TH} also depends on the V_G sweep rate [89]. If present, $\Delta V_{G,spill}$ is also strong function of measurement signal frequency [15,108,109] and temperature [17].

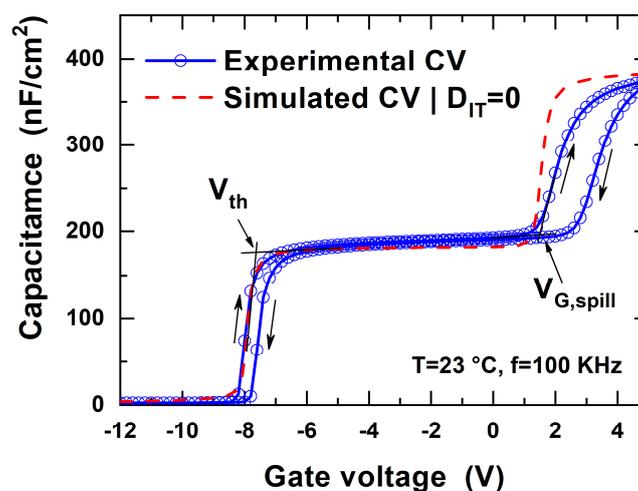


Figure 5. Example of double-sweep CV characteristic measured on large-area $Al_2O_3/AlGaIn/GaN$ MISHEMT structure together with the “ideal” CV curve, calculated using Poisson solver.

Theoretical and experimental study of D-mode Al₂O₃/AlGa_{0.3}N/GaN MISH structures using CV hysteresis measurements was performed by Matys et al. [89]. The authors observed gradual increase in both ΔV_{th} and $\Delta V_{G,spill}$ with $V_{G,max}$ increasing that further increased with lowering of the sweep rate. In addition, lower sweep rate resulted in stronger stretch-out of the CV curve in the spill-over regime. However, shallower IT available for capture/emission in D-mode MISHEMT are expected to result in negligible $\Delta V_{G,spill}$ as well as ΔV_{TH} with $V_{G,max}$ increasing [107]. Instead, the authors proposed the presence of DIGS in the Al₂O₃ dielectric described in Section 2.2.2 (Equations (3) and (4)). Assuming $N_0 = 8 \times 10^{17} \text{ eV}^{-1}\text{cm}^{-3}$, $x_l = 4 \text{ nm}$, and $\sigma_0 = 10^{-15} \text{ cm}^{-2}$, calculated results were able to reproduce complex PBTI as well as NBTI behavior observed experimentally [89]. Somewhat different CV hysteresis behaviors of D-mode Al₂O₃/AlGa_{0.3}N/GaN MISH structures subjected to PBTI were observed by Zhu et al. [97]. Here, increasing of $V_{G,max}$ resulted in gradual increase of ΔV_{th} and $\Delta V_{G,spill}$, which was also accompanied with positive shift of V_{TH} , i.e., rigid right-shift of the CV curve along the V_G axis. Such behavior was attributed to dominant BT capture/emission process (described in Section 2.2.3) enhanced by IT trapping. Despite some controversy, these results suggest that traps located in the oxide close to the dielectric/barrier interface play a vital role for PBTI behavior of GaN MISHEMTs. It also demonstrates that simple CV hysteresis measurement can provide detail information on the BTI processes, complementing the IV measurements of transistors.

In the CV hysteresis measurement, availability of empty traps (located above the Fermi level in the equilibrium) plays a critical role for resulting ΔV_{th} . As discussed in Section 2.1, band bending at the dielectric/barrier interface $\Phi_{interface}$ is given by the amount of P_S compensation. For the practical comparison between the MISHEMTs, it is more appropriate to define the net interface charge $Q_{interface} = P_S + Q_{comp} + qN_{IT}$ (N_{IT} is the effective interface trapped charge), which can be extracted from the slope of $V_{TH} = f(t^{dielectric})$ [16,39]. The effect of $Q_{interface}$ on the CV hysteresis was analyzed for Al₂O₃/AlGa_{0.3}N/GaN large-area MISHEMT capacitors with nominally same heterostructures but different $Q_{interface}/q$ of -1×10^{13} and $1 \times 10^{12} \text{ cm}^{-2}$ resulting from different oxide PDA [41]. Despite relatively high D_{it} ($\sim 10^{12} \text{ eV}^{-1}\text{cm}^{-2}\text{eV}$) determined for both structures, devices with PDA ($Q_{interface}/q = 10^{12} \text{ cm}^{-2}$) showed negligible CV hysteresis with increasing $V_{G,max}$ (Figure 6b), while significant and enhanced CV hysteresis with increased $V_{G,max}$ was observed for structures without PDA ($Q_{int}/q = -1 \times 10^{13} \text{ cm}^{-2}$). Negligible ΔV_{TH} for structures with PDA can be explained by fast emission of shallower IT populated at forward V_G bias (see corresponding band diagram in Figure 6a) during the backward sweep, resulting in similar IT population at $V_G \sim V_{th}$ for forward and backward sweep. In contrast, electrons are captured by much deeper empty IT available in the structure without PDA (see Figure 6a) at positive V_G . This is then followed by slower IT emission during the backward sweep, thus higher negative charge stored in IT after backward measurement compared to the equilibrium. This behavior illustrates that MISHEMTs with similar interface quality but different $Q_{interface}$ can show different CV hysteresis.

Finally, it is also possible to monitor NBTI in D-mode MISHEMT structures (or PBTI in E-mode MISHEMT structures) using capacitance transient ($C-t$) measurements [54,110]. In this technique, transient V_{TH} drift is deduced from the $C-t$ measurement performed at V_G bias corresponding to depletion part of the CV curve (e.g., at $V_G = V_{TH} - 0.3 \text{ V}$), giving the highest sensitivity for V_{TH} shift. After optional pre-filling of the traps at positive V_G , the measured C transient is recalculated to V_{TH} transient using corresponding part of the CV curve [54,110]. The disadvantage of this technique for BTI investigation is the fundamental limitation of the stressing voltage selection and above mentioned relatively low reaction time of the capacitance measurement.

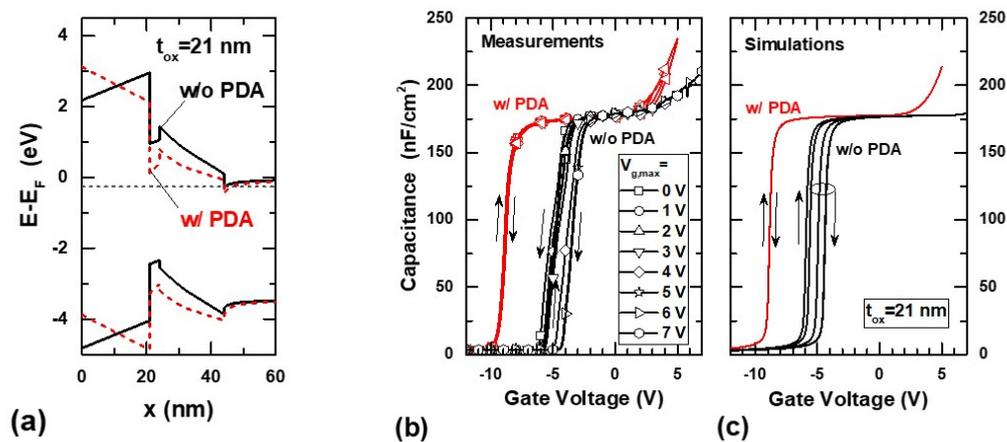


Figure 6. (a). Band diagrams of MISHEMT structures calculated using Poisson equation and assuming $Q_{interface}/q$ of -1×10^{13} (w/o PDA) and $1 \times 10^{12} \text{ cm}^{-2}$ (w/PDA). Experimental (b) and simulated (c) CV hysteresis of MISHEMT structures without and with PDA measured using different maximum V_G ranging from 0 to 7 V. Reprinted from [41], with permission from Elsevier. Copyright © 2020 Elsevier.

2.3.2. Stress-Measure IV and Pulsed I_D Techniques

Stress-measure techniques are based on monitoring of the device parameters during stressing and recovery period. The monitoring is performed by repeated interruptions of the stressing/recovery bias, during which fast DC I_D - V_{GS} , I_D - V_{DS} [21,28,104,105] or pulsed I_D [22,33,111] are measured. While the DC measurements offer detail monitoring of the change in device parameters in time (V_{TH} , R_{ON} , and g_m), pulsed I_D measurement provide only information of V_{TH} drift. On the other hand, short response time of the pulsed measurement, referred to as measure-stress-measure (MSM) technique in the literature [23], allows one to monitor capture and emission processes with sub- μs resolution, which is of particular importance in the study of trapping dynamics. Yet, some change of the trap's occupation induced during the measure period cannot be avoided and needs to be carefully considered in the design of the BTI experiments [23]. Since MSM technique has been recently employed for BTI study in MISHEMTs by several groups [22,24,25], it will be described in more detail in the next paragraph. Many researchers have also employed double-channel pulsed measurement of I_D - V_{GS} characteristics for PBTI assessment [24,75]. Here, quiescent gate bias represents the stressing V_G magnitude while the I_D - V_{GS} characteristics measured at low V_{DS} provide information on the V_{TH} drift and possible g_m change.

The MSM technique monitors V_{TH} drift using an oscilloscope base setup depicted in Figure 7a. In the measurement sequence (Figure 7b), device under test is first stressed at forward gate bias $V_{G,stress}$ for time period t_{stress} ($V_{DS} = 0 \text{ V}$). Then, V_G is stepped to zero ($V_{DS} = 0 \text{ V}$) and the device recovery is monitored by measurement of V_D in short moments at certain time intervals (t_{rec}) and small $V_{D,meas}$. V_{TH} drift (ΔV_{TH}) is evaluated from the transient response of V_D in respect to the virgin transfer characteristic. ΔV_{TH} can be measured for constant $V_{G,stress}$ and logarithmically increased t_{stress} or using increased $V_{G,stress}$ and constant t_{stress} . This technique allows evaluation of V_{TH} drift transients for a wide range of stressing and recovery times, as exemplified in Figure 7c,d, where V_{TH} recovery drifts for t_{stress} of 100 ns and 100 s as a function of $V_{G,stress}$ are shown. It is best suited for D-mode MISHEMTs, where stressing and measurement takes place at positive and negative V_G ($V_{TH} < V_{G,meas} < 0$), respectively. MSM technique has been also implemented by using sampling-mode DC measurements performed by, e.g., standard Keithley 4200 system [20,24,25]. Although such instruments provide much longer response time ($\sim 10 \text{ ms}$) compared to pulsed measurements ($\sim 100 \text{ ns}$), versatility of these measurement systems extends implementation of MSM technique for E-mode devices [25], application of advanced stressing conditions [105], and detailed device characterization during and immediately after the stressing [20].

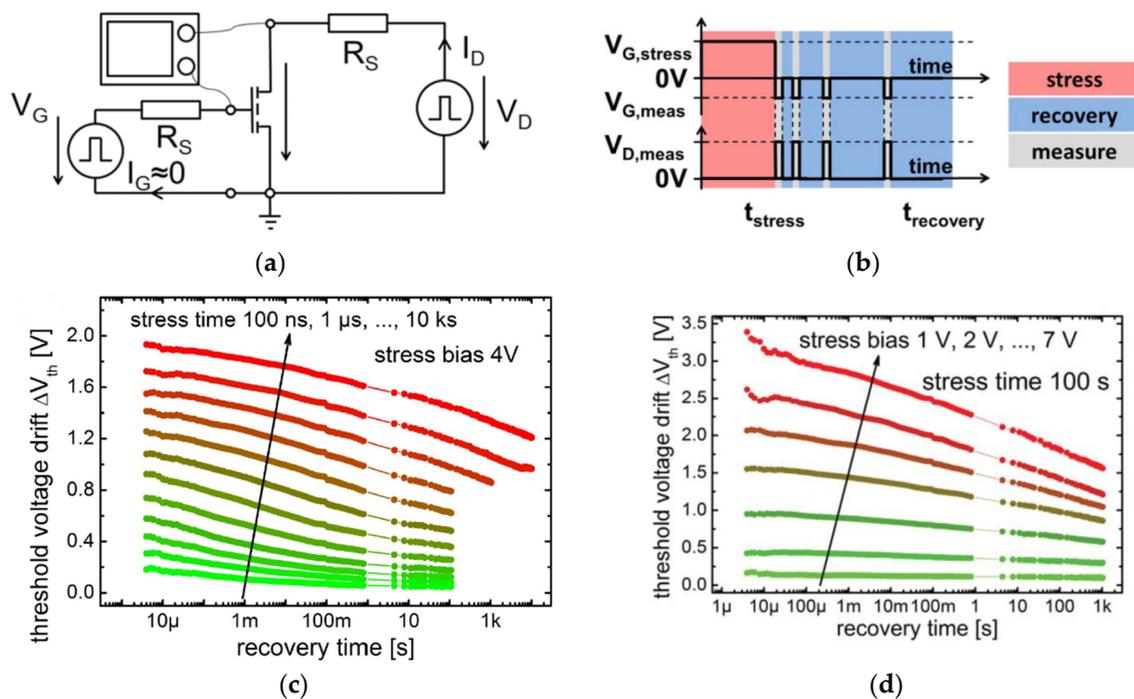


Figure 7. Measurement setup (a) and pulse pattern (b) used for stress-recovery cycle of measure-stress-measure (MSM) technique. To measure the transient response of V_D , the biases are pulsed to $V_G = V_{G,meas}$ and $V_D = V_{D,meas}$. (c,d) Example of recovery transients measured for constant $V_{G,stress} = 4$ V and varying stress times ranging from 100 ns to 100 ks (c) and for constant t_{stress} of 100 s while varying $V_{G,stress}$ from 1 to 7 V (d). Reprinted from Ref. [22], with permission from IEEE. Copyright © 2020 IEEE.

3. BTI in GaN MISHEMTs

Majority of BTI studies in GaN MISHEMTs are focused on PBTI of D-mode devices. This is because of great advancements achieved in the technology of non-recessed or partially recessed AlGaIn/GaN MISHEMT switching devices. These studies allowed for deeper analysis of the V_{TH} drift mechanisms under positive bias stress, even though such devices are not expected to operate at such conditions. In fact, only a limited number of studies investigating PBTI in E-mode GaN MISHEMTs are available in the literature, which is simply because only a few design concepts of non-recessed E-mode MISHEMTs are available [13,14,43,45,46]. On the other hand, NBTI represents a major concern in the D-mode GaN MISHEMTs used, e.g., in the cascade configuration. However, due to availability of reliable and stable SB HEMTs, less interest has been given to NBTI investigations in D-mode GaN MISHEMTs. We will therefore review the most relevant research works aiming for a deeper understanding of the PBTI mechanisms in D- and E-mode GaN MISHEMTs and NBTI in D-mode MISHEMTs.

3.1. PBTI in D-Mode GaN MISHEMTs

Among the first, Lagger et al. [20] studied PBTI in D-mode $Al_2O_3/AlGaIn/GaN$ MISHEMTs using MSM technique for monitoring of V_{TH} drifts upon positive bias stress and recovery. In their later research [22], extended MSM technique (improved by using an oscilloscope-based measurement) was employed to study PBTI in D-mode $SiO_2/AlGaIn/GaN$ MISHEMTs. Measured ΔV_{TH} drift in an extremely broad range of recovery times is exemplified in Figure 7c,d for different t_{stress} and $V_{G,stress}$. For the data interpretation, the authors considered any defects in the active energy region of the gate stack capable to exchange the charge with 2DEG, without explicit discrimination between IT and OT. The measured ΔV_{TH} is then related to change of “interface” traps occupation (ΔN_{IT}) as $\Delta N_{IT} = -C_{OX}(\Delta V_{TH}/q)$. Instead of calculating D_{IT} distribution or density of OT, ΔN_{IT} is interpreted

using concept of capture emission time (CET) map, as originally proposed for analysis of NBTI in Si MOSFETs [112]. Figure 8a shows a CET map calculated from the recovery data shown in Figure 7c. Here, all trap states are described by their ΔV_{TH} (ΔN_{IT}) per decade in 3-dimensional space of corresponding capture and emission time constants, for given $V_{G, stress}$ and temperature [22]. In the case of capture/emission of an electron from/to semiconductor CB with corresponding lattice relaxation, the CET map should comprise only positive entries. However, note that CET map shown in Figure 8a includes also negative values that correspond to decrease in ΔN_{IT} with t_{stress} increasing, even though it first increases with t_{stress} from the beginning of the recovery process. The decrease in N_{IT} with increasing of t_{stress} was attributed to second order dynamics effects discussed in Section 2.2.4.

Due to existing barrier between 2DEG and IT, trap dynamic is also affected by electron transport through the barrier layer itself. This was pointed out by Ostermaier et al. [113], who investigated V_{TH} drift of MISHEMTs with SiN gate dielectric subjected to positive bias stress at different temperatures. It was observed that the onset of positive V_{TH} drift starts at longer t_{stress} as the $V_{G, stress}$ decreases. From the thermal activation of this V_{TH} onset, E_A was found to increase linearly with $V_{G, stress}$ decreasing down to $V_{G, stress} = 1$ V. Beyond this bias, E_A remained constant at a value of ~ 0.52 eV [113]. Such behavior was explained by IT capture via trap-assisted tunneling of electrons from the barrier across the triangular CB edge near the interface. This suggests that effective IT capture represents a serial process, characterized by the sum of actual defect τ_C and the time constant related to the transport process through the barrier.

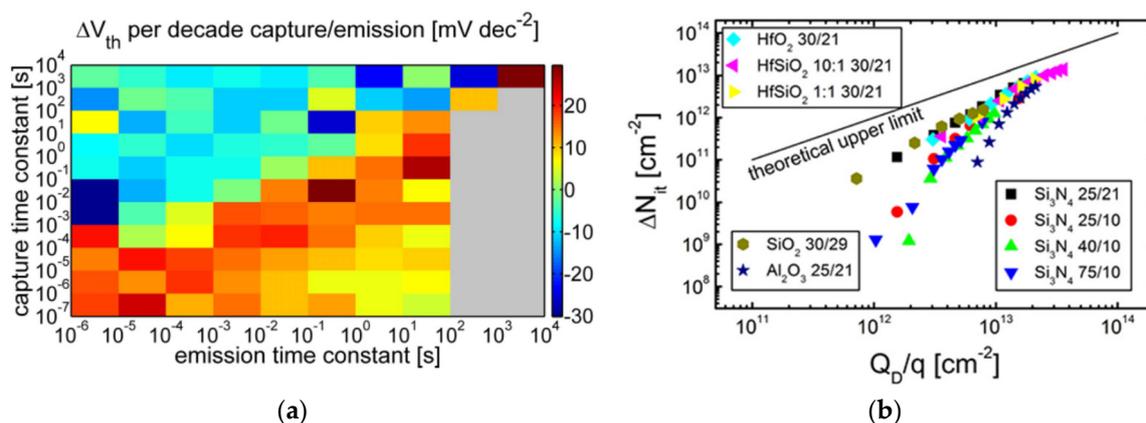


Figure 8. (a) Capture emission time (CET) map extracted from the recovery transients exemplified in Figure 7 (c,d). © 2020 IEEE. Reprinted, with permission, from Ref. [22]. (b) Measured dependence of ΔN_{IT} on the dielectric charge Q_D/q . The deviation from linear dependence between the different samples originates from the variation in $V_{G, spill}$. Reprinted from Ref. [114], with a permission of AIP Publishing. Copyright © 2020 AIP.

MSM technique in conjunction with CET map data analysis was used to study MISHEMTs with various dielectric materials [114]. Although different gate materials resulted in different ΔV_{TH} for given t_{stress} , the authors pointed out that also gate electrostatics, affecting availability of free electrons for capture, need to be considered in such comparison. This is demonstrated in Figure 8b showing the dependence of ΔN_{IT} on the gate displacement charge ($Q_D = C_D \times V_G$, C_D is the dielectric capacitance), which converges towards the same dependence for all dielectric materials, reaching its upper limit $\Delta N_{IT} = Q_D$ [114]. Note that higher the C_D , the more charges are accumulated at the interface for given positive V_G . The linear dependence of ΔN_{it} on Q_D/q without apparent saturation observed for $V_G > V_{G, spill}$ in all dielectrics studied in [114] indicates that a higher density of traps (IT and OT) is available than the number of free electrons present in the reservoir, i.e., 2DEG in bare AlGaIn/GaN heterojunction. A similar situation was concluded also in the study of Winzer et al. [111], investigating PBTi in D-mode MISHEMTs with Al₂O₃ and HfO₂ gate dielectrics with similar C_D . Here, ΔN_{IT} as high as $\sim 10^{13}$ cm⁻² was determined from positive bias stress at $V_G > V_{G, spill}$ for both devices. However, 2DEG concentration of 8×10^{12} cm⁻² was determined by the Hall measurements of the AlGaIn/GaN

heterostructure. As a consequence, such high density of interface traps limits their evaluation by electrical methods. Further, when an MISHEMT is driven into spill-over regime, voltage drop across the barrier remains unchanged with further V_G increasing. Additional increase in V_G results in voltage drop solely across the dielectric and is limited by the dielectric critical breakdown field. Ostermaier et al. [23] applied these two limitations for definition of the practical lifetime requirements for E-mode MISHEMTs. First, sufficiently low ΔV_{TH} assuring maximum specified R_{ON} and the minimum specified I_D at the end-of-life must be fulfilled at the operating V_G . Second, the stability of the gate dielectric must be assured at maximum V_G at end-of-life. Using the experimental values of critical electric field of commonly applied dielectrics, maximum ΔN_{it} was estimated to be in the range of $4\text{--}8 \times 10^{12} \text{ cm}^{-2}$ for typical 2DEG sheet channel density of $0.5\text{--}1 \times 10^{12} \text{ cm}^{-2}$ [23].

The effect of the gate dielectric growth method on PBTI was also studied by Meneghesso et al. [75], who reported comprehensive reliability investigation of partially recessed barrier MISHEMTs with SiN gate dielectric grown by rapid thermal CVD (RTCVD) and plasma-enhanced ALD (PEALD). As deduced from the pulsed I_D - V_{GS} and MSM measurement, MISHEMTs with PEALD dielectric showed notably lower V_{TH} drift with resulting ΔN_{IT} of $\sim 3.5 \times 10^{11} \text{ cm}^{-2}$ (for $t_{stress} = 1000 \text{ s}$) compared to devices with RTCVD dielectric showing ΔN_{IT} of $\sim 2 \times 10^{12} \text{ cm}^{-2}$. Interestingly, the recovery times for both devices exceeded 1000 s for $V_{G, stress} = 2.5 \text{ V}$. V_{TH} drift was found to correlate with the gate leakage current at positive gate voltages, indicating that bulk OTs, which are likely to govern the gate leakage mechanism, are also responsible for V_{TH} drift upon positive stressing bias. In addition, the gate robustness under forward bias was examined using step-stress and time-dependent dielectric breakdown (TDDB) measurements [75]. Improved gate robustness of PEALD grown SiN gate dielectric as compared to RTCVD SiN has been attributed to lower OT density in this dielectric due to lower probability of the percolation leakage path formation. These results highlight the importance of the gate dielectric technology, as non-optimal growth conditions leading to higher density of OT can result in inferior device reliability in terms of V_{TH} stability as well as gate robustness.

Due to presence of different defects in the gate stack and variability of their capture/emission dynamics affected also by the transport through the barrier discussed above, it is generally challenging to discriminate, which defects dominantly affects the PBTI behavior in MISHEMTs. Yet, detailed analysis of the V_{TH} drift induced by forward bias stress and/or subsequent recovery can provide indications on the nature of the relevant defects. Among others, Zhang et al. [24] investigated PBTI in MISHEMTs with PECVD grown SiN gate dielectric using step stress-recovery experiment. The capture process was found to follow a two-step trapping process with fast electron trapping (with time constant below 100 ms) followed by a slow dynamic, featuring a logarithmic time-dependent V_{TH} drift. The fast capture process was attributed to IT capture, while the slow capture process was proposed to result from population of OT located close to the interface. Alternatively, the authors considered the importance of the electrostatic feedback effect, where electron capture rises the barrier potential leading to the decrease of the gate current and thus availability of free electrons. In the study of Wu et al. [103], V_{TH} recovery after forward bias stressing at different temperatures was monitored via fast DC I_D - V_{GS} measurement in AlGaIn/GaN MISHEMTs with ALD Al_2O_3 /in-situ SiN gate dielectric. The derivative of V_{TH} transients revealed distinct peaks, which indicates the presence of discrete traps level. The trap level E_A of 0.69–0.7 eV was determined and ascribed to donor-like $\text{Si}_3\text{N}_4/\text{AlGaIn}$ IT level. Although the presented results seem to be controversial, they highlight the importance of the gate dielectric technology on the defect nature and density. While the MOCVD grown in-situ SiN is expected to provide high-quality interface with the AlGaIn barrier, SiN deposited by PECVD may be expected to result in the gate stack with relatively higher IT density as well as bulk OT.

3.2. PBTI in E-Mode MISHEMTs

As discussed in Section 2.1, E-mode operation of GaN MISHEMTs can be achieved, e.g., by the barrier fluorination [14] or polarization engineering approach [13]. Investigation of PBTI in E-mode MISHEMTs with fluorination approach was performed by Wu et al. [115]. Under gate bias stress

performed at different positive V_{GS} (4–6 V) and temperatures (30–150 °C) for t_{stress} of 10 ks, the authors observed positive V_{TH} shift up to 1 V with time evolution, which can be fitted by the empirical power-law dependence [27]

$$\Delta V_{TH} = A_0(V_{GS} - V_{TH})^n t_{stress}^m \quad (6)$$

where A is the pre-factor and n is the time exponent. This behavior will be further discussed in more detail in Section 4.1. Similar results were observed also for devices without fluorination, so that the PBTI was attributed to pre-existing IT and OT, while negligible plasma treatment-induced trap generation was concluded.

Up to now, we have only discussed PBTI behavior with positive/negative V_{TH} drift under stressing/recovery. However, also opposite V_{TH} drift has been reported for E-mode devices with polarization-engineered barrier structure. In our recent study [25], PBTI in $\text{Al}_2\text{O}_3/\text{InGaN}/\text{AlGaIn}/\text{GaIn}$ MISHEMTs was investigated using the MSM technique. In this structure, a high negative polarization charge at the $\text{InGaIn}/\text{AlGaIn}$ interface raises the bands, leading to formation of 2-dimensional hole gas (2DHG) at this interface [13]. Typical MSM measurements are shown in Figure 9a for stress (left, $t_{stress} = 100 \text{ ms} - 50 \text{ s}$) and recovery (right, $t_{rec} = 50 \text{ s}$) period. The devices show negative V_{TH} drift during stress period and positive V_{TH} drift during recovery. Yet, the final V_{TH} transient ends-up at higher value in respect to the beginning of the stressing. Such behavior was explained by the following model (Figure 9b): When positive $V_{G, stress}$ is applied to the gate, electrons accumulated at $\text{AlGaIn}/\text{GaIn}$ interface are injected into the InGaIn layer and recombine with holes in 2DHG, emitting photons with energy of around 3 eV (i.e., the bandgap of the InGaIn). Some of these photons are absorbed by the $\text{Al}_2\text{O}_3/\text{InGaIn}$ interface states and the released electrons can then tunnel through the triangular barrier of the oxide CB edge. The emptied states build up positive charge, which results in negative V_{TH} shift. During recovery, structure tends to return to the equilibrium, however, some holes are depleted from the 2DHG. Therefore, resulting V_{TH} is shifted to more positive values as compared to pre-stress condition.

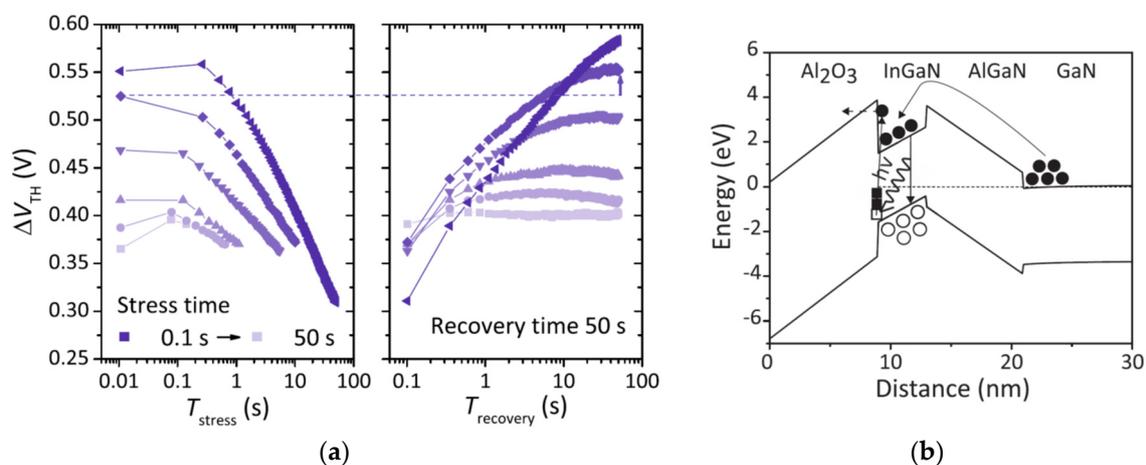


Figure 9. (a) Successive MSM measurement of $\text{Ni}/\text{Al}_2\text{O}_3/\text{InGaIn}/\text{AlGaIn}/\text{GaIn}$ MOS HEMT (stress—left, recovery—right). Measurements start with the shortest stressing time (0.1 s) and continue with increased stressing time. (b) Schematic representation of selected processes during stress. Electrons are injected from 2DEG into InGaIn . Electrons recombine with holes in InGaIn and emit photons that, in turn, de-trap interface states. Emitted electrons from interface states tunnel into conduction band (CB) through triangular barrier. Copyright © 2020 Elsevier. Reprinted, with permission, from Ref. [25].

3.3. NBTI in GaN MISHEMTs

Investigation of NBTI in D-mode MISHEMTs is sparse in the literature. Dalcanale et al. [105] presented an interesting NBTI investigation of GaN MISHEMTs designed to work in a cascode configuration [116]. In addition to the application of high temperature reverse bias (HTRB) testing

protocol with $V_{GS} < V_{TH}$ and V_{DS} biased up to 750 V, the authors defined a novel high temperature source current (HTSC) stressing condition [105]. In this test, the device is stressed in the semi-on state operation so that hot-electrons are generated in the transistor's channel. It was found that no significant V_{TH} drift was observed under HTSC conditions, while HTRB stress results in a strong negative V_{TH} drift. This behavior was ascribed to steady-state population of IT as well as GaN buffer traps by the hot-electrons under HTSC at the drain side of the gate. On the other hand, dominant emission from these traps took place in the case of HTRB with higher V_{GS} .

4. BTI in GaN MISFETs

An often-used approach to process lateral E-mode GaN switching transistor is to fully recess the AlGaN barrier layer under the gate, while existing 2DEG in the source-to-gate and gate-to-drain regions provide a low access resistance. The MIS gate structure of fully recessed GaN devices resembles that of Si MOSFETs and many approaches developed for BTI investigation in Si devices have been adopted also for description of PBTI and NBTI issues of GaN MISFETs. Universal recovery model developed for Si MOSFETs [117] have been widely employed to describe the PBTI [27] as well as NBTI [28] behavior of GaN MISFETs. Although dielectric/GaN IT plays some role, there seems to be a general agreement that dielectric OTs have dominant impact on the PBTI and NBTI mechanism.

4.1. PBTI in GaN MISFETs

Comprehensive analysis of PBTI in fully recessed GaN MISFETs with PEALD SiN and ALD Al₂O₃ gate dielectric was performed by Wu et al. [27]. Due to observed lack of correlation between I_D - V_{GS} hysteresis (thus ΔV_{TH}) and the D_{IT} distribution measured by G - ω method, the authors employed PBTI stress-recovery tests using the MSM technique. It was found that ΔV_{TH} transients for different $V_{G, stress}$ (Figure 10a,b) can be fitted using Eqn. 6 in the whole range of t_{stress} with time exponent n in the range of 0.1–0.02. Despite notably higher D_{IT} , devices with Al₂O₃ showed about 10-times lower ΔV_{TH} compared to those with SiN, when benchmark at $t_{stress} = 2$ s depicted by the black arrows in Figure 10a,b. The voltage exponent γ of 1 and 2 and E_a of 0.57 and 1.02 eV was observed for devices with SiN and Al₂O₃, respectively. The recovery ΔV_{TH} transients obeyed empirical model of universal relaxation [117]

$$\Delta V_{TH}(t_{stress}, t_{relax}) = R(t_{stress}, t_{relax} = 0)r(\xi) + P(t_{stress}) \quad (7)$$

$$r(\xi) = \frac{1}{1 + B\xi^\beta} \quad (8)$$

where R and P represent recoverable and permanent degradation ascribed to different types of defects, t_{relax} is measured from the end of last stress phase, $\xi = t_{relax}/t_{stress}$ is the universal relaxation time, B is the scaling parameter and exponent β represents the dispersion parameter. From the fitting of Equations (7) and (8) to the ΔV_{TH} recovery transients (Figure 10c), devices with Al₂O₃ gate dielectric were found to show lower recoverable and permanent degradation and faster dielectric defect discharge. Such behavior was attributed to presence of OT Gaussian distributions depicted in Figure 3a. In the case of SiN, a wider distribution of OT levels ($\sigma \sim 0.67$ eV), centered below the conduction band of GaN ($E_C - 0.05$ eV) are easily accessible by the channel carriers already at a low $V_{G, stress}$. In contrast, Al₂O₃ gate dielectric was proposed to feature a narrower distribution of OT ($\sigma \sim 0.42$ eV) located far from the conduction band edge of GaN ($E_C + 1.15$ eV), explaining the improved PBTI behavior in devices with ALD grown Al₂O₃ gate dielectric compared to those with SiN.

Dominant impact of dielectric OT on the V_{TH} instabilities has been proposed also by other studies. Bisi et al. [118] studied PBTI stress-recovery kinetics in Al₂O₃/GaN MIS capacitors grown by in-situ MOCVD by means of combined I_G transient, CV and capacitance MSM technique. In the low-field (oxide electric field <3.3 MV/cm) regime, I_G stress and recovery transients were found to obey power-law $I_G(t) \propto t^{-\alpha}$ with $\alpha \sim 1$, suggesting trapping and de-trapping of near-interface OT. In contrast, high-field regime (>3.3 MV/cm) was characterized by the onset of the gate leakage current promoted

by OT and significant positive flat-band voltage (V_{FB}) shift, suggesting enhanced charge trapping of OT, as also revealed by very slow recovery transients [118]. Acurio et al. [119] studied PBTI in a fully recessed-gate MSIFET with PECVD SiO_2 gate dielectric using I_D - V_{GS} measurements interrupting the stressing and recovery. Similar to previous results, power-law dependence of ΔV_{TH} on t_{stress} was observed. Furthermore, trapping rate (evaluated as $\partial \log V_{TH} / \partial \log t$) exhibited a universal decreasing behavior as a function of the number of filled traps. Stress-induced ΔV_{TH} was fully recovered by applying a small negative voltage and the recovery dynamics (monitored in time window between 1 s and thousands of seconds) was found to be well described by the superimposition of two exponential functions. These emission processes were associated with two different OT. The slower trap revealed E_A of 0.93 eV and the faster trap exhibits large spread in E_A ranging from 0.45 eV to 0.82 eV. V_{TH} recovery with two different time constants have been also observed also by Iucolano et al. [120]. By measuring the hysteresis of I_D - V_{GS} characteristics with different $V_{GS,max}$ ($V_{DS} = 0.1$ V), partial V_{TH} recovery was reached after a few seconds, however, a complete V_{TH} recovery required more than one day of unbiased storage. Based on the numerical simulations, the fast and slow recovery processes were associated with the emission from IT and OT localized above the GaN conduction band energy, respectively.

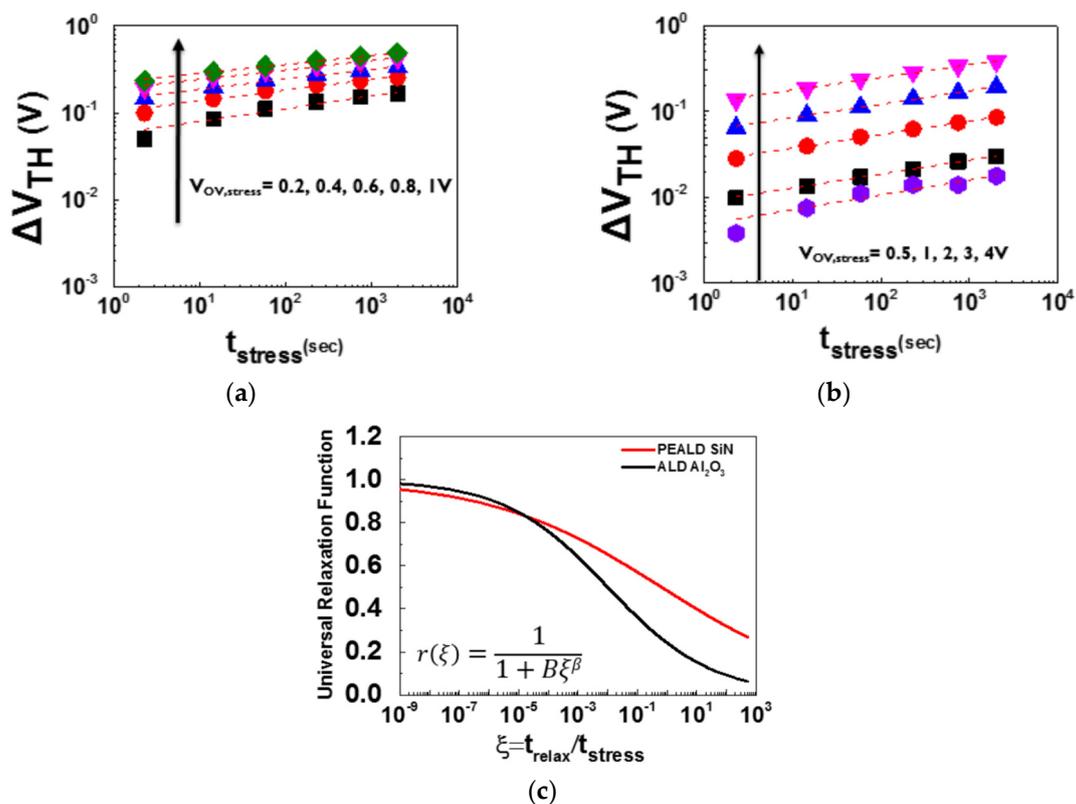


Figure 10. ΔV_{TH} transients for different t_{stress} of fully-recessed MISFETs with (a) plasma-enhanced ALD (PEALD) SiN and (b) ALD Al_2O_3 gate dielectric in a logarithmic–logarithmic scale. Dashed lines represent the power-law fits (Equation (6)) to the data. (c) Recovery transients fitted with the universal relaxation model (Equations (7) and (8)) showing faster relaxation for the device with Al_2O_3 gate dielectric. Copyright © 2020 IEEE. Reprinted, with permission, from Ref. [27].

In fully recess-gate MISFETs, the drain-edge of the gate terminal represent another critical region concerning the BTI, as trapping states formed close to interface between the dielectric and the barrier side-wall can negatively affect V_{TH} as well as R_{ON} stability. In the study of Chini and Iucolano [121], E-mode GaN MISFETs were subjected to PBTI in the switching-mode operation and V_{TH} and R_{ON} drift was monitored simultaneously using special designed pulsed setup [121]. Apart from positive V_{TH} drift related to IT traps under the gate region, also V_{TH} drift linked to a localized trapping in the drain-edge

of the gate terminal was identified. Further, the observed increase in R_{ON} was associated with a hole-emission process taking place in the gate-drain access region within the C-doped buffer layer.

4.2. NBTI in GaN MISFETs

Current understanding of NBTI in E-mode GaN MISFETs is quite limited and some controversy exist in the observed behavior. In one of the first studies, Sang et al. [122] compared V_{TH} drifts under negative V_G stress in the D-mode MISHEMTs and E-mode GaN MISFETs with ALD Al_2O_3 gate dielectric. For the latter, the positive stress-induced V_{TH} shift was observed, which was attributed to metal gate electron injection into OT and following redistribution of the trapped charge towards the GaN channel via trap-assisted tunneling. Later, Guo and del Alamo [19] performed a more detailed investigation of NBTI in $SiO_2/Al_2O_3/GaN$ MISFETs subjected to negative V_{GS} stress with different amplitude, duration, and temperatures. Stress-induced V_{TH} shift was found to progress through three regimes. Under low-stress (low $V_{GS, stress}$, low T , short t_{stress}), ΔV_{TH} was negative and recoverable due to electron de-trapping from pre-existing OT. Under mid-stress (low $V_{GS, stress}$, high T , longer t_{stress}), positive and recoverable ΔV_{TH} was observed, i.e., behavior similar to that reported by Sung et al. [122]. However, the cause of this effect was attributed to electron tunneling from VB to trap states in the GaN channel under the gate edges, also referred to as Zener trapping in the literature [123]. For high-stress ($V_{GS, stress} < -30$ V, RT), non-recoverable negative ΔV_{TH} was observed and ascribed to generation of new IT.

Recently, Guo and del Alamo [28] presented a comprehensive study of BTI in GaN MISFETs under moderate positive and negative gate bias stress ($V_{G, stress} = +5$ and $= 5$ V) using fast I_D - V_{GS} measurements interrupting the stressing. V_{TH} evolution was monitored during the stressing and recovery phase, followed by full recovery of V_{TH} to pre-stress value. For positive $V_{G, stress}$, positive ΔV_{TH} drift was observed, which increased with stressing voltage. Nearly symmetrical behavior with negative V_{TH} drift was observed for NBTI. For both stress conditions, the V_{TH} time evolution was found to follow power-law model (Equation (6)) during the stressing and universal relaxation model (Equations (7) and (8)) during the recovery. Therefore, the authors proposed that NBTI and PBTI are caused by the same mechanism, which is the electron trapping/de-trapping in preexisting OT that form a defect band close to the dielectric/GaN interface [28]. The authors assumed the defect band extending the energies above the GaN CB edge and below the surface Fermi level at $V_{GS} = 0$ V. This means that some trap states are empty while some are populated with electrons at $V_{GS} = 0$ V. During the stress phase, the electron occupation of OT increases or decreases depending on the sign of $V_{G, stress}$, resulting in V_{TH} in positive or negative direction, respectively. In the recovery process, the trap occupation returns to the state corresponding to $V_{GS} = 0$ V.

Apparent positive stress-induced V_{TH} drift under NBTI was observed also in studies of Hua et al. [73,124] and He et al. [125] in E-mode GaN MISFETs with LPCVD- SiN_x /PECVD- SiN_x /GaN gate stack. The PECVD SiN_x interfacial layer (thickness of ~ 2 nm) grown at low temperature was employed to improve the gate stability and reliability [73]. NBTI was performed at $V_{GS, stress} = -30$ V ($V_{DS} = 0$ V) at temperatures of 25 and 150 °C [73,124]. While relatively low positive V_{TH} drift (< 0.2 V) was observed at 25 °C, it increased to ~ 0.4 V for stressing at 150 °C. The positive V_{TH} drift was ascribed to metal electrode injection into OT at negative V_{GS} . In the upcoming work of this group [74], V_{TH} stability under OFF-state step-stress in similar devices was compared for different V_{GS} (0 and -20 V) applied during the stressing, using the same gate-to-drain voltage (V_{GD}). Similar to a previous study, relatively low and recoverable positive V_{TH} drift was observed for step-stress with V_{GD} up to 200 V and $V_{GS} = 0$ V. However, a substantially larger V_{TH} drift (~ 2 V) appeared for $V_{GD} > 100$ V when more negative V_{GS} was applied during the step-stress. The larger V_{TH} drift was explained by a hole-induced degradation model. Here, holes generation via impact ionization [126] or Zener trapping [123] is assumed in the high-field gate-to-drain region in the OFF-state. For stressing with negative V_{GS} , the generated holes can flow to the gate and are assumed to generate new OT in the gate dielectric, similar to TDDB mechanism [127]. The effect of holes generation on the apparent

positive V_{TH} drift was further confirmed by UV light illumination of the devices subjected to OFF-state stressing [128]. However, the observed stress-induced positive shift of V_{TH} was ascribed to electron trapping during the measurement of I_D - V_{DS} characteristic, interrupting the stressing. This clearly illustrates the advantage of the MSM techniques, where V_{TH} drift is sampled quickly after the stress interruption, rather than extracted from slower measurement of the I_D - V_{GS} characteristic.

To mitigate the reverse-bias induced gate degradation in SiN_x/GaN MISFETs, Hua et al. [129] recently processed the transistor with channel converted from GaN to crystalline $\text{GaO}_x\text{N}_{1-x}$ under the gate. The oxynitride with higher bandgap (4.1 eV) compared to GaN (3.4 eV) provides also valence band offset in respect to GaN (0.6 eV), which acts as an energy barrier for holes. This barrier effectively suppresses the injection of the generated holes into the gate, improving the gate stability and robustness [128]. Robustness of V_{TH} stability upon reverse-bias stress in $\text{SiN}_x/\text{GaO}_x\text{N}_{1-x}/\text{GaN}$ MISFETs can be further enhanced by varying the substrate termination [130].

The presented studies clearly point to dominant effect of OT on PBTI as well as NBTI in GaN MISFETs. This means that most commonly used dielectric materials (Al_2O_3 , SiO_2 , SiN) with research [27,28,73,118–122,124,129] as well as industry [131] graded quality contain relatively high density of OT. Apart from BTI issues, these defects represent the concern also in relation to TDDB. However, further research work focusing on the enhanced MSM technique, which allows a detailed study of capture/emission processes in the μ -s range is clearly necessary. Detailed knowledge of the OT origin can, in turn, facilitate their effective suppression via optimization of the dielectric growth technologies.

5. Conclusions and Prospects

This review illustrates that intensive research effort has been dedicated towards development of high-quality dielectric/III-N interface technology as well as deeper understanding of the BTI phenomena in GaN switching transistors. Yet, BTI currently represents a limiting reliability issue of GaN MISHEMTs and MISFETs and further technology improvements are necessary for stable operation of these devices. The observed BTI results from various trap states present in the MIS gates, including dielectric/III-N interface traps and traps distributed in the dielectric bulk (OT, BT, DIGS). In particular, PBTI represents a major concern in D-mode GaN MISHEMTs. Detail analysis of PBTI using enhanced MSM technique suggest existence of 2nd order dynamic effects as well as impact of the barrier conductance on the electron capture process. Despite a clear impact of the gate dielectric material and technology, PBTI seems to follow a common behavior when the gate electrostatic is considered, indicating that density of available traps at the interface is higher than the density of free carrier available in the 2DEG. It is therefore imperative to limit the maximum positive gate bias for D-mode MISHEMTs, so that V_{TH} drift as well as TDDB effects are mitigated. Current understanding of PBTI mechanisms in E-mode GaN MISHEMTs is limited. It seems to be clear, however, that the increased interface potential present in these devices facilitate trapping/de-trapping of very deep traps, which would be inaccessible (and thus benign) in the D-mode counterparts. In respect to PBTI requirements, this effect may limit the applicability of E-mode MISHEMTs for power switching applications.

In the case of GaN MISFETs, further study of PBTI and NBTI behavior in sub-ms time scale is necessary. On the other hand, similar behavior of PBTI has been observed by several groups, with the same empirical models used to describe the observed V_{TH} drift upon stressing and recovery period (Equations (6)–(8)). These results suggest the dominant effect of OT on PBTI as well as NBTI in GaN MISFETs. Currently, it seems that an effective way to mitigate BTI in GaN MISFETs is to optimize the growth of the dielectric, so that formation of the oxide defects is suppressed. However, there is still an open question on the origin of donor states (Q_{comp}), which compensates the GaN surface (spontaneous) polarization charge. Apparent charge neutrality of the dielectric/GaN interface (c.f. Figure 1d) therefore points to the model assuming fixed charge formed by the donor levels located between the dielectric and GaN CB edges [35,38,39]. Nevertheless, considering the current understanding of PBTI in GaN

MIS transistors, the fully recess-gate MISFETs seem to be the preferred concept for E-mode switching device over the MISHEMTs, even though the latter offer slightly lower R_{ON} .

Funding: This research was funded by the Ministry of Education, Science, Research and Sports and the Slovak Academy of Sciences, grant number VEGA 2/0109/17 and VEGA 2/0100/21.

Conflicts of Interest: The authors declare no conflict of interest. The funders had no role in the design of the study; in the collection, analyses, or interpretation of data; in the writing of the manuscript, or in the decision to publish the results.

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