

Review

Heteroepitaxial Growth of III-V Semiconductors on Silicon

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Abstract: Monolithic integration of III-V semiconductor devices on Silicon (Si) has long been of great interest in photonic integrated circuits (PICs), as well as traditional integrated circuits (ICs), since it provides enormous potential benefits, including versatile functionality, low-cost, large-area production, and dense integration. However, the material dissimilarity between III-V and Si, such as lattice constant, coefficient of thermal expansion, and polarity, introduces a high density of various defects during the growth of III-V on Si. In order to tackle these issues, a variety of growth techniques have been developed so far, leading to the demonstration of high-quality III-V materials and optoelectronic devices monolithically grown on various Si-based platform. In this paper, the recent advances in the heteroepitaxial growth of III-V on Si substrates, particularly GaAs and InP, are discussed. After introducing the fundamental and technical challenges for III-V-on-Si heteroepitaxy, we discuss recent approaches for resolving growth issues and future direction towards monolithic integration of III-V on Si platform.

Keywords: heteroepitaxy; monolithic integration; III-V on Si; integrated circuits (ICs); photonics integrated circuits (PICs); antiphase boundary; threading dislocation; thermal crack

1. Introduction

Silicon (Si) has long been of great importance in a wide range of micro/nanoelectronics industry because it offers numerous benefits, such as large wafer size, low cost, abundant source, and mature manufacturing technology [1]. Indeed, for instance, Si-based complementary metal-oxide-semiconductor (CMOS) technology is the fundamental building block in most of the contemporary electronics [2,3], and Si has also been one of the dominant prime materials for photovoltaic technology since the 1950s [4]. More importantly, the utility of Si has expanded from traditional electronics to next-generation photonics industry as Si photonics, enabling ultra-fast and low-cost optical data transmission on Si-on-insulator (SOI) platform compatible with a CMOS process, has emerged recently [5]. Unfortunately, however, bulk Si material is an indirect bandgap semiconductor and hence very inefficient for light emission. Although Si-based light-emitting devices, such as Si Raman laser [6,7] and p-n junction emitter [8–10], have been developed, their performances are impractical and far less than those of III-V devices [11,12]. On the other hand, most III-V semiconductors provide superior optoelectronic properties owing to their direct bandgap and high electron mobility properties. These advantages enable the III-V semiconductors to be widely used in light-emitting/absorbing devices, including light-emitting diodes (LEDs), lasers, detectors, and solar cells [13–16]. In addition, the III-V materials have been employed for power devices, such as high electron mobility transistor (HEMT) [17,18]. However, the limited wafer size of III-V materials (3 or 4 inch), which increases manufacturing cost, is a critical drawback. In addition, the use of III-V semiconductors requires careful attention due to their toxicity [19], and despite the advances in the InP-based PICs [20,21],

the III-V foundry still lacks mature electronic and photonic platforms compared with the Si-based platforms [5,22].

In order to leverage the benefits of both Si (low-cost, large wafer size, and advanced manufacturing technology) and III-V (optoelectronic properties), a heteroepitaxial growth of III-V semiconductors on Si substrates has been extensively investigated since the 1980s [23–29]. In addition, the III-V-on-Si heteroepitaxy has opened the possibility of the monolithic integration of III-V devices on Si-based platform which offers new functionality, low-cost, and dense integration in next-generation photonic integrated circuits (PICs), as well as traditional integrated circuits (ICs) [5,30,31]. For example, to overcome the downscaling limit of conventional CMOS technology, monolithic integrations of various III-V devices, such as InGaAs-based channel field-effect transistor (FET), InP heterojunction bipolar transistor (HBT), and GaN HEMT, have been proposed, enabling dense 3-dimensional integration, low power consumption, and high-speed [32–34]. Notwithstanding the tremendous efforts on III-V-on-Si heteroepitaxy, however, the monolithic integration of III-V devices on Si-based PICs or ICs is not deployed yet, mainly due to the material dissimilarities between III-V and Si introducing a high density of defects, such as antiphase boundaries (APBs) and threading dislocations (TDs) [24,26]. These defects significantly degrade the performance or even prevent the operation of III-V devices. Hence, to avoid the negative influence of high density of defects, most of the current integration processes between III-V and Si commonly adopt heterogeneous approaches using III-V epitaxial layer or devices grown on their native substrates [35,36]. In general, the heterogeneous integration can be achieved by either flip-chip or wafer bonding. The flip-chip bonding process easily integrates the pre-fabricated III-V devices on Si by using solder bump, but it suffers from the requirement of accurate alignment and the limited integration density [12,37]. In case of wafer bonding, a wide range of approaches, such as eutectic bonding [38], adhesive bonding [39,40], solder bonding [41], direct bonding [42–45], and so on [36,46], have been developed. For instance, Si photonics, in which Si-based monolithic light source remains as a missing component over decades, typically adopts plasma-assisted direct bonding of III-V die on SOI platform [47]. Although the III-V quantum-dot (QD) lasers monolithically grown on Si have been successfully demonstrated in recent years [48–53], the integration-incompatibility with other photonic components impedes the deployment on PICs; thus, heterogeneous integration of III-V lasers is the dominant approach in current Si photonics technology. However, the heterogeneous integration still suffers from high manufacturing cost and low integration density [54]. This is mainly due to the inherent limitation of using III-V native substrates. The size and cost of III-V native substrates are much smaller and higher than those of Si substrates, respectively [55]. Therefore, it is crucial to achieve monolithic integration of III-V/Si which enables cost-effective and dense integration.

In this regard, growing high-quality III-V semiconductors on Si is a key pathway towards monolithic integration of III-V devices on Si-based PICs or ICs. For high-quality III-V layer on Si, the main challenges, namely the high density of various defects caused by material dissimilarities, such as large lattice mismatch, polar-on-nonpolar growth, and different coefficient of thermal expansion, should be tackled [12]. Above all, it is prerequisite to prevent the formation of APBs. This is because the APBs nucleated at the interface between III-V and Si can propagate through whole III-V overlayer, and thus the presence of APBs makes it impossible to fabricate the devices [56]. It is also important for high-performance devices to reduce the density of TDs, which act as nonradiative recombination centers and leakage path [28].

In this review, we discuss the recent advances in the heteroepitaxial growth of III-V on Si substrates and focus on the growth of GaAs and InP, which are particularly important materials for laser applications. The growth of III-nitride materials on Si, closely related to the field of LEDs and HEMT, is excluded in this review, and the recent overview of nitride-on-Si can be found in following articles [57–59]. In addition, the dilute nitride materials, such as GaNAsP, have attracted considerable interest recently because of their advantages, such as the direct bandgap property and the lattice-matched growth on Si [60]. Particularly, the growth of lattice-matched GaNAsP-based materials on Si or GaP/Si eliminates an issue of the generation of misfit and threading dislocations [61]. Therefore,

the GaNAsP-based materials are very promising for the monolithic integration of optoelectronic devices on Si-based platform. Indeed, substantial progress has been made in the development of GaNAsP-based photovoltaic cells and lasers monolithically grown on Si-based platform [61–67]. Although the growth of dilute materials on Si is an emerging field in terms of monolithic integration, the physics and growth are quite different from III-V (GaAs and InP), thereby the growth of dilute materials on Si is excluded in this review. The overview for dilute material can be found elsewhere [60,61,68,69].

After a brief introduction to the challenges for III-V-on-Si heteroepitaxy, recent approaches for growing high-quality III-V materials on Si will be addressed: (1) APB-free III-V growth on CMOS-compatible on-axis (001) Si substrates; (2) strategies for reducing the threading dislocation density (TDD); and (3) minimization of thermal cracks. Finally, we summarize the current status and discuss the potential future of III-V-on-Si heteroepitaxy.

2. Fundamental Challenges for III-V Heteroepitaxy on Si

Despite the technological advances in the heterogeneous integration of III-V devices on Si-based platform, monolithic integration, in the long term, is considered as the most promising solution to tackle the limits of current ICs and PICs technology. For the practical implementation of monolithic integration, it is prerequisite to resolve the fundamental problems of III-V-on-Si heteroepitaxy, including APBs, TDs, and thermal crack. In this section, these fundamental challenges which stem from the difference in material properties between III-V and Si will be introduced.

2.1. Antiphase Boundary

First, the formation of APBs arising from the polar on nonpolar nature of III-V/Si heteroepitaxy and monatomic step of (001) Si surface is a critical issue [56,70]. For the vicinal Si(001) surface, a slight misorientation (less than $2^\circ \sim 3^\circ$) with respect to the [001] direction in the [110] and $[\bar{1}10]$ direction, corresponding to the direction of dimer rows, causes monatomic steps [71–74]. Due to the symmetry of diamond structure, two types of steps, running parallel (*A*-type straight step) and perpendicular (*B*-type ragged step) to the dimer rows of the upper terrace, can be found on the vicinal Si(001) surface. Indeed, the neighboring terraces consist of two alternating (2×1) and (1×2) domains. In the zinc-blende structure, e.g., GaAs, InP, and GaP, two face-centered-cubic sublattices are occupied by different atoms. Therefore, if this allocation is changed, the domain with opposite sublattice allocation creates a planar defect called APBs or inversion boundaries (IBs). The domains separated by APBs are known to be antiphase domains (APDs). As shown in Figure 1, for example, monatomic steps on the (001) Si surface result in APDs in the III-V overlayer which are separated by APBs consisting of either III-III or V-V bonds [75]. Even though the formation of wrong bonds across the APBs is energetically unfavorable, this can be easily observed in the III-V epitaxy on nonpolar substrates. APBs containing III-III or V-V bonds are electrically charged defects and thus act as nonradiative recombination centers and electrical leakage path. In addition, the presence of APBs propagating the whole overlayer is likely to prevent the operation of III-V devices because the APB is not a line defect but planar defect. Therefore, achieving APB-free III-V/Si heteroepitaxy is a necessary first stage for growing high-quality III-V overlayer.

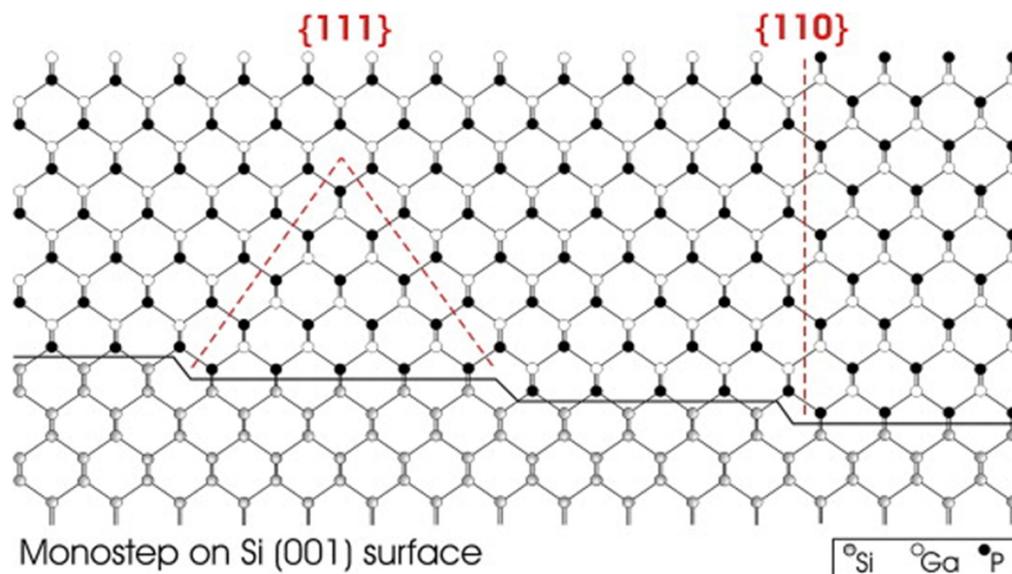


Figure 1. Schematic representation of the formation of antiphase boundaries (APBs) in GaP on silicon (Si) due to the presence of monatomic steps on the (001) Si surface. Reprinted with permission from Reference [75] © 2008 Elsevier B.V.

2.2. Threading Dislocation

Second, the TDs originating from the large lattice mismatch between III-V and Si is also an important issue [28,76–78]. The lattice constant mismatch, e.g., 4% (8%) between GaAs (InP) and Si, introduces a build-up of strain energy on the epitaxial layer during the growth. If the thickness of III-V epilayer on Si exceeds a certain value, the so-called critical thickness, the accumulated strain energy proportional to the thickness of epilayer is released via the formation of misfit dislocations (MDs) along the heterointerface and TDs toward the surface. Matthews et al. [76] described a theoretical model for the critical thickness of epilayer. In this model, it is assumed that a pre-existing dislocation in substrate is replicated in the epitaxial layer and glides back and forth by the misfit strain to create misfit dislocation at the interface. The critical thickness h_c is found to be

$$h_c = \frac{b}{2\pi f} \frac{(1 - \nu \cos^2 \alpha)}{(1 + \nu) \cos \lambda} \left[\ln \left(\frac{h_c}{b} \right) + 1 \right], \quad (1)$$

where b is the length of the Burgers vector for the dislocation, ν is the Poisson ratio, α is the angle between the dislocation line and its Burgers vector, f is the lattice mismatch strain, and λ is the angle between the slip plane and the line in the film plane that is perpendicular to the intersection line of the slip plane and interface.

As the line defects cannot be naturally terminated within the crystal lattice, the MDs along the heterointerface can reach the edge of epilayer or merge with pre-existing TDs within the substrate. In addition, the MDs can form the dislocation half-loop, introducing additional TDs which penetrate the whole layer and reach the surface. Because the dislocation half-loop is likely to be nucleated at pre-existing crystal defects, it is also important to control the crystal imperfection during the growth. It is well known that the TDs introduce the electronic state in the bandgap of III-V semiconductor which acts as nonradiative recombination centers.

The density of TDs is very important and straightforward parameter which describes the quality of epitaxial layer. There are three common approaches used to measure the TDD of III-V epitaxial layer [79–81]: (1) Etch-pit density (EPD) measurement; (2) Transmission electron microscopy (TEM) measurement; (3) X-ray diffraction (XRD) measurement. First, for EPD measurement, etching solution is applied to the semiconductors. Because the etching rate at the dislocation is higher than that

at crystalline region, the pits around TDs are formed and thereby can be easily counted by optical observation or atomic force microscopy (AFM). The EPD measurement is very easy, quick, and cheap process, but it tends to underestimate the TDD. Moreover, quantitative analyses, such as Burgers vector determination, are impossible. Second, TEM measurement enables direct observation of TDs and quantitative analysis. However, an accurate analysis is restricted only to the highly defected crystals because of the small volume of the examined sample. Last, unlike the EPD and TEM measurements, XRD provides non-destructive measurement of TDD in the range from 10^5 to 10^9 cm^{-2} . It is possible to calculate the TDD by measuring a few (hkl) rocking curve widths, because dislocations broaden the rocking curve. Gay et al. [82] and Ayers [81] introduced the theory for the measurement of TDD in metals and (001) zinc-blende semiconductors, respectively.

2.3. Thermal Crack

Finally, a large difference in coefficient of thermal expansion (CTE) causes the introduction of a thermal strain during any temperature changing process [83,84]. In particular, when the wafer cooled down from III-V growth temperature (580 °C for GaAs) to room temperature (RT), the accumulated thermal strain is likely to be relaxed by forming thermal cracks. The thermal cracks can be easily found in the GaAs-on-Si heteroepitaxy, where the GaAs has a larger CTE than Si ($6.6 \times 10^{-6} \text{ K}^{-1}$ and $2.3 \times 10^{-6} \text{ K}^{-1}$ for GaAs and Si, respectively), because a tensile strain is applied to the epitaxial layer during the cool-down process. Griffith [85] first proposed the simple fracture model of brittle materials for predicting the onset of crack growth. In this model, the critical thickness of heteroepitaxial layer under tensile strain can be approximated. The derived condition for crack propagation is [86–88]

$$h_G \geq \frac{2\gamma}{\pi Y \varepsilon_{\parallel}^2}, \quad (2)$$

where h_G is the thickness of epitaxial layer, Y is the biaxial modulus, γ is the surface energy per unit area for semiconductor, and ε_{\parallel} is the in-plane tensile strain.

If the surface energy for the favorable (110) crack plane in zinc-blende structure is approximated by $\gamma(110) = Y(1 - \nu)a/2\sqrt{2}\pi^2$, the Griffith criterion for crack propagation in the (001) heteroepitaxy of a zinc-blende semiconductor becomes [88]

$$h_G \geq \frac{a(1 - \nu)^2}{\sqrt{2}\pi^3 \varepsilon_{\parallel}^2}, \quad (3)$$

where a is the lattice constant, and ν is the Poisson ratio.

The Griffith criterion describes the condition for crack propagation, rather than for crack formation, under pre-existing cracks. Nonetheless, because the presence of any imperfections in the epitaxial layer also affects the crack formation [89], the thickness at which the crack forms may be close to the Griffith thickness h_G [88]. A wide variety of theoretical models which describe the condition for crack formation can be found elsewhere [90,91].

In general, thermal crack lines exactly parallel or perpendicular to each other appear in the III-V epitaxial layer [92]. This can be explained by the unique $\langle 110 \rangle$ {111} slip system in zinc-blende III-V semiconductors. In case of zinc-blende III-V grown on (001) oriented substrates, most of misfit dislocations are 60° dislocations. Particularly, two types of misfit dislocations are preferred, α and β , lying along two orthogonal $\langle 110 \rangle$ directions at the interface, due to the asymmetry of zinc-blende crystal structure [93–95]. At the interface under tensile strain, the α (group V atom core) and β (group III atom core) dislocations have [110] and $[\bar{1}10]$ line direction, respectively. The directions of these dislocations are reversed at the interface under compressive stress. In addition, the asymmetric cracking occurs in III-V epitaxial layer, which means that the density of two orthogonal cracks is quite different [91,93,95,96]. During the early stage of crack formation, cracks with one of $\langle 110 \rangle$ directions are dominant. However, if the epitaxial layer is far thicker than the critical thickness of crack formation,

orthogonal crack lines are commonly observed. This can be ascribed mainly to the difference in glide velocity of α and β dislocations [97].

In addition, as the crack nucleation originates from other pre-existing defects, the presence of any imperfections in the epitaxial layer also affects the crack formation [89]. Like other defects, the presence of thermal cracks introduces destructive effects on the quality of III-V epilayer and performance of optoelectronic devices, such as light scattering centers, electrical leakage path, and limitation on the total thickness of epilayer [98]. More importantly, like the APBs, high density of thermal cracks significantly reduces the yield of device fabrication.

For the GaAs-on-Si, thermal cracks begin to propagate if the thickness of GaAs exceeds about 3 μm , and the number of cracks increases as the thickness increases [89]. As shown in Figure 2a, the cracks appear predominantly in only one of $\langle 110 \rangle$ direction when the thickness of GaAs is close to the critical thickness for crack formation. For the thick GaAs (8.1 μm) layer far beyond critical thickness, high density of cracks in two orthogonal directions can be observed, as in Figure 2b.

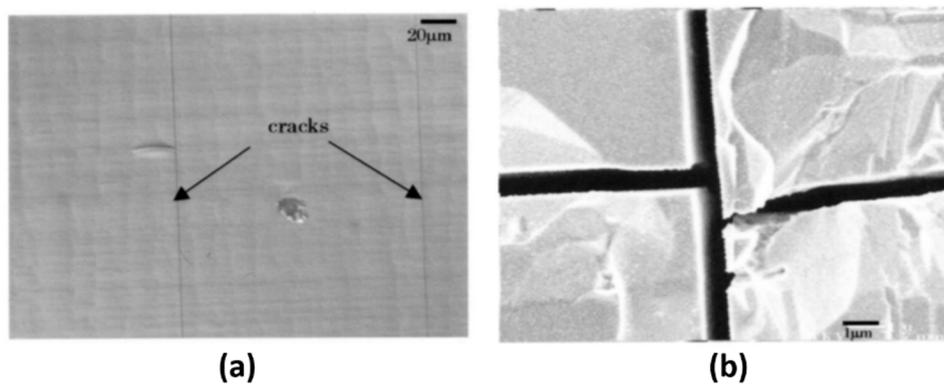


Figure 2. Optical micrographs of thermal cracks formed on GaAs/Si samples (a) with 3.8 μm -thick GaAs layer; (b) with 8.1 μm -thick GaAs layer. Reprinted with permission from Reference [98] © 2003 American Institute of Physics.

For InP-on-Si, on the other hand, the issue of thermal cracks is not as critical as in GaAs-on-Si growth. It was reported that the thermally-induced tensile stress in InP film on Si was much less than that in GaAs film on Si [99]. This can be attributed to the fact that the InP has lower growth temperature and a smaller difference of CTE from Si, compared with GaAs. Additionally, the rearrangement of misfit dislocations in InP, partially accommodating the thermally-induced stress during the cooling process, occurs at relatively low temperature ($\sim 250^\circ\text{C}$).

3. Approaches for High-Quality III-V on Silicon

3.1. APB-Free III-V on Silicon

To obtain a single domain of III-V materials on Si is prerequisite for growing high-quality III-V layer because the APBs, the planar defect, propagate from the heterointerface to the surface. Indeed, the presence of APBs makes it almost impossible to fabricate and operate optoelectronic devices. This section will introduce several methods to achieve APB-free III-V layer on Si substrates, mainly focusing on the use of on-axis (001) Si substrates. This is because most of modern ICs and PICs industry uses CMOS-compatible on-axis (001) Si substrates.

3.1.1. Offcut Silicon Substrates

It is well known that the use of offcut Si substrates with various angles from 4° to 7° is effective in suppression of the formation of APBs [100–103]. As mentioned in Section 2.1, the monatomic steps of the Si(001) surface consist of two alternating (2×1) and (1×2) dimerization. However, it was observed that the misoriented Si with an offcut angle larger than 4° experienced the surface

reconstruction after proper annealing process, yielding a (2×1) single domain [73,74,104,105]. In this case, the Si-Si dimers are parallel to the upper terrace, and the steps are predominantly double-atomic steps. This reconstruction can be explained by the formation energy [74]. The monatomic steps are found to have lowest formation energy, but the formation of double-atomic steps is energetically preferred on the misoriented surface towards $[110]$ or $[\bar{1}10]$ direction, in which the monatomic steps with dimers parallel and perpendicular to the upper terrace alternate. Therefore, the surface reconstruction in the offcut Si(001) is necessary to obtain the single domain of III-V layer on Si [106–109]. However, the formation of double-atomic step doesn't always guarantee the APB-free III-V epitaxial layer on Si. Bringans et al. [110] reported the surface rearrangement of Si(001) by interaction with arsenic. On the double-atomic stepped Si(001) with a (2×1) single dimerization, applying As_4 flux leads to the formation of a monolayer of As-As dimers, depending on the As_4 flux exposure conditions. The orientation of As dimers can be parallel or perpendicular to the step edge, which can affect the nucleation of GaAs. To obtain the III-V single domain on Si, therefore, As or Ga pre-layer, as well as surface reconstruction, should be considered [111–114].

By using offcut Si substrates, high-quality III-V layers on Si without APBs have been successfully demonstrated [16,48,49]. However, the offcut Si substrates are incompatible with CMOS, as well as advanced Si manufacturing technologies. Moreover, recent booming development of Si photonics accelerates the necessity of CMOS-compatible on-axis (001) Si substrates. Unlike the offcut Si, it is very difficult to obtain the single domain of III-V on on-axis Si due to the difficulty in the reconstruction of monatomic steps, and therefore recent research focus of III-V-on-Si heteroepitaxy moved towards the growth of III-V on the CMOS-compatible on-axis (001) Si substrate.

3.1.2. Selective Area Growth

The selective-area growth (SAG), allowing the epitaxial layer to grow on the pre-defined region, has been intensively developed due to its unique defect reduction property, the so-called aspect ratio trapping (ART) [115–118] or necking effect [119,120]. The basic concept of SAG is to trap the defects inside the sidewalls of patterned dielectric mask materials, typically SiO_2 , on Si substrates. Unlike the bulk growth, for the SAG technique, more complex growth parameters, as well as the optimization of mask pattern design, are required to achieve high-quality selective growth because of the reduced dimensions and confined structures [26]. Nonetheless, the SAG is very effective in reducing the density of defects if the dielectric mask pattern has enough aspect ratio (h/w where h and w indicate mask height and width, respectively). As shown in Figure 3, the TD segments are likely to glide along the $\{111\}$ slip plane, which forms an angle of 54.7° with the $\langle 110 \rangle$ orientation during the growth. Hence, the TD segments on the $\{111\}$ slip plane, reaching the oxide sidewall, are trapped, regardless of whether the $\{111\}$ slip plane is parallel or perpendicular to the trench orientation. In addition, the angle of 54.7° determines the minimum aspect ratio (at least 1.43) for trapping the TDs on the $\{111\}$ slip plane. The SAG using trench structures also traps the planar defects, namely the APBs, in a similar way of TDs. However, only planar defects formed on the $\{111\}$ plane parallel to the trench orientation can be trapped, as shown in the third case of Figure 3. In other words, the planar defects on planes perpendicular to the trench orientation will not be trapped. However, Orzali et al. [121], who employed the chemically etched V-shaped Si surface for defect reduction, reported that the nucleation of GaAs initiated only on the etched $\{111\}$ Si plane contributed to the prevention of APB formation.

Even though many SAG techniques have shown their capability of reducing the density of defects, the APB issue is not fully resolved. In order to address APB and rough surface issues, growing III-V materials on the chemically etched (111) Si surface with nanowire coalescence was proposed [122,123]. For example, Li et al. [123] reported GaAs-on-V-grooved Si (GoVS) templates which offered APB-free flat GaAs layer on on-axis (001) Si substrates. To obtain GoVS template, n-type on-axis (001) Si substrates patterned with SiO_2 stripe were chemically etched by potassium hydroxide (KOH) solution to form trench structure exposing (111) facets, and subsequently the GaAs nanowires were selectively grown on the V-grooved Si by metal-organic chemical vapor deposition (MOCVD). After removing

the SiO₂ stripe pattern, coalesced GaAs thin films were regrown on the nanowire arrays. Figure 4a shows a scanning electron microscopy (SEM) image of the resultant coalesced GaAs layer with a flat surface. The surface morphology of 300 nm-thick coalesced GaAs layer measured by atomic-force microscopy (AFM) produced a root-mean-square (rms) of 1.9 nm across a scanned area of 5 × 5 μm². The APBs were not observed in the GoVS template, which can be explained by the III-V growth on Si {111} plane. A transmission electron microscopy (TEM) image in Figure 4b presents a unique stacking fault trapping. It was shown that a tiara-like structure beneath the SiO₂ sidewall, created by Si undercutting, effectively trapped most of the stacking faults around the interface of GaAs/Si(111). Owing to this unique trapping mechanism, after removing the SiO₂, the subsequent GaAs overgrowth can be performed with maintaining the ability of defect trapping, as shown in Figure 4c. Although some of stacking faults can escape the tiara-like structure in the thick stacking-disorder regions, the escaped stacking faults can be annihilated by crossing of two stacking faults due to the closely spaced V-groove structure.

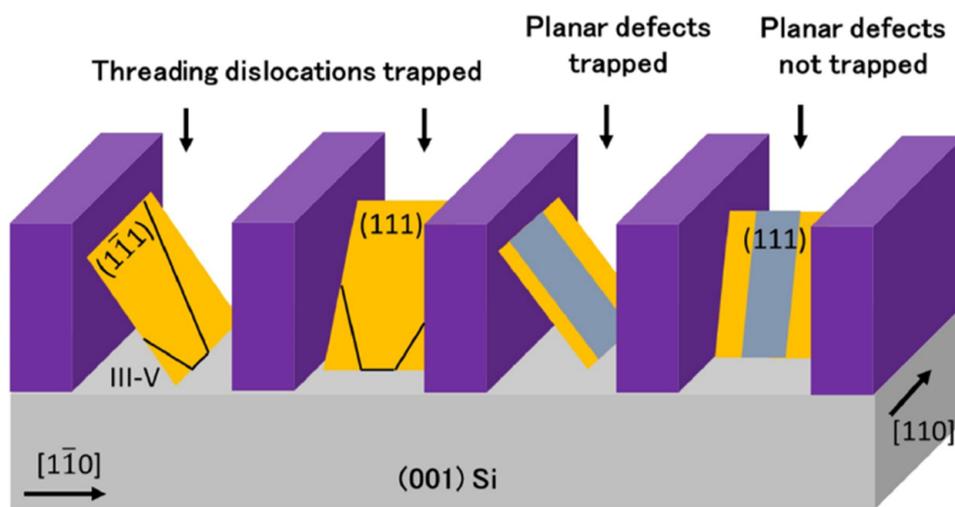


Figure 3. Schematic illustration of capability for trapping threading dislocations (TDs) and APBs in aspect ratio trapping (ART) technique. Reprinted with permission from Reference [24] © 2017 Elsevier, Ltd.

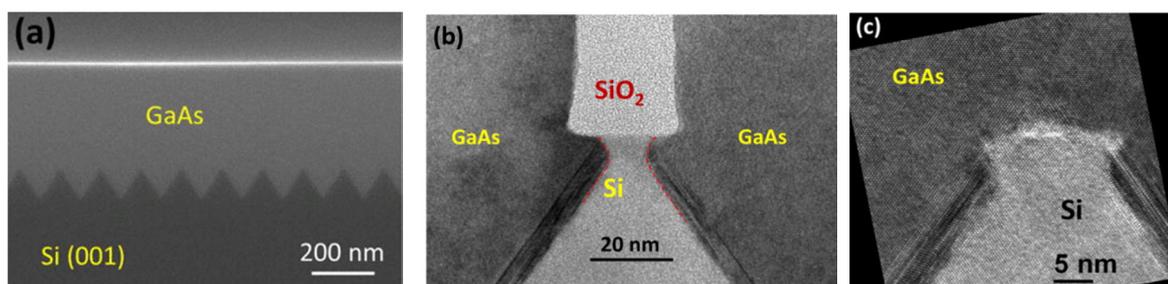


Figure 4. (a) Cross-sectional scanning electron microscopy (SEM) image of 300 nm-thick coalesced GaAs film grown on a nanowire array. Cross-sectional Transmission electron microscopy (TEM) images showing stacking fault trapping by tiara-like structure formed by the Si undercut (b) with SiO₂ sidewall and (c) in the coalesced GaAs film after removing SiO₂. Reprinted with permission from Reference [123] © 2015 AIP Publishing, LLC.

For the InP growth on on-axis Si, Zhu et al. [124], investigating the APB-free InP-on-grooved Si (IoVS) templates similar to the GoVS, demonstrated electrically pumped 1.5-μm InGaAs/InAlGaAs laser monolithically grown on IoVS template. The method for obtaining IoVS template is very similar to that of GoVS. A main difference is that a 10 nm-thick GaAs wetting layer was grown on the exposed

(111) Si facets before the InP nanowire growth. This is because employing GaAs wetting layer reduces a strain for InP growth and prevents InP seed layer from being clustered.

3.1.3. MOCVD/MOVPE-Grown Buffer Layer

Alcotte et al. [125] developed APB-free GaAs layer directly grown on nominal (001) Si substrates without the SAG. In this work, microelectronics standard nominal (001) Si 300 mm wafers, first deoxidized in a SiConiTM chamber with NF₃/NH₃ remote plasma, were subsequently transferred into the MOCVD chamber and annealed at high temperature (800 °C–950 °C) in H₂ ambient. This optimized preparation promotes reconstructing the 2 × 1 surface, namely the formation of double atomic steps, which is believed to be a crucial step for inhibiting the formation of APBs. In Figure 5a, the AFM image of a 400 nm-thick GaAs grown on unoptimized Si shows a high density of randomly distributed APBs. In contrast, the optimized Si surface mainly consists of double atomic steps (Figure 5b), and the APBs were not observed in the 150 nm-thick GaAs layer grown on optimized Si (Figure 5c). In addition, the surface roughness of 150 nm GaAs layer grown on optimized Si was measured to be 0.8 nm rms, corresponding to the lowest value reported for 1 μm-thick GaAs grown on offcut Si substrates.

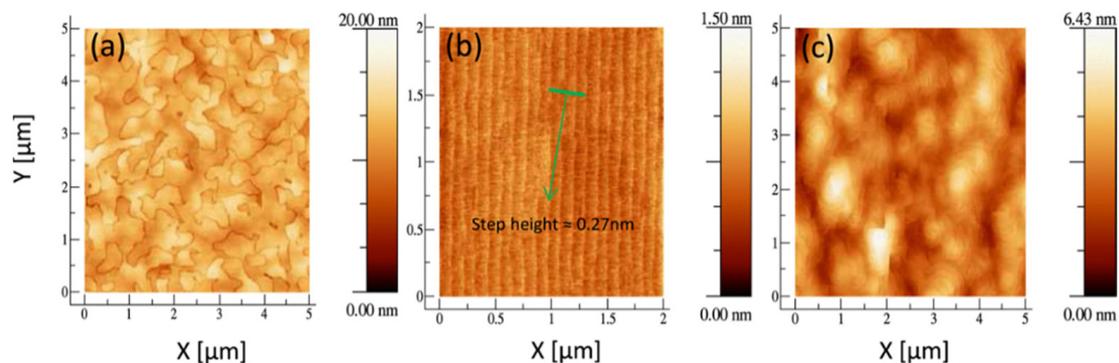


Figure 5. (a) $5 \times 5 \mu\text{m}^2$ atomic force microscopy (AFM) image of a 400 nm-thick GaAs grown on un-optimized (001) Si with high density of randomly distributed APBs. Root-mean-square (RMS) roughness = 1.6 nm. (b) $2 \times 2 \mu\text{m}^2$ AFM image of optimized (001) Si (800 °C–950 °C annealing under H₂). The surface mainly consists of double-atomic steps. (c) $5 \times 5 \mu\text{m}^2$ AFM image of APB-free 150 nm-thick GaAs grown on optimized (001) Si. Reprinted from Reference [125] © 2016 Author(s), under a Creative Commons Attribution license (CC BY) 4.0.

In addition to the GaAs/Si, Volz et al. [126] also demonstrated the APB-free GaP/Si template using homoepitaxial Si buffer and heteroepitaxial GaP buffer layer grown by vapor phase epitaxy (VPE) and metal-organic vapor phase epitaxy (MOVPE), respectively. To obtain APB-free GaP/Si template, the 500 nm-thick homoepitaxial Si buffer layer was first grown on deoxidized on-axis (001) Si at 200 mbar and 850 °C, where the optimized post-annealing (10 min, 950 mbar H₂, 975 °C) process was subsequently performed. In Figure 6a, the AFM image of the annealed Si buffer surface confirms the formation of double-atomic steps (0.27 nm height), which is believed to be responsible for preventing APB nucleation. Then, the GaP layer was grown on the prepared Si buffer layer in a two-step procedure consisting of a nucleation and an overgrowth. For the optimal growth of GaP nucleation layer, flow-rate modulated epitaxy (FME) method, in which the Ga and P precursors are alternately injected into reactor, was employed. The low-temperature FME growth mode results in a two-dimensional continuous GaP nucleation layer, irrespective of whether Ga or P was first deposited. Figure 6b presents a TEM image of a continuous GaP nucleation layer grown by P-started FME method at 450 °C. In contrast, a continuously-injected nucleation forms three-dimensional GaP islands, which can evolve into stacking faults upon coalescence. After the growth of the optimal 3 nm GaP nucleation layer, bulk GaP layer was overgrown at 625 °C with continuous growth mode. As shown in Figure 6c, most of APBs are self-annihilated within 50 nm-thick GaP layers by kinking

towards {111} plane or higher index plane. Consequently, the formation of double-atomic steps by the annealed homoepitaxial Si buffer contributed to the suppression of APB nucleation, and the two-step GaP growth on the Si buffer consisting of low-temperature (LT) FME nucleation and high-temperature HT overgrowth enabled APBs to kink and self-annihilate with each other.

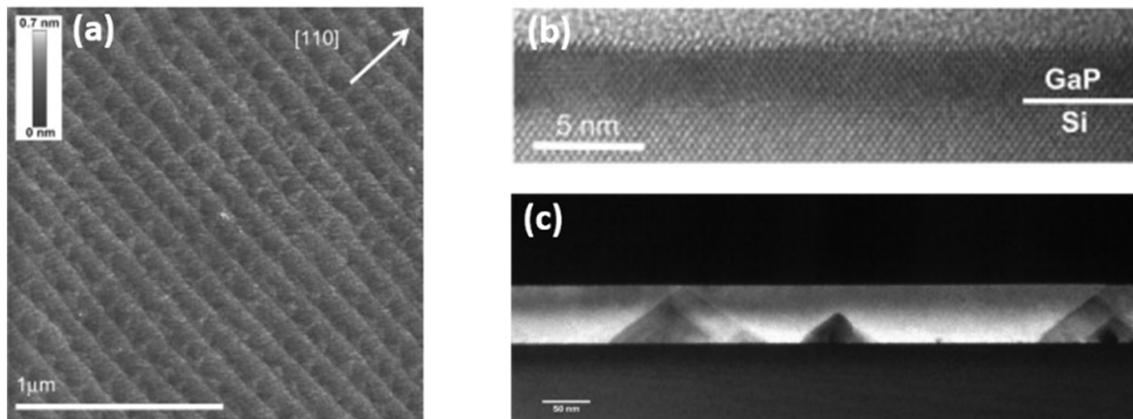


Figure 6. (a) AFM image of Si homoepitaxial buffer surface grown on (001) Si which is annealed under optimized condition (10 min, 950 mbar H₂, 975 °C); (b) high resolution TEM image of GaP nucleation layer on Si (nucleation temperature of 450 °C, flow-rate modulated epitaxy (FME) method, and P-started nucleation). (c) Cross-sectional TEM dark field image of GaP layer continuously grown at 625 °C with an optimized GaP nucleation layer. Reprinted with permission from Reference [126] © 2010 Elsevier B.V.

3.1.4. MBE-Grown Buffer Layer

Most of the mature approaches for APB elimination employ MOCVD/MOVPE growth system to obtain virtual templates, such as GoVS, GaAs/Si, and GaP/Si. In general, these methods require pre-treatment under high temperature and high-pressure hydrogen before growth to promote the formation of double-atomic steps. On the other hand, solid-state molecular beam epitaxy (MBE) doesn't provide the hydrogen-based treatment. Nonetheless, all MBE-grown and APB-free III-V layer on on-axis Si is beneficial in terms of the low-cost and straightforward process because III-V devices grown on GaP/Si or GaAs/Si virtual substrates commonly use two different growth system, namely III-V and APB-free buffer growth by MBE and MOCVD/MOVPE, respectively. In addition, the MBE system has shown superior performance in growing high-quality InAs/GaAs QD lasers, which are promising Si-based light sources in Si photonics.

There have been only a few reports on the approaches using direct MBE growth without a virtual template. For example, Kwoen et al. [127], investigating the effect of AlGaAs nucleation layer on the elimination of APBs, demonstrated APB-free GaAs layer directly grown on on-axis (001) Si. In this paper, four different compositions of 40 nm-thick Al_xGa_{1-x}As nucleation layer was investigated, and subsequently 2.3 μm-thick GaAs buffer layer was grown. Figure 7a–d present the cross-sectional SEM images of GaAs/Si with Al_xGa_{1-x}As and GaAs nucleation layer. Unlike the GaAs/Si with Al_{0.7}Ga_{0.3}As seed layer in which APBs extended to GaAs surface (Figure 7d), the Al_{0.3}Ga_{0.7}As seed layer was effective in self-annihilation of APBs near the nucleation layer (Figure 7b). The GaAs crystal quality was also confirmed by photoluminescence (PL) emission intensity. As shown in Figure 7e, the PL intensity of InAs QD layer grown on GaAs/Si with Al_{0.3}Ga_{0.7}As nucleation layer was two times higher than that with a GaAs nucleation layer, and, as the Al content of Al_xGa_{1-x}As nucleation layer increases, the PL intensity tended to decrease. It was revealed that the APB-free GaAs layer could be obtained by employing the Al_{0.3}Ga_{0.7}As nucleation layer and the APB suppression mechanism was attributed to the self-annihilation of APBs rather than the formation of double-atomic step on

Si surface. However, the detailed annihilation mechanism is not clearly understood, and the critical growth parameters remain uncertain.

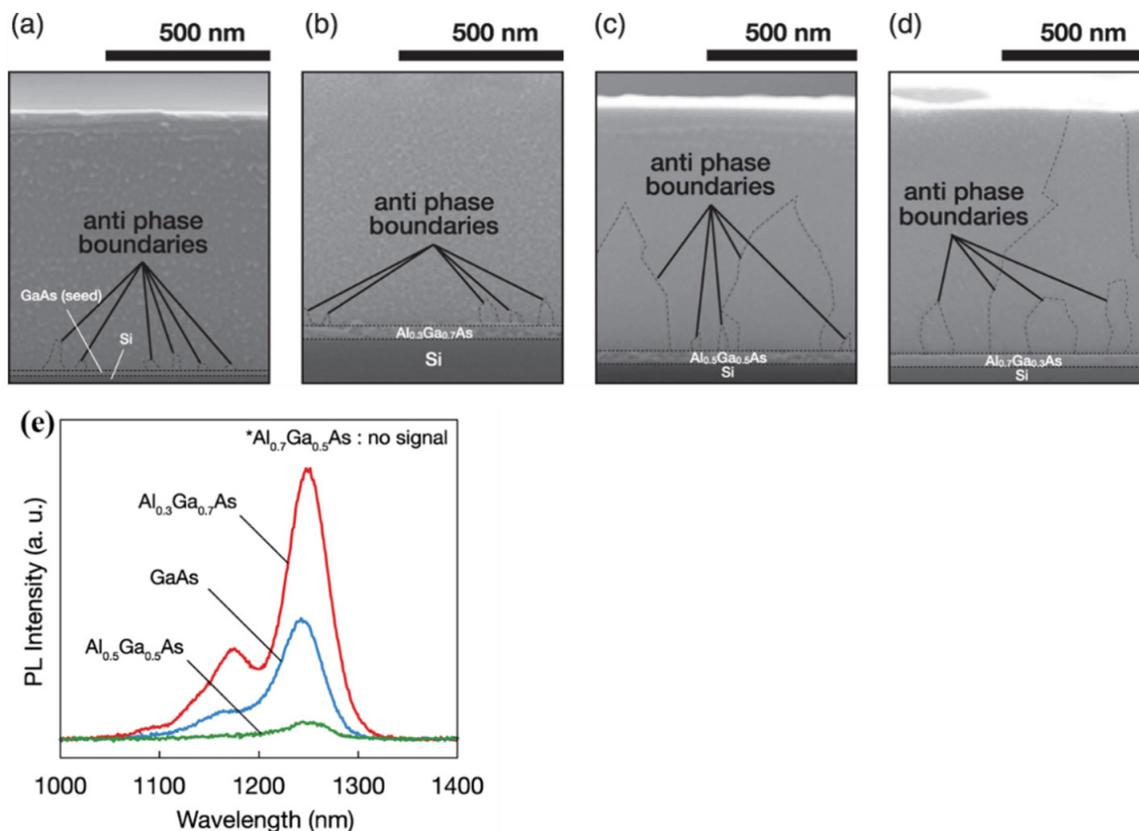


Figure 7. Cross-sectional SEM images of GaAs layer with (a) GaAs nucleation layer, (b) $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ nucleation layer, (c) $\text{Al}_{0.5}\text{Ga}_{0.5}\text{As}$ nucleation layer, and (d) $\text{Al}_{0.7}\text{Ga}_{0.3}\text{As}$ nucleation layer grown on (001) Si substrates. (e) Room temperature photoluminescence (PL) intensity of an InAs quantum-dot (QD) layer grown on Si with different nucleation layer. Reprinted with permission from Reference [127] © 2019 The Japan Society of Applied Physics.

It was previously believed that the formation of double-atomic (D) steps on Si was the key step for APB or IB annihilation during the III-V growth on Si. In 2020, however, Li et al. [128] first proposed a new mechanism for APB annihilation and reported all MBE-grown APB-free GaAs monolithically grown on on-axis Si (001) using an annealed Si buffer layer. In this report, a 200 nm-thick Si buffer layer, comprised of 100 nm-thick Si layer and five sets of 20 nm-thick Si layers annealed at 900 °C and 1200 °C, respectively, was grown on the deoxidized on-axis (001) Si substrate. Subsequently, conventional GaAs buffer layer, defect filter layers (DFLs), and QD laser structures were grown. Both the use of AlGaAs seed layer [127,129] and heat treatment on the deoxidized Si (001) substrate up to 1200 °C [130], known to offer APB-free GaAs growth on Si, showed APBs on the GaAs surface in this experiment, whereas the sample with an annealed 200 nm-thick Si buffer layer exhibited APB-free GaAs surface. To examine the origin of the APB annihilation, AFM images of surface morphology of Si substrates without and with the annealed Si buffer layer were shown in Figure 8a,b, respectively. Contrary to the deoxidized Si surface showing a random atomic-step distribution (Figure 8a), ordered Si steps were observed in the annealed buffer Si surface, as shown in Figure 8b. The ordered Si steps consist of alternating straight and meandering Si monatomic steps (Figure 8c), each of which has the height of around 0.13 nm (Figure 8d). This indicates that the annealed Si buffer produces single-atomic (S) steps rather than the D steps. The inset of Figure 8c illustrates a schematic diagram of alternating straight and meandering single-atomic steps denoted by S_a and S_b , respectively.

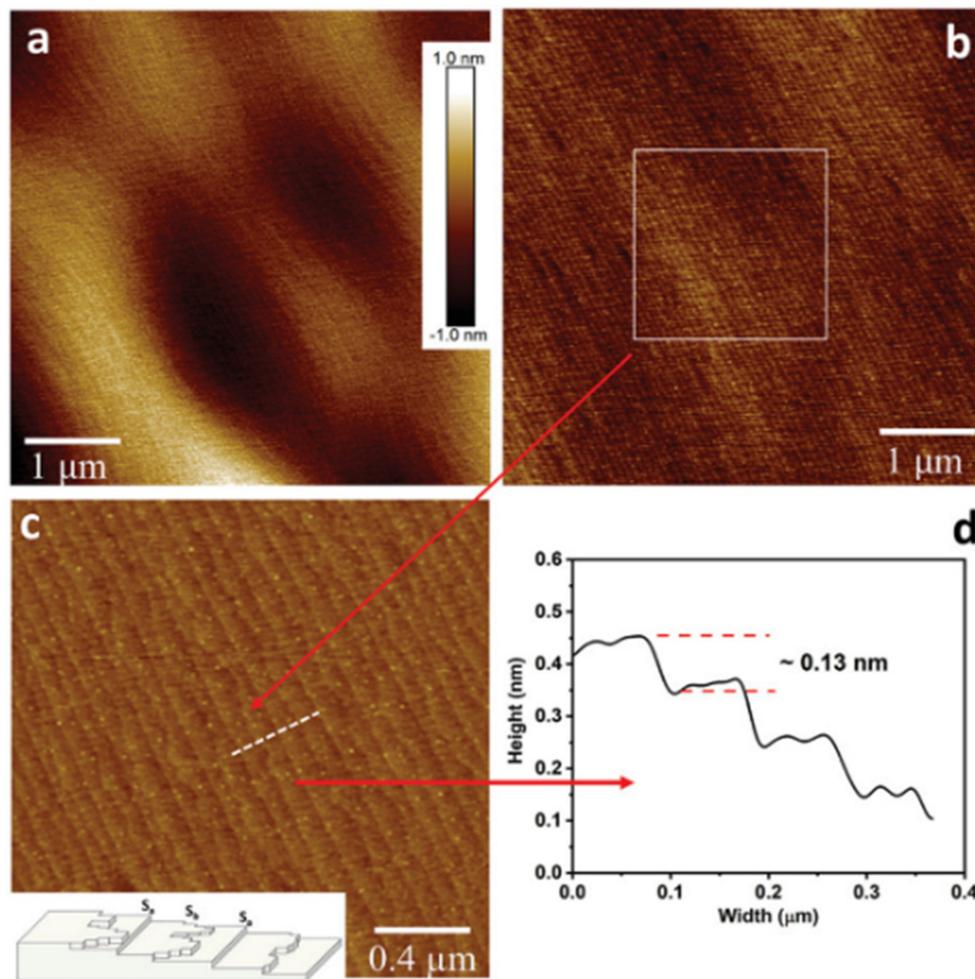


Figure 8. $5 \times 5 \mu\text{m}^2$ AFM images showing surface morphology of (a) Si surface after 30 min deoxidation and (b) surface of 200 nm-thick Si buffer layer on Si. (c) $2 \times 2 \mu\text{m}^2$ AFM image of Si buffer layer with alternating S steps; inset: schematic illustration of alternating straight S_a and meandering S_b steps. (d) Height measurement of each step on the 200 nm Si buffer. Reprinted from Reference [128] © 2020 The authors, under CC BY.

Cross-sectional TEM measurements with two viewing directions of $[110]$ (Figure 9a–d) and $[\bar{1}\bar{1}0]$ (Figure 9e,f) were conducted on the sample without and with the annealed Si buffer layer. For the sample without the annealed Si buffer, although the APBs nucleated at the GaAs/Si interface propagate along higher index planes and hence annihilate with each other (Figure 9a), some APBs which are not self-annihilated penetrate the whole GaAs layer (Figure 9c). For the sample with the annealed Si buffer, on the other hand, periodic arrays of the self-annihilated APBs, where the distance between the periodic arrays corresponds to the half-width of each Si step terrace, were observed in Figure 9b. Moreover, most of the APBs initiated from $S_a + S_b$ array were annihilated within 500 nm-thick GaAs layer, as shown in Figure 9d. A similar tendency was also confirmed from $[\bar{1}\bar{1}0]$ direction view in Figure 9e,f. Consequently, it was revealed for the first time that the Si surface with alternating straight S_a and meandering S_b single-atomic steps, formed by the annealed Si buffer layer, enabled the periodic APBs to follow the shapes of $S_a + S_b$ steps and annihilate within 500 nm-thick GaAs overlayer.

3.2. Reduction of the Dislocations

For high-quality III-V layer monolithically grown on Si, achieving a low density of TD is a key issue. In particular, the TDs penetrating an active region of optoelectronic devices significantly degrade their performance. For example, quantum-well (QW) lasers monolithically grown on Si substrates,

in which the TDD is $5 \times 10^7 \text{ cm}^{-2}$ corresponding to common TDD of GaAs/Si, shows no lasing behavior [131]. Therefore, a great deal of effort has been made on the reduction of TDD since the 1980s, and now the TDD of about 10^6 cm^{-2} for GaAs-on-Si can be achieved [48,132]. This section introduces general approaches essential for reducing TDD in III-V/Si heteroepitaxy.

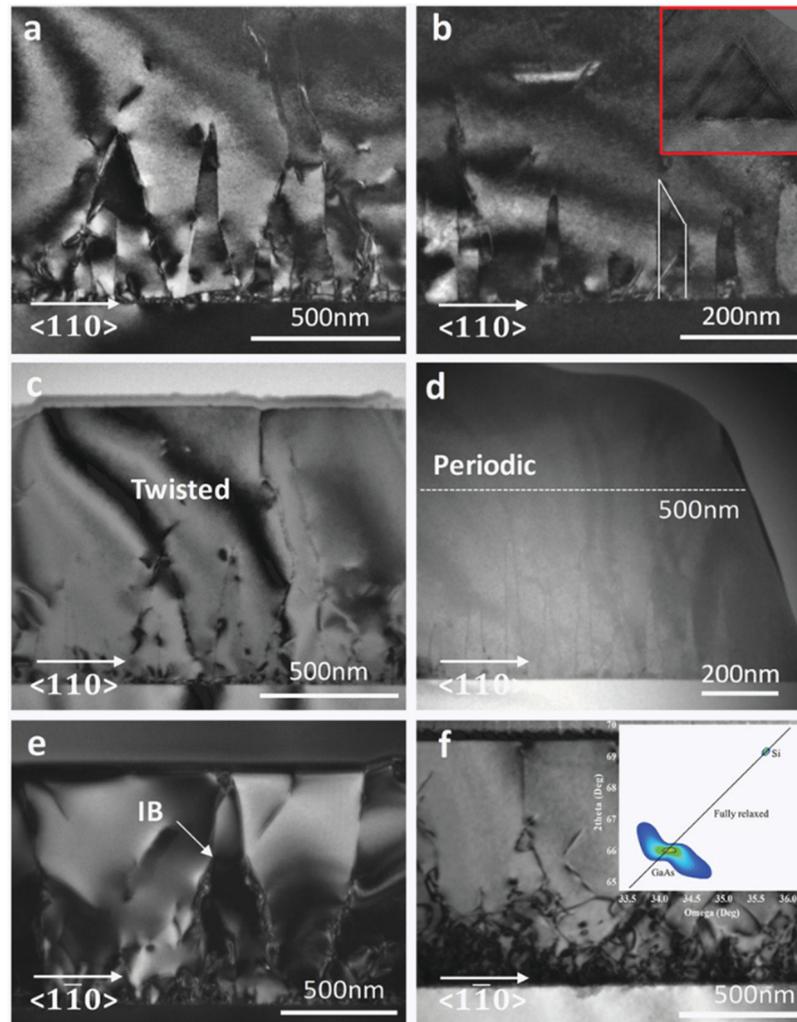


Figure 9. Cross-sectional TEM measurements of inversion boundary (IB) propagation and annihilation of sample without and with Si buffer. Dark field TEM images with $[110]$ direction view for sample (a) without and (b) with Si buffer; inset: a stacking fault at nucleation layer. Bright field TEM images with $[110]$ direction view for sample (c) without and (d) with Si buffer. TEM images with $[\bar{1}\bar{1}0]$ direction view for sample (e) without and (f) with Si buffer; inset: XRD reciprocal space mapping (RSM) image of fully IB-free $1 \mu\text{m}$ GaAs on on-axis (001) Si substrate. Reprinted from Reference [128] © 2020, the authors, under CC BY.

3.2.1. Nucleation and III-V Buffer Layer

Initial stage of III-V growth on Si plays an important role since the growth begins with the formation of the island on Si surface, which considerably affects the TDD of the following overlayer. Therefore, a wide variety of methods have been extensively studied, including Si buffer layer [133,134], pre-layer formation [112,135,136], two-step growth [106,108], migration-enhanced epitaxy [137,138], and amorphous buffer layer [139,140]. Among these approaches, the so-called two-step growth has been most widely adopted in GaAs/Si. The two-step growth starts with low-temperature (LT) growth ($400 \text{ }^\circ\text{C}$) of GaAs in the initial stage, followed by annealing and growing the GaAs at typical growth temperature about $550 \text{ }^\circ\text{C}$ – $600 \text{ }^\circ\text{C}$. The reason for using this growth order is because at LT the GaAs

becomes continuous before the defects are introduced. Figure 10 compares the ways how the GaAs islands coalesce into a continuous layer at high and low growth temperature [25]. At the typical growth temperature of GaAs (550 °C~600 °C), the GaAs islands have a lot of defects before coalesced. Once these islands coalesce, the defects, trapped inside the island, are extended in continuous layer. Then, the extended defects are difficult to be removed. In general, LT growth introduces a higher density of islands than that of high-temperature (HT) growth due to the reduced diffusive mobility of adatoms. For LT growth, therefore, many defects originating from the high density of islands are generated. Hence, two-step growth including LT growth is expected to produce high density of defects. However, the two-step growth generally exhibits much better structural properties than single-step growth. This can be explained by that the defects of which the form is less diverse and more mobile may annihilate during growth and coalescing.

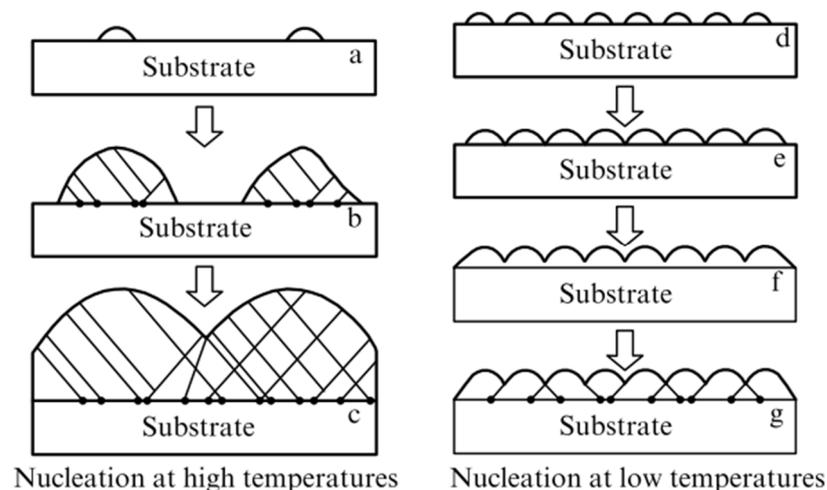


Figure 10. Two ways of introducing misfit dislocations at high-temperature (HT) and low-temperature (LT). Left: Misfit dislocations (MDs) are introduced before the islands coalesce. Right: MDs are introduced after the islands become continuous pseudomorphic film. Reprinted with permission from Reference [25] © Uspekhi Fizicheskikh Nauk 2008.

In addition, a three-step growth, the modified two-step growth method in which an intermediate-temperature (IT) layer is added between LT and HT layer, was commonly employed in recent years [128,141–143]. Nozaki et al. [144] proposed and reported that the three-step growth method in GaAs-on-Si improved the surface morphology, as well as crystallinity. The detailed mechanism of this improvement was not clearly understood, but it was ascribed to the GaAs top layer grown at HT without direct contact to the LT nucleation layer. In addition, Wang et al. [145] directly compared the effect of three-step growth on the quality of GaAs on Si with two-step growth. It was shown that the three-step growth with two thermal cycle annealing produced rms roughness of 1.8 nm and the TDD of $1.1 \times 10^7 \text{ cm}^{-2}$ ($3 \times 10^6 \text{ cm}^{-2}$) calculated from XRD (EPD), all of which are improved compared with the conventional two-step process.

Similar to GaAs/Si, the InP-on-Si system also commonly employs the two-step growth [146–148]. However, direct growth of InP on Si produces much higher TDD than that of GaAs on Si due to larger lattice mismatch (~8%) [149]. For the InP-on-Si, accordingly, the insertion of the intermediate buffer layer between InP and Si is preferred.

3.2.2. Intermediate Buffer Layer

To avoid the problem arising from material dissimilarity between Si and III-V, the basic solution to insert other materials of which the lattice constant and CTE are matched with Si has been developed. For GaAs/Si heteroepitaxy, a wide variety of methods using germanium (Ge) [150–154], GaAsP [155,156], and InGaP [157] were developed. Among these materials, Ge has been most widely used because of

its complete miscibility with Si, well-developed Ge-on-Si growth technology, and nearly the same lattice constant and CTE matching between GaAs and Ge [158]. Moreover, the compositionally graded Ge/Ge_xSi_{1-x} offers efficient strain relaxation in the buffer layer, and therefore a final Ge cap layer serves as a virtual substrate for GaAs growth. In 1991, Fitzgerald et al. [159] reported the primary study on the compositionally graded Ge_xSi_{1-x} layers ($x = 0.23, 0.32, \text{ and } 0.5$) on Si, producing the TDD on the order of low 10^6 cm^{-2} . After that, substantial efforts have been devoted to achieving an artificial Ge/Ge_xSi_{1-x}/Si substrates [113,160–164]. For instance, Groenert et al. [158] demonstrated RT continuous-wave (cw) GaAs/Al_xGa_{1-x}As QW lasers monolithically grown on the graded Ge/Ge_xSi_{1-x}/Si virtual substrates. As shown in Figure 11, most of dislocations are effectively confined within graded Ge_xSi_{1-x} buffer layer, which offers strain relaxed pure Ge top layer and GaAs layer. The TDD on the Ge cap layer was measured to be $1.2 \times 10^6 \text{ cm}^{-2}$.

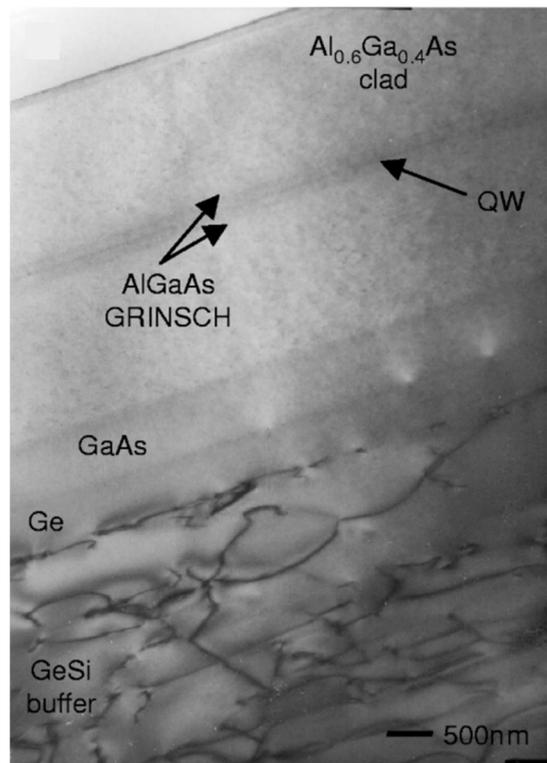


Figure 11. Cross-sectional TEM image of GaAs-based laser structures on germanium (Ge)/GeSi/Si. Reprinted with permission from Reference [158] © 2003 American Institute of Physics.

Today, for GaAs/Si system, direct growth of GaAs buffer layers using multi-step growth method is more preferred to the intermediate buffer layer, such as Ge or graded GeSi layers. This is because the use of Ge/GeSi buffer generally requires much thicker layers than that of common GaAs buffer layers despite similar TDD on the order of low 10^6 cm^{-2} . For the monolithic integration on Si platform, in general, a thin buffer layer is favorable in terms of thermal cracks [98] and co-integration with other components [12]. Although using thin Ge/GeSi buffer layers has been also demonstrated [165], the order of TDD ($\sim 10^8 \text{ cm}^{-2}$) is much higher than that of thick Ge/GeSi or GaAs buffer layer ($\sim 10^6 \text{ cm}^{-2}$). In addition, the chemical-mechanical polishing (CMP) process [164] used to obtain smooth surface in rough Ge/GeSi buffers can increase the fabrication cost and complexity.

Unlike the GaAs/Si, the InP/Si heteroepitaxy normally adopts the intermediate (graded) buffer layers because of the large lattice mismatch between InP and Si ($\sim 8\%$). The prevailing material commonly used for the intermediate buffer is GaAs [166–169]. The most typical approach for growing InP on Si is employing the mature multi-step growth of GaAs on Si with strained-layer superlattices filtering the TDs [149,170,171]. Even though the GaP buffer layer has also been utilized, it was known

to be less effective in terms of TDD, residual stress, and quality of InP, compared with the GaAs buffer layer [172–174]. Besides, the employment of compositionally graded buffer layer, including InGaAs, InGaP, InAlAs, and InGaAlAs alloys, has shown successful reduction of the TDD in InP/GaAs [175–178]. For example, Quitoriano et al. [175], who studied graded buffers grown on GaAs substrates to obtain high-quality InP without phase separation, demonstrated low TDD of $1.2 \times 10^6 \text{ cm}^{-2}$ through the hybrid InGaAs and InGaP graded buffer layer. In a similar way, to further decrease the TDD of InP/GaAs/Si epitaxy, growing the graded buffer layers on the GaAs/Si substrates has also been explored. For instance, Shi et al. [149] have shown a low TDD of $5 \times 10^6 \text{ cm}^{-2}$ by using 1.8 μm -thick graded $\text{In}_{0.4}\text{Ga}_{0.6}\text{As}$ buffers on 2 μm -thick GoVS template.

3.2.3. Epitaxial Lateral Overgrowth

Epitaxial lateral overgrowth (ELO) is also an important technique to inhibit the propagation of TDs in epitaxial layer. Like ART process reviewed in Section 3.1.2, ELO is also based on SAG method. In the ELO process, a III-V buffer layer is first grown on Si substrate, and subsequently a dielectric mask, such as SiO_2 , is deposited on the III-V buffer layer. Then, the dielectric mask is selectively etched to expose the III-V buffer layer for regrowth. Then, the III-V epitaxial layer is vertically regrown through the opened region of the mask and thereafter can be laterally grown over the mask. The most of TDs in the buffer layer are blocked by the bottom of the mask, but a small number of TDs around the opened region will propagate upwards, as shown in Figure 12a. Therefore, the laterally grown epitaxial layer above the dielectric mask exhibits a high crystalline quality.

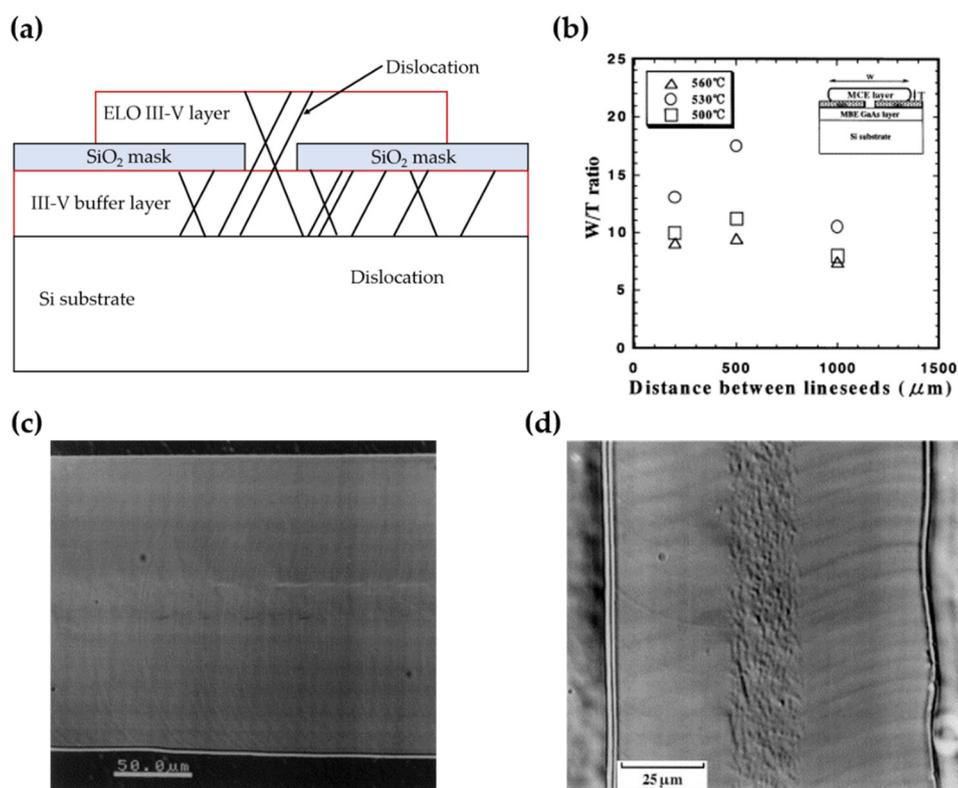


Figure 12. (a) A schematic illustration of the epitaxial lateral overgrowth (ELO). (b) Dependence of width to the thickness (W/T) ratio on the growth temperatures and the line separation of the opened mask. (c) Optical microphotograph of the surface of ELO GaAs layer after 7 h growth. The width and thickness of the layer are 195 and 12 μm , respectively. (d) Optical microphotography of the ELO GaAs layer after KOH wet etching. The width of the etch-pit-free laterally grown region is 43 μm . (b–d) Reprinted with permission from Reference [179] © 1998 Elsevier Science B.V.

For the GaAs on Si, pioneering works on ELO have been reported since 1980s [180–182]. However, the early reports on ELO for GaAs-on-Si suffered from the limited defect-free region and the mechanical weakness of the laterally grown parts, both of which became severe as the ELO layer was further grown. In order to resolve these limitations of ELO technique, a great deal of effort has been dedicated to optimizing growth conditions [118,179,183–189]. For example, Chang et al. [179], investigating the dependence of the ratio of the ELO layer width to the thickness (W/T ratio) on the growth temperature and the seed line separation, showed that the width of dislocation-free GaAs region achieved about 43 μm . In this work, misoriented (100) Si substrates, on which a GaAs buffer layer was grown by MBE, were used for ELO of GaAs by liquid phase epitaxy (LPE). For comparison, the width of the line seed (opened region for regrowth) was fixed as 5 μm , but the line seed separation was varied as 200, 500, and 1000 μm . In addition, growth temperature of GaAs was chosen as 500, 530, and 560 $^{\circ}\text{C}$. As shown in Figure 12b, a maximum W/T ratio of 17.5 was achieved by the line seed separation of 500 μm and the growth temperature of 530 $^{\circ}\text{C}$. Figure 12c shows a wide ELO layers of 195 μm -width after the growth time of 7 hours. To identify dislocation-free region, etch-pit density (EPD) was measured by KOH etching. As shown in Figure 12d, a high density of TDs which propagated from the GaAs buffer layer through the narrow line seed region can be clearly seen. However, no etch pits were found in the laterally overgrown GaAs. In addition, He et al. [188] proposed a three-stage ELO to obtain uniform and flat coalescence of selectively grown GaAs. In this report, 1.8 μm GaAs buffer was first grown on 4 $^{\circ}$ offcut (001) Si substrate toward the <011> direction. Then, 80 nm-thick SiO₂ mask was deposited on buffer layer, and nano-trench of 120 nm-width and 100 nm-separation was patterned on the mask. Last, the three-stage of ELO growth, comprised of the selective growth, coalescence, and planar growth stage, were carried out by MOCVD. It was shown that the nano-trench and three-step growth resulted in a mirror-smooth coalesced 410 nm-thick GaAs film.

In case of InP-on-Si, ELO techniques have been more widely employed [190–196], compared with GaAs-on-Si in which direct growth of GaAs on Si is preferred. Because it is very difficult to obtain low density of TDs through the direct growth of InP on Si, the use of ELO method is beneficial for achieving high-quality InP layer on Si. For the optimization of parameters of InP ELO on (001) InP substrate, Sun et al. [197] investigated the dependence of lateral overgrowth and vertical growth rate of InP on the mask stripe orientation. It was revealed that while the vertical growth rate was relatively independent of the opened stripe orientation, the maximum lateral overgrowth rate was achieved when the opened stripe oriented at 30 $^{\circ}$ and 60 $^{\circ}$ off [110] direction, as shown in Figure 13a. Following this result, Sun et al. [198] achieved a broad lateral overgrowth of InP on (001) Si substrate. In addition, Metaferia et al. [199] studied the morphological evolution during ELO of InP on Si with mesh opening, and showed that the coalesced region produced the TDD in a range from $6 \times 10^6 \text{ cm}^{-2}$ to $4 \times 10^7 \text{ cm}^{-2}$ depending on the thickness of ELO layer. In this work, 1.5 μm -thick InP/Si and 40 nm-thick SiO₂ mask were used to overgrow InP. The mesh and line masks (opening and masking width of 200 nm and 3 μm , respectively), tilted 15 $^{\circ}$ and 30 $^{\circ}$ off the [110] direction, are compared. The angle between the opening line in mask and [110] direction was chosen from previous result by Sun et al. [197]. As shown in Figure 13b,c, the coalescence of the InP layer occurs predominantly at the corners of the mask. Such a coalescence mechanism in mesh mask resulted in higher growth rate than that in line mask, attributed to the less probability of the boundary plane formation. The quicker coalescence in the mesh opening resulted in better surface roughness at the early growth stage (~10 μm -thick InP layer), but, after an extended growth (~100 μm -thick InP layer), both mesh and line opening cases exhibited a similar surface roughness (rms roughness of 16 nm~25 nm). It was shown that regardless of both angles (15 $^{\circ}$ and 30 $^{\circ}$) and masks (mesh and line opening) the TDDs were measured to be similar value. The TDD of about 10 μm -thick and 100 μm -thick InP layer was measured to be $2\text{--}4 \times 10^7 \text{ cm}^{-2}$ and $6\text{--}7 \times 10^6 \text{ cm}^{-2}$, respectively.

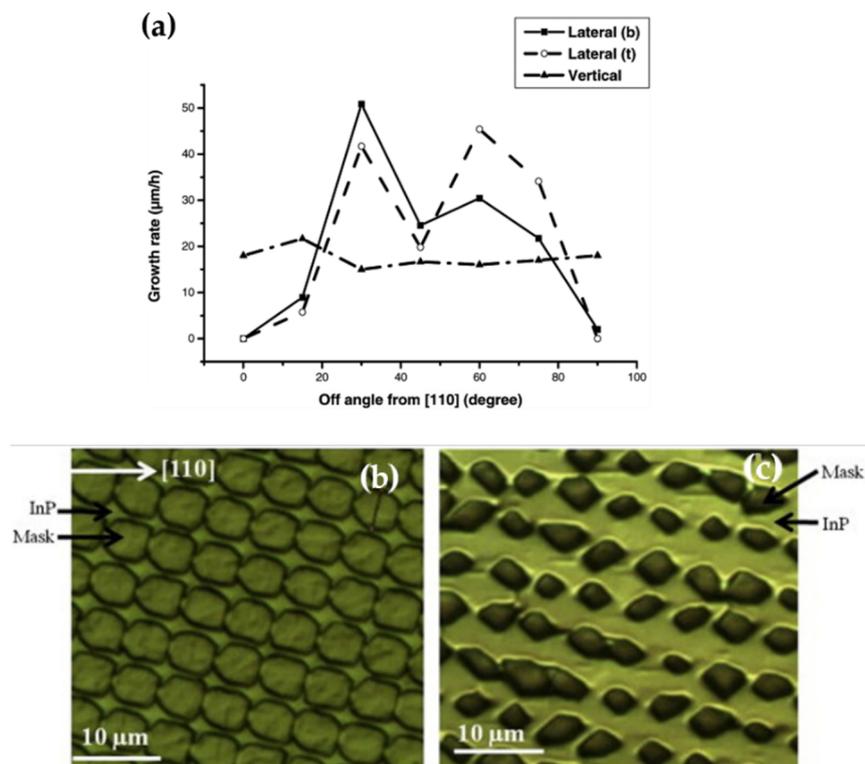


Figure 13. (a) Dependence of the growth rates on the off angle from [110] direction. Nomarski contrast images of sample after (b) 0.5 min and (c) 1.5 min growth with mesh opening mask tilted 15° off [110]'s direction. (a) Reprinted with permission from Reference [197] © 2001 Elsevier Science B.V. (b,c) Reproduced with permission from Reference [199] © 2011 Elsevier B.V.

3.2.4. Thermal Annealing

The traditional way to reduce defect density is thermal cycle annealing (TCA) during growth, enabling thermally-activated dislocation migration and thus the annihilation of dislocations. Indeed, the TCA-induced reduction of TDD in GaAs/Si has been substantially investigated [200–205]. For instance, Yamaguchi et al. [201], investigating the TCA effects on the defect reduction in GaAs/Si, reported that the dislocation density was considerably reduced as the annealing temperature and cycling number increased. The etch pit density (EPD) was reduced from 10^8 cm^{-2} to $2 \times 10^6 \text{ cm}^{-2}$ after TCA. It was revealed that the thermally-induced stress as a driving force of dislocation motion contributed to the dislocation annihilation, such as coalescence. The numerical analysis also showed that the large number of TCA and/or annealing temperatures of more than 700 °C were effective in the reduction of TDD. However, in the case that the grown films initially have low density of dislocation which can move and coalesce, the attainable reduction of TDD is limited. In addition, Jung et al. [203] demonstrated that the in-situ TCA effectively reduced the TDD of GaAs grown on on-axis GaP/Si (001). To investigate the effect of in-situ TCA, a 1.5 µm-thick GaAs layer was first grown on GaP/Si, followed by four cycles of annealing. Then, another 1.5 µm-thick GaAs layer was regrown. For comparison, 3 µm-thick GaAs layer was also grown on GaP/Si without TCA. During in-situ TCA, the wafer was heated up to 700 °C and held for 5 min. Then, the temperature cooled down to 320 °C. The electron channeling contrast imaging (ECCI) revealed that the TDD of the TCA-treated sample ($5.5 \times 10^7 \text{ cm}^{-2}$) was much lower than that of untreated sample ($2.8 \times 10^8 \text{ cm}^{-2}$). It was also found that the TCA process improved the surface roughness from 7.8 nm to 4.8 nm (rms). Recently, Shang et al. [206] investigated the effect of TCA on the reduction in TDD of GaAs-on-Si template. As shown in Figure 14A, a minimum TDD of $3 \times 10^7 \text{ cm}^{-2}$ was obtained after 12 cycles of TCA. A noticeable reduction in TDD was achieved at 4 (8) cycles of annealing at 735 °C (700 °C). The maximum annealing temperature was set to below 745 °C because annealing at above 745 °C causes remarkable degradation of the GaAs surface, such as

the formation of Ga droplet, as shown in Figure 14B. In Figure 14C, ECCI images showed that the TDD was reduced from $4.18 \times 10^8 \text{ cm}^{-2}$ to $3 \times 10^7 \text{ cm}^{-2}$ after 16 cycles of TCA. It should be noted that a surface TDD lower than $2 \times 10^6 \text{ cm}^{-2}$ was obtained after a step-graded filter layer was grown on the post-TCA GaAs-on-Si. In a similar mechanism of TCA, post-growth annealing (PGA), carried out after completing the growth, has also been widely employed to reduce the TDD of GaAs [207–209].

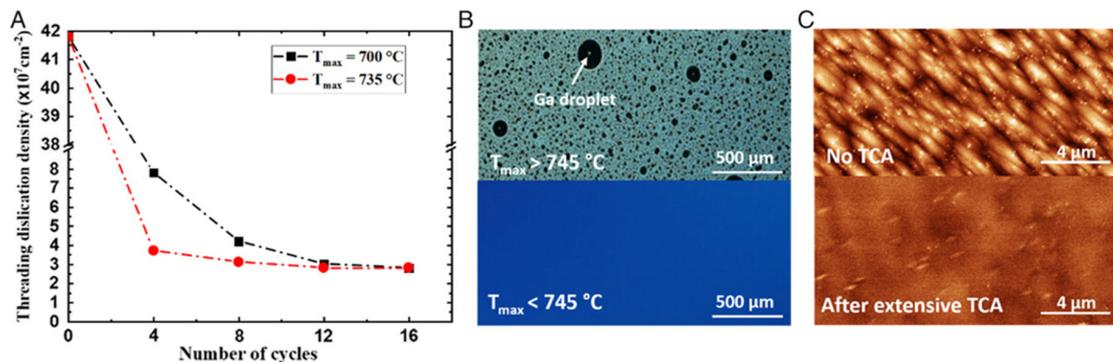


Figure 14. (A) Dependence of the threading dislocation density (TDD) of GaAs-on-Si template on the number of thermal cycle annealing (TCA) cycles. (B) Nomarski contrast images of the GaAs surface after annealing above and below 745 °C pyrometry temperature. (C) Electron channeling contrast imaging (ECCI) images of the GaAs surface without TCA (top) and with 16 cycles of TCA (bottom). Reprinted from Reference [206] © 2020 The authors, under CC BY.

For the InP/Si, TCA or PGA has also been applied to improve the crystal quality [168,169,210,211]. However, the effect of thermal annealing on the defect reduction is not as dramatic as in GaAs/Si because the difference of CTE between InP and Si is relatively small; thus, the dislocation motion by thermally-driven stress is limited.

3.2.5. Strained-Layer Superlattices Defect Filter Layer

Strained-layer superlattices (SLSs) have long been extensively investigated in order to reduce the dislocation density since the 1980s [212–215]. Matthews et al. [212], who proposed the use of an SLS to reduce the TDD, demonstrated that the strain field in GaAsP-GaAs superlattice turned aside the TD propagating upward. The SLSs commonly consist of multiple pairs of two lattice-mismatched layers alternately under compression and tension. If the thickness of each SLS layer is less than a certain critical thickness, which otherwise creates misfit dislocations, each SLS layer accommodates elastic strains caused by lattice mismatch. The strain field of SLSs can bend over and force the dislocations propagating upward to move laterally toward the edge of the sample, leading to the dislocation coalescence and annihilation. Noted that the SLSs should have enough lattice mismatch and thickness to generate strain required for bending dislocations.

Ternary-binary SLSs DFLs have been widely used in GaAs/Si heteroepitaxy, including InGaAs/GaAs, InAlAs/GaAs, GaAsP/GaAs, and so on [216–224]. For example, Mingchu et al. [224] optimized InGaAs/GaAs DFLs for 1.3- μm QD lasers on Si. In this work, the indium composition and thickness in $\text{In}_x\text{Ga}_{1-x}\text{As}/\text{GaAs}$ SLSs, as well as the growth condition of GaAs spacer layer, were investigated. In the growth method I (Figure 15a), the GaAs spacer layer was grown while the temperature in chamber was ramping up from 420 °C to 610 °C after the SLS growth at 420 °C. In contrast, in the growth method II (Figure 15b), the GaAs spacer layer was grown at 610 °C after finishing the ramp-up of temperature and in-situ annealing of the SLSs. In Figure 15c, the PL peak intensity of QD laser structure with growth method II was at least three times higher than that with growth method I. This improvement can be attributed to the high-temperature growth of GaAs spacer layer and in-situ annealing of SLSs. The high-temperature growth and annealing promoted the dislocation motion and resultant annihilation. It is also revealed that the optimized indium composition

and GaAs thickness in SLSs were 0.18 and 10 nm, respectively. In Figure 15d, it was shown that the employment of three sets of $\text{In}_{0.18}\text{Ga}_{0.82}\text{As}/\text{GaAs}$ SLSs DFLs effectively blocked and annihilated the TDs.

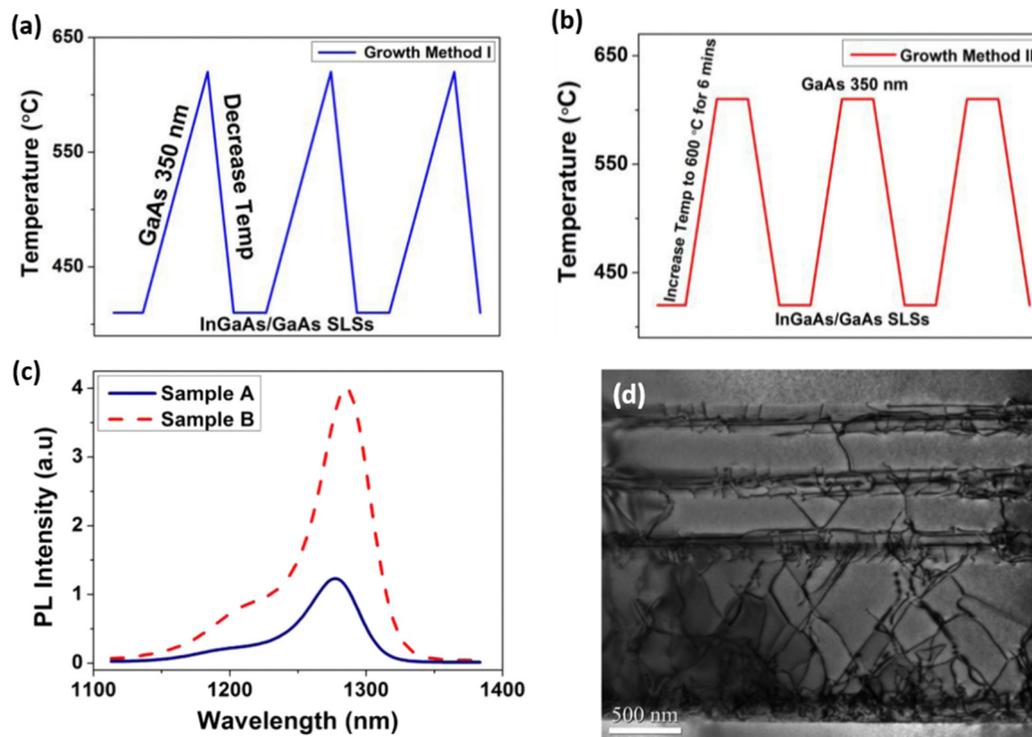


Figure 15. (a) Growth method I: The GaAs spacer layer was grown during the ramp-up of temperature from 420 to 610 °C and then cooled down to 420 °C for subsequent growth of InGaAs/GaAs strained-layer superlattices (SLSs) (b) Growth method II: The GaAs spacer layer was not grown during the ramp-up of temperature from 420 to 610 °C, and grown only at a stable temperature of 610 °C and then cooled back to 420 °C for subsequent InGaAs/GaAs SLSs growth. (c) PL spectra measured at room temperature of sample A (growth method I) and B (growth method II). (d) Dark-field cross-sectional TEM image of optimized three layers of defect filter layers (DFLs). Reprinted from Reference [224] © 2016 The authors, under CC BY.

In the InP/Si platform, the DFLs based on InGaAs/InP, In(Ga)AsP/InP, (In)GaP/InP, and so on [149,170,225–230] have been also commonly adopted. For instance, Shi et al. [149] reported the effect of $\text{In}_{0.73}\text{Ga}_{0.27}\text{As}/\text{InP}$ SLSs DFLs on the reduction of TDD in InP grown on on-axis (001) Si. In this report, InP buffer layers were first grown on GoVS template using multi-step growth, followed by four sets of InGaAs (13 nm)/InP (19 nm) 10-pair SLSs with 300 nm-thick InP spacer layers. In Figure 16a, bright-field scanning transmission electron microscopy (STEM) image of InP-on-Si structure exhibits the generation and propagation of TDs. A high density of TDs on the order of 10^{10} cm^{-2} generated from the InP/GaAs interface (line 1) was reduced to the TDD of $1.5 \times 10^9 \text{ cm}^{-2}$ through multi-step grown InP buffer layer (line 2). The final InP surface defect density was measured to be $1.17 \times 10^8 \text{ cm}^{-2}$ after four sets of InGaAs/InP DFLs (line 6). In Figure 16b, a zoomed-in STEM image of SLSs DFLs clearly shows that most of the dislocations are bent along the bottom or top interfaces of each SLS layer, resulting in the mutual annihilation of TDs. It was also revealed that SLSs with high indium composition ($\text{In}_{0.82}\text{Ga}_{0.18}\text{As}$) achieved low TDD of $7.9 \times 10^7 \text{ cm}^{-2}$ but formed rough surface with many hillocks. By considering surface morphology, as well as defect filtering efficiency, therefore, the optimized indium composition was about 71%. However, in general, using SLSs DFLs in InP-on-Si is not as effective as in GaAs-on-Si. For example, the TDD of InP-based materials remains on the order of 10^8 cm^{-2} , while, in GaAs-based materials, the order of 10^6 cm^{-2} can be achieved. The reason for

the discrepancy is not clearly understood, but it is believed to be due to the phase separation in the SLSs and/or the high density of dislocations arising from larger lattice mismatch in InP/Si than that in GaAs/Si [175]. It is also reported that, if the TDD is on the order of 10^8 cm^{-2} or greater, the SLSs is not very effective in dislocation filtering [216].

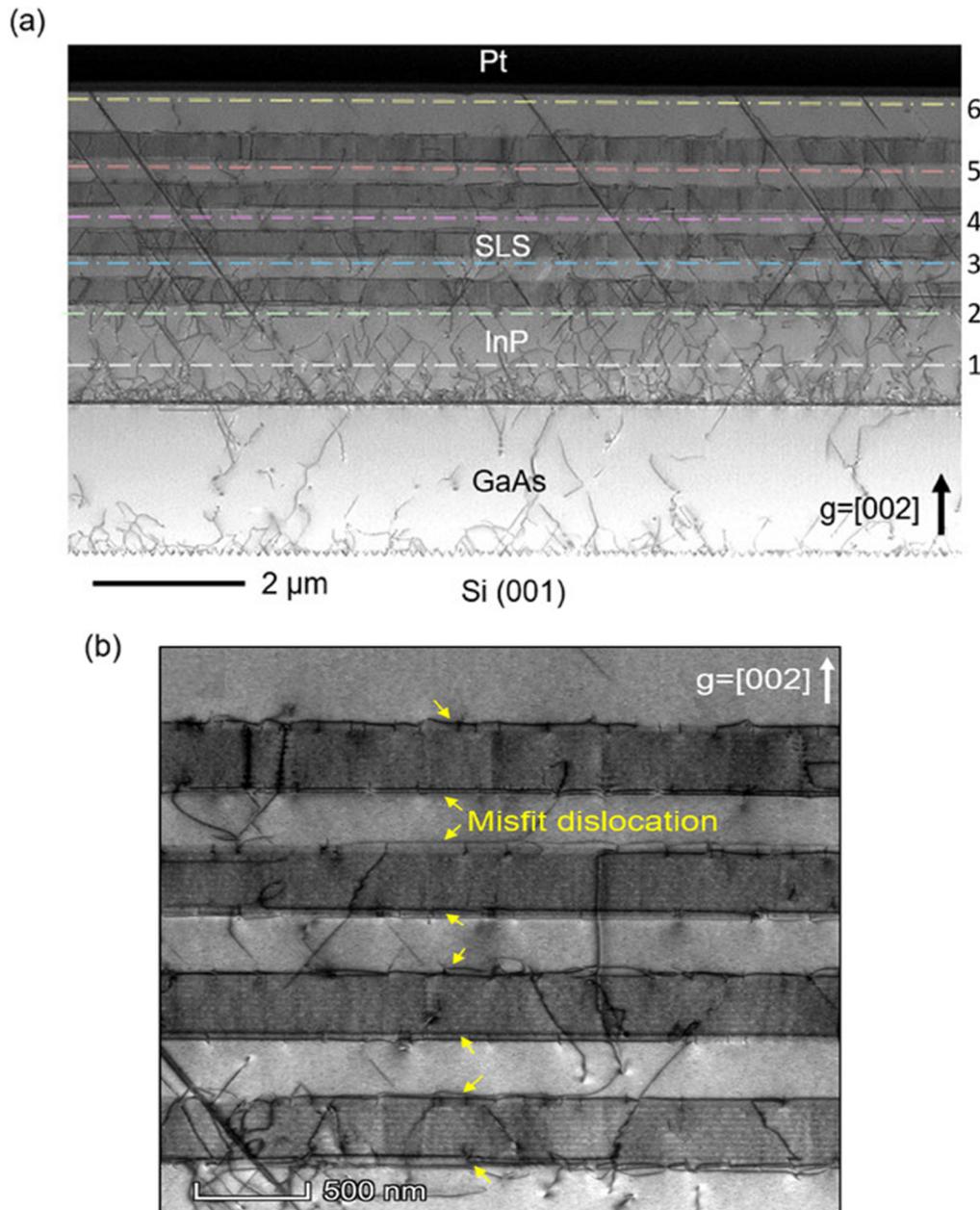


Figure 16. (a) Cross-sectional STEM image of InP-on-Si showing the generation and propagation of TDs and stacking faults. (b) Zoomed-in STEM images of SLSs DFLs region showing the propagation of TDs. Reprinted with permission from Reference [149] © 2020 American Institute of Physics.

In addition, instead of SLSs, the self-assembled QDs can be used as DFLs [231–233]. The employment of InAs QDs as DFLs in GaAs-based material was first proposed and demonstrated by Yang et al. [231]. Because the strain-driven self-organized QDs produce large three-dimensional strain field around themselves, dislocations around QDs can be bent over and annihilated in a similar way to SLSs DFLs. For instance, Shi et al. [232] reported a four-fold reduction in density of TDs in InP/Si system by using self-organized InAs/InAlGaAs QDs as DFLs. In Figure 17a, a number of TDs,

generated from InP/GaAs and GaAs/Si interfaces, propagate toward the top surface, leading to the TDD of $1.3 \times 10^9 \text{ cm}^{-2}$. In contrast, adopting the seven-layer of InAs/InAlGaAs QDs DFLs in InP/Si clearly shows dislocation bending and filtering effects, offering a four-fold reduction in TDD ($3.2 \times 10^8 \text{ cm}^{-2}$), as shown in Figure 17b.

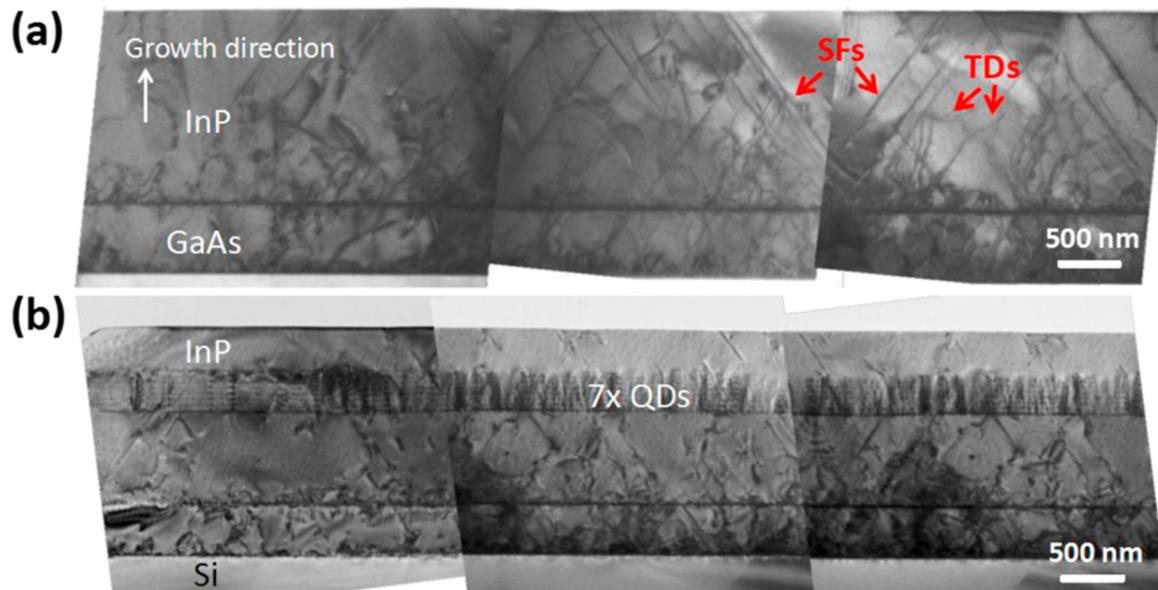


Figure 17. (a) Large-area cross-sectional TEM images of the InP-on-Si (a) without and (b) with QD DFLs. Reprinted with permission from Reference [232] © 2016 Elsevier B.V.

3.3. Minimizing Thermal Cracks

Controlling thermally-induced strain during the growth is very important because the residual strain by a large difference of CTE leads to thermal cracks or delamination, which are unacceptable for the device fabrication. In order to prevent the crack formation, basically, the thickness of epitaxial layer should be less than the critical thickness of crack formation. In addition, any imperfections, such as surface contaminants and defects, should be minimized because the formation of thermal crack is heterogeneous nucleation [98]. For III-V-on-Si heteroepitaxy, however, both thick buffer layers and crystal imperfections are inevitable. Therefore, various strategies for minimizing thermal cracks, including porous Si layer [234], strain compensated layer [235,236], use of indium dopant [237], and patterned substrate [83,92,238,239], have been proposed. Among these techniques, the use of patterning has been widely developed. For example, Huang et al. [239] reported crack-free GaAs layer on Si with an area of $800 \times 700 \mu\text{m}^2$ by employing mid-patterned growth. In this work, to obtain crack-free GaAs/Si template, three steps were carried out: (1) a $2.3 \mu\text{m}$ -thick GaAs layer with AlAs/AlGaAs nucleation layer was first grown on (100) Si substrate with 3° off toward [011], and the in-situ TCA was applied; (2) rectangular mesa structures ($800 \times 700 \mu\text{m}^2$) were achieved by chemical etching with $\text{H}_2\text{SO}_4/\text{H}_2\text{O}_2/\text{H}_2\text{O}$ (1:1:2) and KOH (40 wt. %) solutions in sequence; (3) a $1.7 \mu\text{m}$ -thick GaAs buffer layer was regrown, and the second in-situ TCA was performed. Then, GaAs-based Fabry-Perot filtering cavity with an InP-based p-i-n absorption structure was finally grown on the mid-patterned GaAs/Si platform. As shown in Figure 18a, no crack line is observed in the wet-etched epilayers grown on mid-patterned GaAs/Si. In contrast, for the sample without patterning, a high density of crack lines ($\sim 112 \text{ cm}^{-1}$) parallel to the [011] or $[0\bar{1}1]$ direction was confirmed in Figure 18b. The crack-free and high-quality GaAs layer was attributed to the mid-patterned growth that enables the thermal stress to be consumed for reducing dislocation. In other words, the thermal energy was used to form the parallel dislocations, which alleviates the thermal stress.

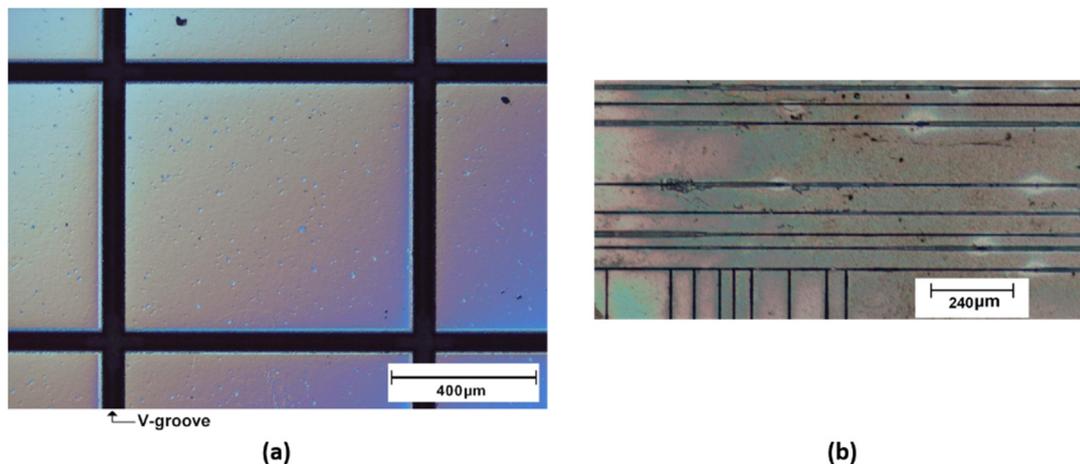


Figure 18. Nomarski optical micrograph of the etched surface morphologies of GaAs/Si sample (a) with and (b) without mid-patterned growth. Reprinted with permission from Reference [239] © 2008 American Institute of Physics.

Recently, approaches using the Ge on the micropillar patterned Si(001) substrates were proposed [240–245]. For instance, Falub et al. [244] reported that the closely spaced Ge and GeSi crystals with arbitrary height were grown on the deeply etched micropillar patterned Si(001) substrates. In this work, the self-limiting lateral growth of Ge crystals on micropillar patterns (height, width, and spacing are 1.7–8 μm , 0.75–15 μm , and 0.2–50 μm , respectively) enables very thick Ge towers (up to, but not limited to, 50 μm) without cracking. The crack propagation was impeded by preventing a continuous growth of Ge, and the TDs are trapped at the sidewall of Ge crystals with ART process. In a similar way, Zhang et al. [243], who employed {113}-faceted Ge/Si (001) hollow substrate, showed a crack-free GaAs film up to 7 μm . To fabricate the template illustrated in Figure 19a, the U-shape grating pattern (period, ridge width, and depth were 360, 140, and 500 nm, respectively) was defined on an on-axis Si (001) substrate by using deep ultraviolet lithography and reactive ion etching. After the deposition of 60 nm Si buffer on the patterned substrate, a 600 nm Ge layer was grown to achieve the {113}-faceted Ge hollow structures, as shown in Figure 19b. Then, the typical two-step GaAs and InAs/GaAs dot-in-a-well structure were grown on the template for the characterization of epitaxial layer. To characterize the thermal strain issue, a high-resolution XRD reciprocal space mapping was performed around (004) and (2-)-2(-)4 reflections. From peak positions in Figure 19c,d, the in-plane and out-of-plane lattice constants for GaAs (Ge) were measured to be 5.660 \AA (5.659 \AA) and 5.648 \AA (5.654 \AA), respectively. The in-plane strain ε_{\parallel} of GaAs (Ge) was calculated to be 1.13×10^{-3} (1.68×10^{-4}) by comparing the measured lattice constants with the lattice constant of bulk GaAs (5.653 \AA) and Ge (5.658 \AA). It was revealed that the residual thermal strain of Ge layer on the hollow Si substrate (1.68×10^{-4}) was 89.8% lower than that of a Ge layer on normal Si substrates (1.65×10^{-3}) [241]. The residual thermal strain of GaAs layer in this work (1.13×10^{-3}) was 29.4% lower than that of GaAs layer on the conventional Ge/Si substrates (1.6×10^{-3}) [246]. The reduction of thermal strain was ascribed to the presence of extra free surface. As a result, the 7 μm -thick GaAs layer, which is far beyond the typical value of the cracking thickness, can be grown on {113}-faceted Ge/Si hollow substrate.

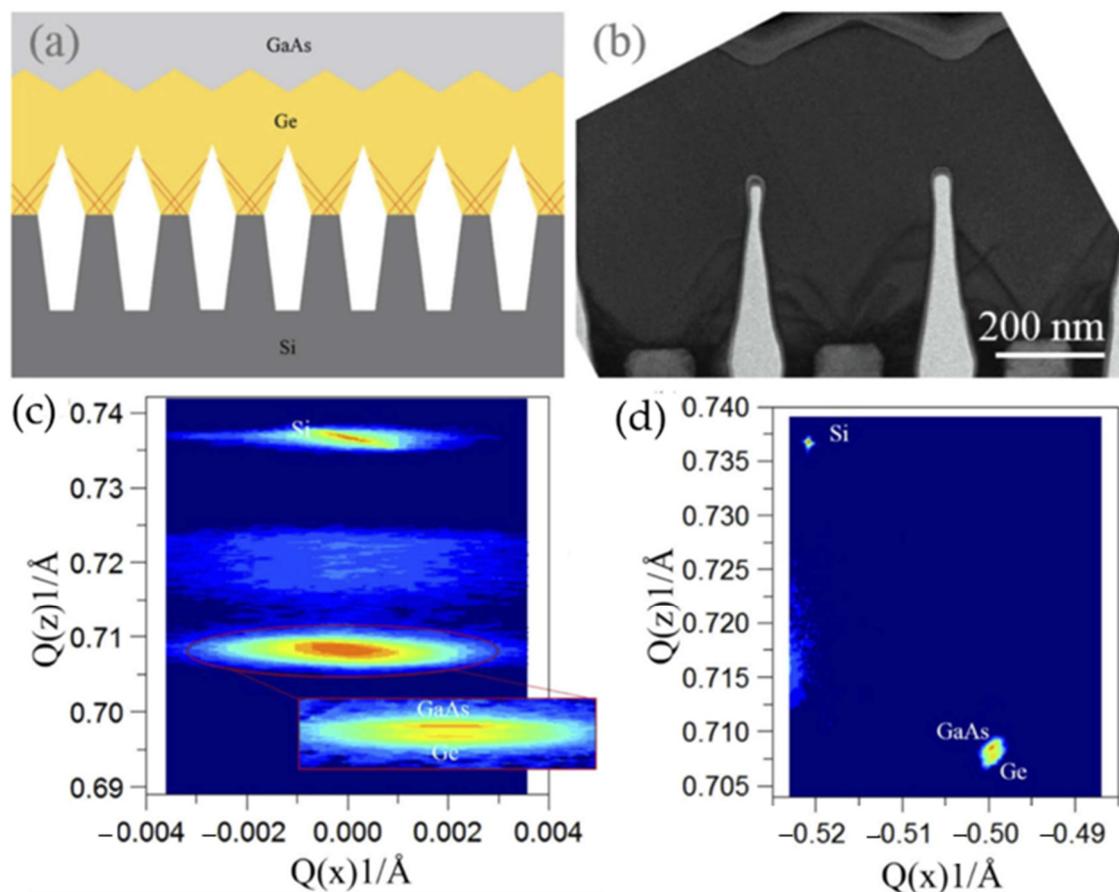


Figure 19. (a) The schematic illustration of the GaAs grown on the Ge/Si hollow substrate. It also shows the dislocation termination at the sidewalls. (b) Cross-sectional TEM image of 600 nm-thick Ge layer grown on the hollow patterned (001) Si. High-resolution XRD reciprocal-space mapping around (c) (004) and (d) $2(-)2(-)4$. Inset of (c) Higher resolution (004) map from triple-axis mode. Reprinted with permission from Reference [243] © 2020 The Optical Society.

In addition, Oh et al. [83] proposed a new scheme which controls the crack formation by using notch patterns. The periodic notches, lying along parallel or perpendicular lines, were formed on Si substrate. Because the cracks were preferentially formed at the edges of the notches acting as stress concentrators, the periodic crack arrays could be achieved, resulting in a crack-free region ($2 \times 2 \text{ mm}^2$) where 5.8 μm -thick GaAs-based solar cell structures were grown. Recently, instead of a thick GaAs buffer layer, growing a thin Ge layer on Si was proposed [143,247]. For example, Yang et al. [143] demonstrated that although a 300 nm-thick thin Ge layer replaced the conventional 1 μm -thick GaAs buffer layer for InAs/GaAs QD lasers on Si, the fabricated lasers with thin Ge buffer showed comparable performances, in terms of TDD and lasing behavior, to the conventional QD lasers with thick GaAs buffer. This indicates that the use of thin Ge buffer is beneficial for reducing the total thickness of epitaxial layer and, therefore, minimizing of crack formation.

4. Summary and Conclusions

We reviewed the recent progress on the monolithic growth of III-V on Si substrates, focusing on the GaAs and InP. The discrepancies of material property between III-V and Si lead to three major challenges: (1) antiphase (inversion) boundaries; (2) TDs; and (3) thermal cracks. In order to tackle each issue, a wide variety of strategies are discussed. For the APB-free III-V growth on Si, the offcut Si substrates, which can easily suppress the formation of APBs, were typically used before. However, together with the emerging importance of CMOS-compatibility towards monolithic integration, the use

of on-axis (001) Si substrates has become a paramount issue in III-V-on-Si heteroepitaxy. Accordingly, a few novel approaches, including V-grooved Si, MOCVD-grown GaAs or GaP on Si template, and MBE-grown Si buffer on Si, have been extensively demonstrated in recent years. To reduce the TDDs, a lot of methods, including various nucleation layer, multi-step growth buffer layer, defect filter layers, and so on, have been developed, resulting in the low TDD ($\sim 10^6 \text{ cm}^{-2}$ for GaAs). However, the InP-on-Si produces higher TDD ($\sim 10^7 \text{ cm}^{-2}$) than GaAs-on-Si, mainly due to larger lattice mismatch ($\sim 8\%$) between InP and Si. For the thermal crack issue, reducing the total thickness of epitaxial layer and minimizing the crystal imperfections (crack nucleation sites) are basic solution for hindering crack formation. However, because the crystal imperfections and thick buffer layers are inevitable in III-V/Si heteroepitaxy, various approaches using patterned substrates, Ge on patterned Si, and thin Ge buffer have been investigated.

Even though major obstacles for III-V-on-Si heteroepitaxy, such as APBs and thermal cracks, are resolved now, the quality of III-V layers on on-axis Si is still unsatisfactory for the deployment on the PICs or ICs. Compared with III-V devices on native substrates showing very low TDD ($\sim 10^4 \text{ cm}^{-2}$), it is particularly challenging to reduce the TDD of III-V devices on Si below the order of 10^6 cm^{-2} . In addition, most of III-V/Si heteroepitaxy essentially require thick buffer layers, which reduces the integration compatibility of III-V devices with other components in PICs and ICs.

Therefore, further efforts should be devoted to improving the quality of the III-V layer on Si in an integration-compatible way, in order to fully exploit the potential benefits of monolithically integrated III-V on Si-based platform. Nevertheless, an unprecedented rate of the recent development in III-V-on-Si heteroepitaxy, driven by the emerging issue of monolithic integration in Si photonics, implies that the monolithic integration of III-V on Si is likely to be realized in the near future.

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