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An Active-Clamp Forward Inverter Featuring Soft Switching and Electrical Isolation

Chien-Hsuan Chang *, Chun-An Cheng, Hung-Liang Cheng and Yen-Ting Wu

Department of Electrical Engineering, I-Shou University, Dashu District, Kaohsiung City 84001, Taiwan; cacheng@isu.edu.tw (C.-A.C.); hlcheng@isu.edu.tw (H.-L.C.); e12345678902001@gmail.com (Y.-T.W.)

* Correspondence: chchang@isu.edu.tw; Tel.: +886-7-657-7711 (ext. 6641)

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Abstract: Traditional photovoltaic (PV) grid-connection inverters with sinusoidal pulse-width modulation (SPWM) control suffer the problem of buck-typed conversion. Additional line-frequency transformers or boost converters are required to step-up output voltage, leading to low system efficiency and high circuit complexity. Therefore, many flyback inverters with electrical isolation have been proposed by adopting a flyback converter to generate a rectified sine wave, and then connecting with a bridge unfolder to control polarity. However, all energy of a flyback inverter must be temporarily stored in the magnetizing inductor of transformer so that the efficiency and the out power are limited. This paper presents a high-efficiency active-clamp forward inverter with the features of zero-voltage switching (ZVS) and electrical isolation. The proposed inverter circuit is formed by adopting a forward converter to generate a rectified sine wave, and combining with the active-clamp circuit to reset the residual magnetic flux of the transformer. Due to the boost capability of the transformer, this inverter is suitable for the PV grid-connection power systems with wide input-voltage variation. The operation principles at steady-state are analyzed, and the mathematical equations for circuit design are conducted. Finally, a laboratory prototype is built as an illustration example according to proper analysis and design. Based on the experimental results, the feasibility and satisfactory performance of the proposed inverter circuit are verified.

Keywords: photovoltaic (PV); inverter; active-clamp; zero voltage switching (ZVS); grid-connection

1. Introduction

Today, because photovoltaic (PV) energy is noiseless, pollution-free, non-radioactive and inexhaustible, PV grid-connection power systems are receiving increasing attention [1–3]. For the PV grid-connected systems, inverters are necessary to convert the DC voltage of the PV panel to an AC voltage, and then supply power in parallel with utility-line. Therefore, many experts have invested in the research of the circuit architecture and control strategy of inverters [4–7]. The full-bridge voltage-source inverter is the popular topology in low-power PV grid-connected systems. However, due to its buck-typed conversion, a line-frequency transformer has to be inserted between the inverter and utility-line. This system structure greatly increases the volume, weight and cost of the system, and reduces the power density.

Inserting a boost converter to step-up the output voltage of the PV panel is the alternative solution. The boost converter can not only regulate PV output voltage but also achieve maximum power point tracking (MPPT) [8,9]. The main advantage of this two-stage cascade structure is the independent control of the power converters. It is easy to optimize the function of each stage, and the input voltage of the inverter is regulated. However, the disadvantages are the increase in the complexity of the system circuit, the increase in cost, and the reduction in reliability. The power loss due to multiple energy processing will reduce the overall system efficiency. The pseudo-dc-link inverters are

proposed to improve these shortcomings [10,11]. In these inverters, a DC converter is used to generate a single-polarity rectified sine wave, and a line-frequency bridge unfolding circuit is used to switch the polarity of the output voltage. Since there is only single energy processing, power loss can be reduced to improve efficiency.

Among these high-efficiency inverters with pseudo-dc-link, the buck-boost type converters are widely used to implement non-isolated inverters for the photovoltaic grid-connected power system with wide-range input voltage fluctuation [12–15]. Furthermore, in order to obtain higher boosting capacity and meet the safety requirement of electrical isolation, isolated DC-DC converters, such as flyback converter, are often used to design isolated pseudo-dc-link inverters [16–19]. The flyback converter has the advantages of simple structure and easy control. However, because the transformer of the flyback converter needs to function as an inductor for energy storage, all energy needs to be temporarily stored in the transformer and then transferred to the output load, so its output power and efficiency are limited.

In order to improve the output power and conversion efficiency of the inverter with electrical isolation, the forward inverter is proposed [20], where the forward converter is adopted to replace the flyback converter and to generate a rectified sine wave. However, since the forward converter needs a third winding of the transformer to reset its residual magnetic flux, the maximum duty ratio of the power switch is limited, thereby reducing the boosting capacity of the converter. The dual-switch forward inverter [21] adds additional power switches, diodes, and a secondary winding to reset the residual magnetic flux of the transformer. The transformer can be operated in both of the first and third quadrants, but its volume and total circuit cost are greatly increased. Therefore, an active-clamp forward inverter is proposed in this paper. By replacing the traditional reset winding with an auxiliary switch and a clamp capacitor, the residual magnetic flux can be reset through the resonance of the clamp capacitor and the magnetizing inductor. In addition to recovering the energy of the magnetizing inductor back to the input, the power switch can also be turned on with zero voltage switching (ZVS) to reduce switching losses and effectively increase the efficiency of the inverter. Circuit configuration, operation principles, and design considerations will be presented sequentially in the following. Finally, a laboratory prototype of the proposed inverter is built accordingly to verify the feasibility of the proposed circuit architecture and the correctness of the theoretical analysis.

2. Circuit Configuration

As mentioned previously, the popular PV grid-connection systems need a line-frequency transformer or a boost converter to step-up output voltage. Their system block diagrams are shown in Figures 1 and 2, respectively. In order to improve efficiency and reduce cost, the pseudo-dc-link inverters are proposed, as shown in Figure 3. However, these inverters are non-isolated, which may not avoid the leakage current of the PV panel. Therefore, an active-clamp forward inverter featuring soft switching and electrical isolation is proposed in this paper.

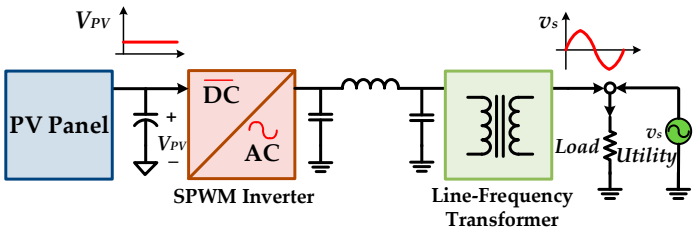


Figure 1. PV grid-connection systems with a line-frequency transformer.

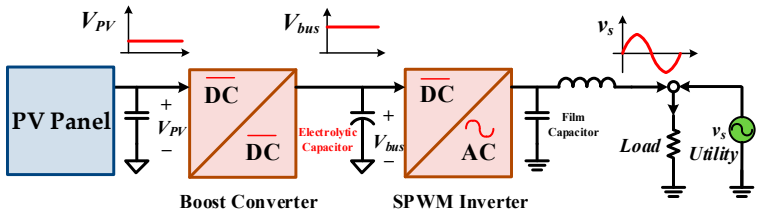


Figure 2. PV grid-connection systems with the two-stage cascade structure.

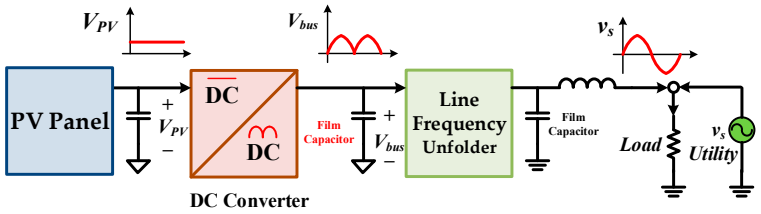


Figure 3. PV grid-connection systems with the pseudo-dc-link structure.

The circuit diagram of the proposed inverter is shown in Figure 4. The active-clamp forward converter with zero voltage switching is used to generate the single-polarity rectified sine wave, and the full-bridge unfolding circuit with line-frequency switching switches the output polarity. The power stage of the active-clamp forward converter mainly consists of the main power switch S_{m1} (including MOSFET Q_{m1}, body diode D_{m1}, and parasitic capacitor C_{ds1}), the real transformer T_{x1} (including magnetizing inductor L_{m1} and ideal transformer with turn ratio 1:n), the forward diode D_1, the freewheel diode D_2, the inductor L_1, and the output capacitor C_f. The auxiliary switch S_{a1} (including MOSFET Q_{a1} and body diode D_{a1}) and the clamp capacitor C_{c1} are used for resetting the residual magnetic flux of the transformer. The energy of the magnetizing inductor L_{m1} and the clamp capacitor C_{c1} are alternately transferred. Except for effectively recovering the energy of residual magnetic to the input power source, both the switches S_{m1} and S_{a1} can achieve ZVS characteristics to reduce switching losses. In addition, the full-bridge unfolding circuit consists of the power switches S_1, S_2, S_3 and S_4, and the output filter is formed of the inductor L_o and the capacitor C_o. The power switches S_1, S_2, S_3 and S_4 are only switching with line frequency, so that there is almost no switching loss.

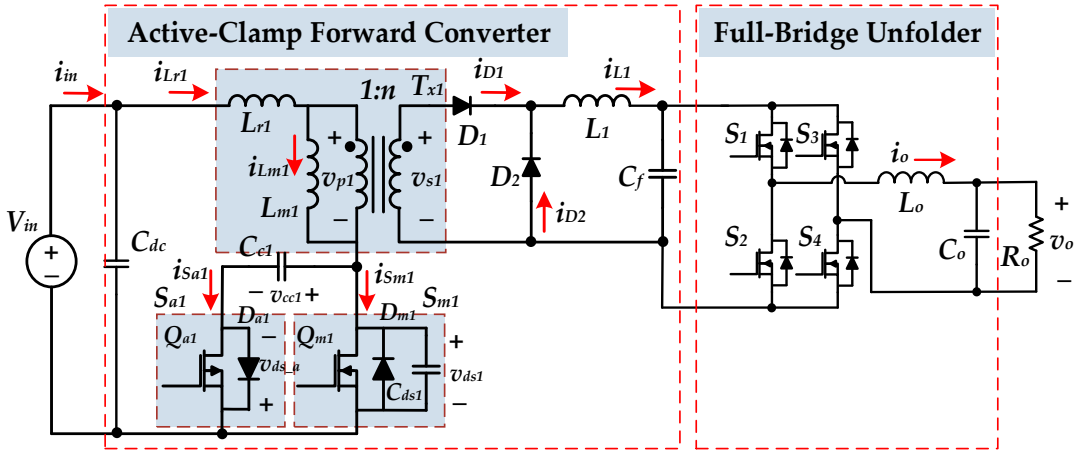


Figure 4. The circuit configuration of the proposed active-clamp forward inverter.

The traditional voltage source inverter is the buck type. In order to obtain a DC input voltage higher than the peak voltage of utility-line, an additional boost converter is necessarily adopted, resulting in low system conversion efficiency. Since the active-clamp forward inverter has both step-up and step-down functions, the boost converter is no longer required. The proposed inverter is suitable for the application with low input voltage and wide voltage variation. In addition, because partial

energy can be directly transmitted to the output during the main switch S_{m1} turning-on, the proposed inverter can effectively improve the conversion efficiency. Since only two switches S_{m1} and S_{a1} are switching with high frequency, the switching loss can be greatly reduced to improve system efficiency.

3. Operation Principles

The proposed active-clamp forward inverter is controlled by SPWM. When the inverter operates at steady state, the duty ratio of the main switch S_{m1} and the auxiliary switch S_{a1} can be respectively expressed as follows [22]:

$$d_{m1}(t) = \frac{V_M \sin \omega t}{nV_{in}}, \quad (1)$$

$$d_{a1}(t) = 1 - d_{m1}(t) = 1 - \frac{V_M \sin \omega t}{nV_{in}}. \quad (2)$$

The on-time of the main switch S_{m1} is $d_{m1}T_s$, and the on-time of the auxiliary switch S_{a1} is $(1 - d_{m1})$ T_s, where T_s is the high-frequency switching period. Assuming that the inverter operates in continuous conduction mode (CCM), when the main switch S_{m1} is turned on and the auxiliary switch S_{a1} is turned off, the voltage v_{p1} across the transformer magnetizing inductance is equal to the input voltage V_{in} and expressed as:

$$v_{p1} = V_{in}. \quad (3)$$

When the main switch S_{m1} is turned off and the auxiliary switch S_{a1} is turned on, the voltage v_{p1} across the transformer magnetizing inductance is changed to be:

$$v_{p1} = V_{in} - v_{cc1}, \quad (4)$$

where v_{cc1} is the voltage across the clamp capacitor C_{c1}. According to the volt-second balance theorem, the relationship between the input voltage V_{in} and v_{cc1} can be expressed as follows:

$$V_{in}d_{m1}T_s = (v_{cc1} - V_{in})(1 - d_{m1})T_s. \quad (5)$$

Arranging Equation (5) can get the relationship between v_{cc1} and V_{in} as:

$$v_{cc1} = \frac{1}{(1 - d_{m1})}V_{in}. \quad (6)$$

It can be found from Equation (6) that the transfer function of the voltage v_{cc1} is the same as that of the boost converter. When the main switch S_{m1} is turned off, since the auxiliary switch S_{a1} is turned on, the voltage v_{ds1} across the main switch S_{m1} is:

$$v_{ds1} = v_{cc1} = \frac{1}{(1 - d_{m1})}V_{in}. \quad (7)$$

According to the state of the switching components and the direction of their currents, the operation of the active-clamp forward inverter can be divided into nine states in one high-frequency switching period. The theoretical timing diagram of each component is shown in Figure 5, and the nine states will be described in order in the following. To simplify the circuit analysis, the following assumptions are made:

1. All components are ideal.
2. The clamp capacitor C_{c1} is much larger than the parasitic capacitor C_{ds1} of the main power switch, and the magnetizing inductor L_{m1} of the transformer is much larger than the leakage inductor L_{r1}.
3. The inductor L_1 and the capacitor C_f are large enough so that the output voltage v_o and the output current i_o can be regarded as constant in one switching period.
4. Because the dead time is extremely short, it can be ignored.

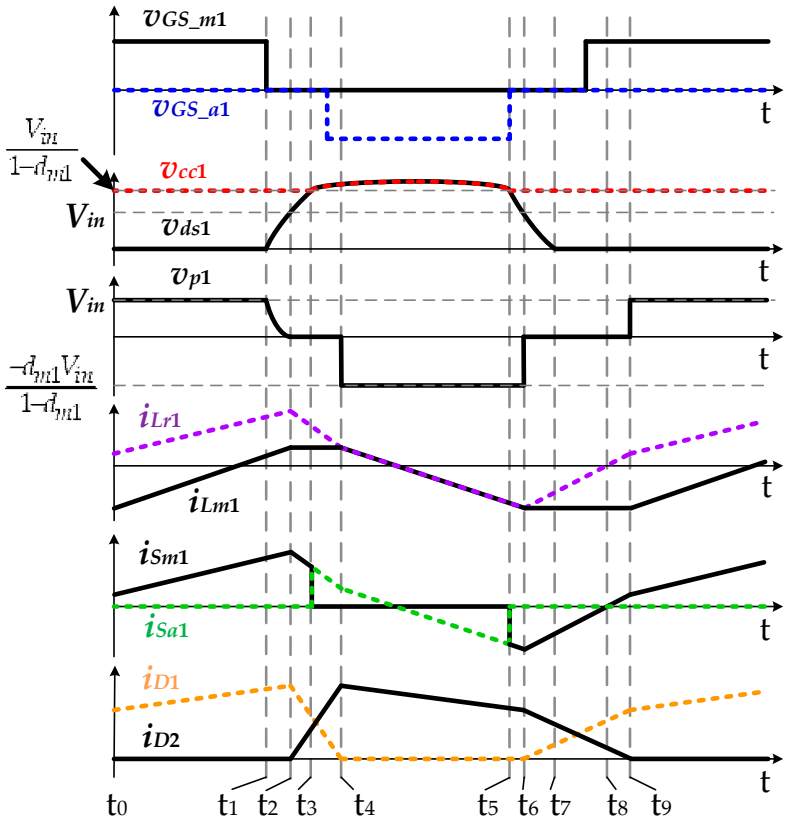


Figure 5. The theoretical timing diagram of key components in one switching period.

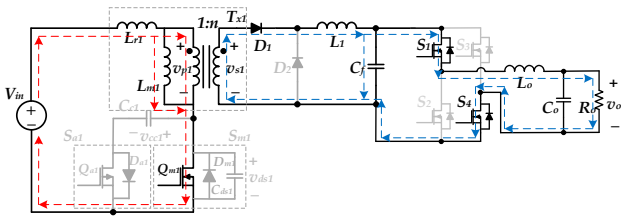
A. State 1 ($t_0 < t < t_1$, Figure 6a)

At the time $t = t_0$, the main power switch S_{m1} is turned on, and the auxiliary switch S_{a1} is turned off. At this time, the primary voltage v_{p1} across the transformer magnetizing inductor is equal to V_{in}, so the current i_{Lm1} through magnetizing inductor rises linearly. The secondary voltage v_{s1} of transformer is V_{in}/n, so the forward diode D_1 is forward biased, and the freewheel diode D_2 is reverse biased. The input power is transmitted to the inductor L_1 and the load R_o via the transformer T_{x1} and the diode D_1. The equivalent circuit is as shown in Figure 6a. The voltage v_{ds1} across the main switch S_{m1} and the current i_{Lr1} through the leakage inductor can be expressed as

$$v_{ds1}(t) = 0, \tag{8}$$

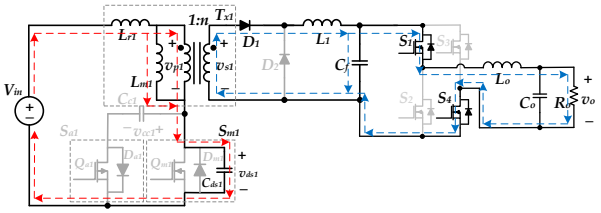
$$i_{Lr1}(t) = i_{Lm1}(t) + \frac{i_{D1}(t)}{n} = i_{Lm1}(t) + \frac{I_{Lo}}{n}, \tag{9}$$

where I_{Lo} is the average current of the output inductor L_o in one switching period. At the time $t = t_1$, the main switch S_{m1} is switched off, and the circuit operation enters the next state.



(**a**)

Figure 6. *Cont.*



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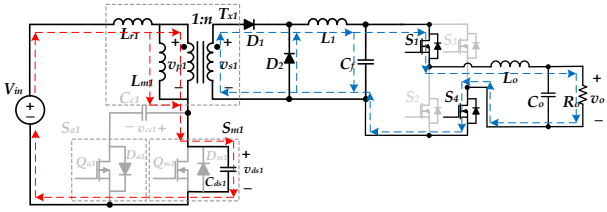

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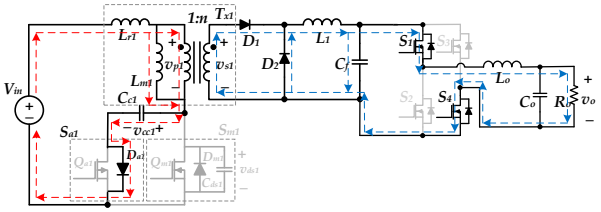

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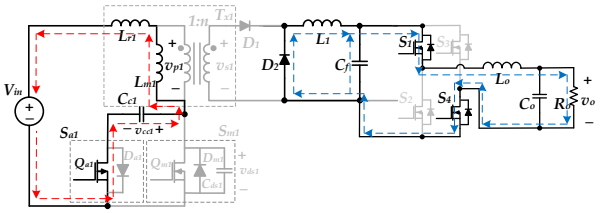

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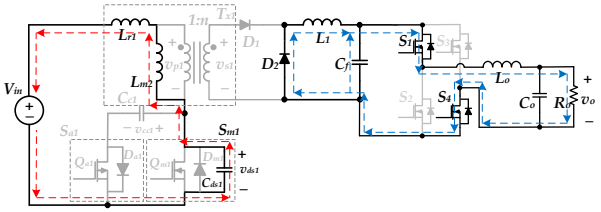
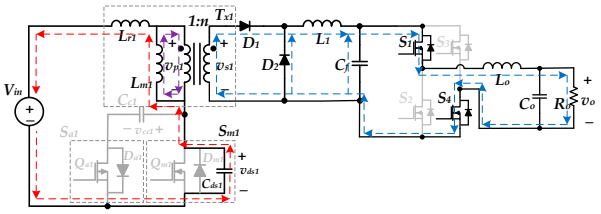
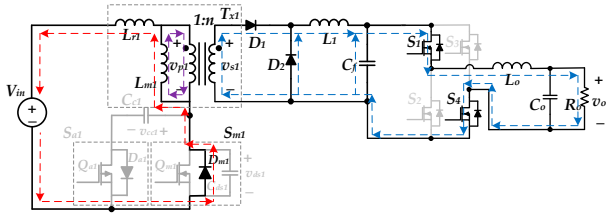


(**f**)

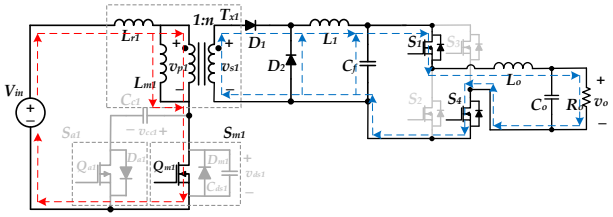


(**g**)

Figure 6. *Cont.*



(**h**)



(**i**)

Figure 6. The equivalent circuits of each operating state during the positive half line-cycle. (**a**) State 1 [$t_0 < t < t_1$], (**b**) state 2 [$t_1 < t < t_2$], (**c**) state 3 [$t_2 < t < t_3$], (**d**) state 4 [$t_3 < t < t_4$], (**e**) state 5 [$t_4 < t < t_5$], (**f**) state 6 [$t_5 < t < t_6$], (**g**) state 7 [$t_6 < t < t_7$], (**h**) state 8 [$t_7 < t < t_8$], (**i**) state 9 [$t_8 < t < t_9$].

B. *State 2 ($t_1 < t < t_2$, Figure 6b)*

When the main switch S_{m1} is switched off, the leakage inductor L_{r1}, the magnetizing inductor L_{m1}, and the parasitic capacitance C_{ds1} are resonant in series. The current i_{Lr1} of leakage inductor starts to charge the capacitor C_{ds1}, the voltage v_{ds1} starts to rise, and the primary voltage v_{p1} starts to drop. At this time, the forward diode D_1 remains on, and the freewheel diode D_2 remains off. The equivalent circuit of this state is as shown in Figure 6b. The voltage v_{ds1} across the main switch and the current i_{Lr1} through the leakage inductor can be expressed as

$$v_{ds1}(t) = V_{in}[1 - \cos\omega_1(t - t_1)] + i_{Lr1}(t)Z_1 \sin\ \omega_1(t - t_1), \tag{10}$$

$$i_{Lr1}(t) = i_{Lr1}(t_1)\cos\omega_1(t - t_1) + \frac{V_{in}}{Z_1}\sin\ \omega_1(t - t_1), \tag{11}$$

where $\omega_1 = \frac{1}{\sqrt{C_{ds1}(L_{r1}+L_{m1})}}$, and $Z_1 = \sqrt{\frac{(L_{r1}+L_{m1})}{C_{ds1}}}$. The time the state 2 required can be expressed as follows:

$$t_2 - t_1 = \frac{1}{\omega_1}\tan^{-1}\left[\frac{V_{in}}{i_{Lr1}(t_1)Z_1}\right]. \tag{12}$$

At the time $t = t_2$, v_{ds1} rises to be equal to V_{in}, this state ends and goes to the next state.

C. *State 3 ($t_2 < t < t_3$, Figure 6c)*

At the time $t = t_2$, the primary voltage v_{p1} drops to be zero, so that both the forward diode D_1 and the freewheel diode D_2 are turned on. The forward diode current i_{D1} is gradually reduced, and the freewheel diode current i_{D2} is gradually increased. The equivalent circuit is shown in Figure 6c. When the voltage v_{ds1} increases, the leakage inductor current i_{Lr1} decreases and can be expressed as:

$$i_{Lr1}(t) = \frac{i_{D1}(t)}{n} + i_{Lm1}(t). \tag{13}$$

The magnetizing current i_{Lm1} remains unchanged. At this time, the voltage v_{ds1} and the leakage inductor current i_{Lr1} can be respectively expressed as:

$$v_{ds1}(t) = V_{in} + i_{Lr1}(t_2)Z_2 \sin \omega_2(t-t_2), \tag{14}$$

$$i_{Lr1}(t) = i_{Lr1}(t_2)\cos \omega_2(t-t_2), \tag{15}$$

where $\omega_2 = \frac{1}{\sqrt{L_{r1}C_{ds1}}}$, and $Z_2 = \sqrt{\frac{L_{r1}}{C_{ds1}}}$. When the voltage v_{ds1} arrives $V_{in}/(1-d_{m1})$, the leakage inductor current i_{Lr1} stops charging the capacitor C_{ds1}, and the circuit operation enters the next state.

D. State 4 ($t_3 < t < t_4$, Figure 6d)

At the time $t = t_3$, the leakage inductor current i_{Lr1} is charging the clamp capacitor C_{C1} via the anti-parallel diode D_{a1} of the auxiliary switch S_{a1}, so the voltage across S_{a1} is zero. The equivalent circuit is shown in Figure 6d. Since the anti-parallel diode D_{a1} is turned on, the gate driving signal of the auxiliary switch S_{a1} must be provided during this state to achieve ZVS. At this time, the primary voltage v_{p1} is zero. The clamp-capacitor voltage v_{cc1} and the leakage inductor current i_{Lr1} can be expressed as

$$v_{cc1}(t) = V_{in} - [V_{in} - v_{cc1}(t_3)]\cos \omega_3(t-t_3) + i_{Lr1}(t_3)Z_3 \sin \omega_3(t-t_3), \tag{16}$$

$$i_{Lr1}(t) = i_{Lr1}(t_3)\cos \omega_3(t-t_3) + \frac{V_{in} - v_{cc1}(t_3)}{Z_3} \sin \omega_3(t-t_3), \tag{17}$$

where $\omega_3 = \frac{1}{\sqrt{L_{r1}C_{c1}}}$, and $Z_3 = \sqrt{\frac{L_{r1}}{C_{c1}}}$. When i_{Lr1} is equal to i_{Lm1}, the forward diode current i_{D1} drops to zero, and this state ends.

E. State 5 ($t_4 < t < t_5$, Figure 6e)

At the time $t = t_4$, since the forward diode current i_{D1} is zero, the magnetizing inductor L_{m1} is in series with the leakage inductor L_{r1}, and resonates with the clamping capacitor C_{c1}. The primary voltage v_{p1} is $-d_{m1}V_{in}/(1-d_{m1})$, and the equivalent circuit is as shown in Figure 6e. The leakage inductor current i_{Lr1} is equal to the magnetizing inductor current i_{Lm1} and continues decreasing. Due to the resonance, the direction of the current i_{Lm1} is reversed during this state, forcing the stored energy of the magnetizing inductor L_{m1} to be recycled to the input power source. In this state, the clamp-capacitor voltage v_{cc1} and the leakage inductor current i_{Lr1} can be expressed as

$$v_{cc1}(t) = V_{in} - [V_{in} - v_{cc1}(t_4)]\cos \omega_4(t-t_4) + i_{Lr1}(t_4)Z_4 \sin \omega_4(t-t_4), \tag{18}$$

$$i_{Lr1}(t) = i_{Lr1}(t_4)\cos \omega_4(t-t_4) + \frac{V_{in} - v_{cc1}(t_4)}{Z_4} \sin \omega_4(t-t_4), \tag{19}$$

where $\omega_4 = \frac{1}{\sqrt{(L_{r1}+L_{m1})C_{c1}}}$, and $Z_4 = \sqrt{\frac{(L_{r1}+L_{m1})}{C_{c1}}}$. This state ends when the driving signal of the auxiliary switch S_{a1} disappears.

F. State 6 ($t_5 < t < t_6$, Figure 6f)

At the time $t = t_5$, the auxiliary switch S_{a1} is turned off. The primary voltage v_{p1} is $-d_{m1}V_{in}/(1-d_{m1})$, so that the secondary voltage v_{s1} is also negative. At this time, the resonant current flows through the capacitor C_{ds1} to force it discharging, and the voltage v_{ds1} decreases. The equivalent circuit is as shown in Figure 6f. In this state, the voltage v_{ds1} and the leakage inductor current i_{Lr1} can be expressed as:

$$v_{ds1}(t) = V_{in} - [V_{in} - v_{cc1}(t_5)]\cos \omega_1(t-t_5) + i_{Lr1}(t_5)Z_1 \sin \omega_1(t-t_5), \tag{20}$$

$$i_{Lr1}(t) = i_{Lr1}(t_5)\cos\omega_1(t-t_5) + \frac{V_{in}-v_{cc1}(t_5)}{Z_1}\sin\ \omega_1(t-t_5), \tag{21}$$

where $\omega_1 = \frac{1}{\sqrt{C_{ds1}(L_{r1}+L_{m1})}}$, and $Z_1 = \sqrt{\frac{(L_{r1}+L_{m1})}{C_{ds1}}}$. This state ends when the voltage v_{ds1} drops to V_{in}, and the time it takes is as follows:

$$t_6 - t_5 = \frac{1}{\omega_1}\tan^{-1}\left[\frac{V_{in}-v_{c1}(t_5)}{Z_1 i_{Lr1}(t_5)}\right]. \tag{22}$$

G. State 7 ($t_6 < t < t_7$, Figure 6g)

At the time $t = t_6$, the voltage v_{ds1} drops to V_{in}, causing the primary voltage v_{p1} equal to zero again. The magnetizing inductor L_{m1} no longer participates in resonance, and its current remains constant. The voltage across the leakage inductor L_{r1} is V_{in}, so its current i_{Lr1} rises linearly from a negative value and with the slope of V_{in}/L_{r1}. In addition, the forward diode D_1 is turned on again, so that the current i_{D1} increases, and the freewheel diode current i_{D2} decreases. The equivalent circuit is as shown in Figure 6g. The voltage v_{ds1} across the main switch and the leakage inductor current i_{Lr1} are expressed as:

$$v_{ds1}(t) = V_{in} + i_{Lr1}(t_6)Z_2\sin\ \omega_2(t-t_6), \tag{23}$$

$$i_{Lr1}(t) = i_{Lr1}(t_6)\cos\omega_2(t-t_6), \tag{24}$$

where $\omega_2 = \frac{1}{\sqrt{L_{r1}C_{ds1}}}$, and $Z_2 = \sqrt{\frac{L_{r1}}{C_{ds1}}}$. Since the direction of the current i_{Lr1} cannot be changed instantaneously, the anti-parallel diode D_{m1} is forced to turn on, and the energy is recovered to the input. In order for the main switch S_{m1} to have the ZVS characteristic, Equation (23) should satisfy $v_{ds1}(t) \le 0$ before this state ends. The following conditions can be obtained:

$$\left|i_{Lr1}(t_6)Z_2\right| \ge V_{in}. \tag{25}$$

When the voltage v_{ds1} continues dropping to zero, this state ends and the time it takes is:

$$t_7 - t_6 = \frac{1}{\omega_2}\sin^{-1}\left[-\frac{V_{in}}{i_{Lr1}(t_6)Z_2}\right]. \tag{26}$$

H. State 8 ($t_7 < t < t_8$, Figure 6h)

At the time $t = t_7$, the current i_{Lr1} flows through the anti-parallel diode D_{m1} to release the energy stored in the magnetizing inductance L_{m1} back to the input power source, and the equivalent circuit is as shown in Figure 6h. The driving signal of the main power switch S_{m1} should be applied in this interval. Since the anti-parallel diode D_{m1} has been turned on, the switch S_{m1} can achieve the characteristic of ZVS turn-on. Because the forward diode D_1 and the freewheel diode D_2 are remained being on state, the leakage inductor current i_{Lr1} continues to increase linearly with the slope of V_{in}/L_{r1}, and can be expressed as:

$$i_{Lr1}(t) = i_{Lr1}(t_7) + \frac{V_{in}}{L_{r1}}(t-t_7). \tag{27}$$

When the current i_{Lr1} rises to be zero, this mode ends and the time it takes is:

$$t_8 - t_7 = \frac{-L_r i_{L_r}(t_7)}{V_{in}}. \tag{28}$$

I. State 9 ($t_8 < t < t_9$, Figure 6i)

At the time $t = t_8$, the leakage inductor current i_{Lr1} becomes positive. The forward diode current i_{D1} continues to increase linearly, and the freewheel diode current i_{D2} continues to decrease linearly. The equivalent circuit is shown in Figure 6i. In this state, the voltage v_{ds1} across the main switch and the leakage inductance current i_{Lr1} can be respectively expressed as:

$$v_{ds1}(t) = 0, \tag{29}$$

$$i_{Lr1}(t) = i_{Lr1}(t_8) + \frac{V_{in}}{L_{r1}}(t - t_8). \tag{30}$$

When the diode D_2 is turned off at the time $t = t_9$, the state ends, and one switching period of the proposed inverter is completed. The circuit operation will return to the state 1 of the next switching period, and the nine operation states are repeated in sequence. The time it takes for this stage is:

$$t_9 - t_8 = \frac{L_{r1}}{V_{in}}\left(\frac{I_{Lo}}{n} + i_{Lm1}(t_0) - i_{Lr1}(t_8)\right). \tag{31}$$

It can be seen from the above analyses that the advantages of the proposed inverter are listed as follows:

1. The magnetizing inductor current i_{Lm1} of the transformer is bidirectional, so the iron core is operated in the first and third quadrants of the hysteresis curve, which can improve the core utilization.
2. Replacing the traditional reset winding, the auxiliary switch S_{a1} and the clamp capacitor C_{C1} are used to reset the residual magnetic flux of the transformer. The energies of the magnetizing inductor and the clamp capacitor are mutually transferred so that the energy can be recycled to the input. Since both the magnetizing inductor and the clamping capacitor are passive components for energy storage, there is theoretically no power loss.
3. By using the magnetizing inductor and the leakage inductor of the transformer, both the main power switch S_{m1} and the auxiliary switch S_{a1} achieve the characteristics of ZVS turn-on, which can effectively reduce the switching loss.

4. Grid-Connection System and Control Circuit

The circuit diagram of a PV grid-connection power system using the proposed active clamp forward inverter is shown in Figure 7, which mainly includes a PV array, a dc-link capacitor C_{dc}, and an active clamp forward inverter, system controller, load and utility-line. The core of the system controller is the digital signal processor (DSP) dsPIC33FJ16GS504. Except for extremely fast operations, this DSP has built-in analog/digital conversion (ADC) and multiple pulse-width-modulation (PWM) control signals. Due to the Harvard structure, it can analyze load current components, and sample voltage and current signals, simultaneously. Digital design can simplify hardware circuits and reduce the number of components, resulting in small size, light weight, high flexibility and high reliability.

The main function of the PV grid-connected power system is to deliver solar energy to utility-line. Since the maximum PV power changes with sunlight intensity and temperature, the inverter output current should regulate accordingly. The control circuit diagram of the PV grid-connection power system is shown in Figure 8. By inputting the feedback voltage $V_{PV,f}$ and the feedback current $I_{PV,f}$ from the PV panel to the MPPT controller, the level of the output current command i_o^* is changed accordingly. The MPPT controller uses the perturbation & observation (P&O) algorithm [8,9] and is implemented by the DSP, which can ensure that the system can draw the maximum power from the PV panel and feed it into the utility-line. The current command i_o^* is a half-wave, and its frequency is twice the frequency of the line voltage v_s. By comparing the output current feedback signal $i_{o,f}$ with the output current command i_o^*, the obtained error signal i_{err} will adjust the SPWM switch driving signal through the compensator G_{cc}. Therefore, the output current i_o can have the same frequency and the same phase as the line voltage v_s, and the solar energy can be completely fed into the utility-line

or the load. In addition, a square wave signal v_P with the same frequency as line voltage v_s can be obtained by the phase detector, which can be used to generate the driving signal of the low-frequency bridge unfolding circuit.

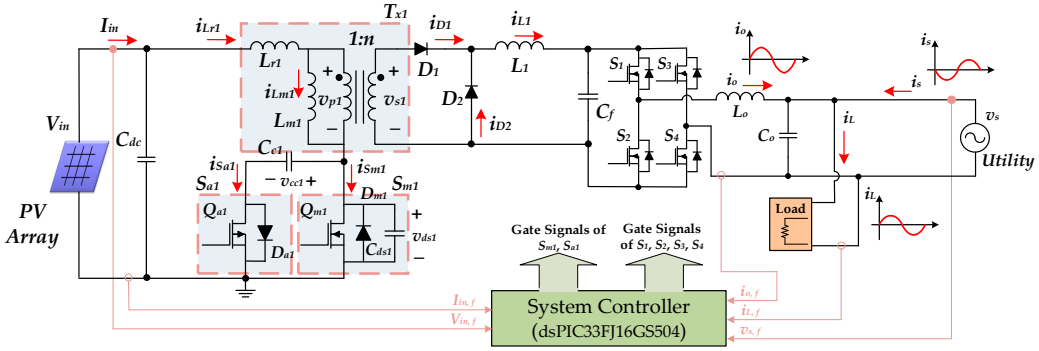


Figure 7. The circuit diagram of a grid-connection power system using the proposed active-clamp forward inverter.

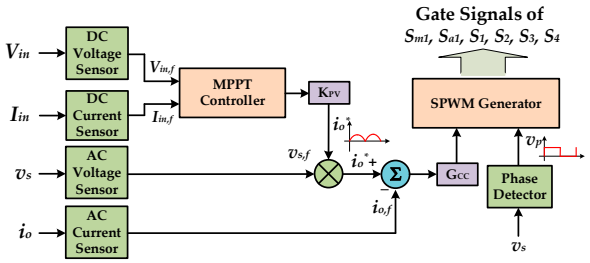


Figure 8. The block diagram of the control circuit of the PV grid-connection power system.

5. Experimental Results

According to the foregoing analysis, a DSP-based prototype of the proposed inverter is built as an example for illustration. Refer to the circuit diagram shown in Figure 7, the electrical specifications are listed in Table 1.

Table 1. Electrical specifications of the proposed inverter.

Electrical Specifications	
Typical input voltage, V_{in}	48 V
Output voltage, v_o	110 V_{rms}
Line frequency, f_{ac}	60 Hz
Switching frequency, f_s	20 kHz
Output power, P_o	400 W

Considering that the input voltage is 48 V and the peak output voltage $V_{o,p}$ is 156 V, the transformer turns ratio (n) is selected as 10. From the transfer function of the forward converter, the duty ratio can be calculated as:

$$d_{m1} = \frac{V_{o,p}}{n \times V_{in}} = 0.325. \quad (32)$$

The boundary inductance L_B of L_1 in boundary conduction mode (BCM) can be derived as:

$$L_B = \frac{V_{o,p} \times (1 - d_{m1})}{I_o \times 2 f_s}, \quad (33)$$

The inductor current is selected to operate in BCM under 20% load current and the peak of the output voltage. Therefore, the boundary inductance L_B can be calculated from Equation (33) to be

2.57 mH. This boundary value is the minimum of output inductor L_1, so the inductance of 3 mH is selected in the implementation example.

In this design, the magnetizing inductor L_{m1} of the transformer is 835 µH. From the operation principles mentioned before, the condition of that main switch S_{m1} achieves ZVS is:

$$Z_2 \geq \frac{V_{in}}{\left|i_{Lr1}(t_6)\right|}, \tag{34}$$

where $Z_2 = \sqrt{\frac{L_{r1}}{C_{ds1}}}$. From Equation (23), the current i_{Lr1} (t_6) can be obtained as:

$$i_{Lr1}(t_6) = \frac{d_{m1}V_{in}}{2L_m f_s}. \tag{35}$$

By combining Equations (34) and (35), the minimum value of the leakage inductance L_{r1} can be calculated as follows:

$$L_{r1} \geq \frac{4f_s^2 \times C_{ds1} \times L_{m1}^2}{d_{m1}^2} = 3.38(\mu H). \tag{36}$$

Choose 4 µH as the inductance of the leakage inductor L_{r1}.

Besides, the active-clamp forward inverter uses the auxiliary switch S_{a1} and the clamp capacitor C_{c1} to reset the residual magnetizing flux of the transformer. When the resonance of C_{c1}, L_{r1} and L_{m1} occurs, the small value of C_{c1} will shorten the resonant period and induce voltage spikes. As a result, the voltage stresses of the clamp capacitor C_{c1}, the main switch S_{m1}, and the auxiliary switch S_{a1} are increased. Therefore, the resonant period should be designed to be greater than ten times the main switch turn-off time, that is:

$$2\pi \times \sqrt{(L_{r1} + L_{\mathrm{m1}}) \times C_{c1}} \geq 10 \times (1 - d_{m1})T_S. \tag{37}$$

From Equation (37), the capacitance of C_{c1} can be calculated as:

$$C_{c1} \geq \frac{100 \times (1 - d_{m1})^2}{(L_{r1} + L_{m1}) \times (2\pi f_s)^2} = 3.44(\mu\mathrm{F}). \tag{38}$$

Choose 4 µF as the capacitance of the clamp capacitor C_{c1}.

According to the previous design and calculations, the selected component parameters are summarized in Table 2. The experimental results described below will be used to verify the feasibility of the proposed circuit architecture and the correctness of the theoretical analysis.

Table 2. Component parameters of the proposed inverter.

Component Parameters	
Bus filter, C_{dc}	2000 µF
Main switch, S_{m1}	6R045
Auxiliary switch, S_{a1}	47N60C3
MOSFETs, S_1–S_4	47N60C3
Diodes, D_1, D_2	C3D10060A
Transformer turn ratio, n	10
Magnetizing inductor, L_{m1}	835 µH
Leakage inductor, L_{r1}	4 µH
Clamping capacitor, C_{c1}	4 µF
Inductor, L_1	3 mH
Capacitor, C_f	4.7 µF
Output inductor, L_o	1 mH
Output capacitor, C_o	4.7 µF

The proposed active-clamp forward inverter is driven by SPWM signals. Figure 9a,b are the simulation and measured waveforms of the output voltage v_o and output current i_o when the inverter is operated at 48 V input voltage, and Figure 9c,d are the simulation and measured waveforms of the output voltage v_o and output inductor current i_{L1}. It can be seen from the figures that the output voltage and current are in the form of a sine wave with low distortion, which proves that this isolated inverter can effectively convert the DC voltage into an AC output. Furthermore, Figure 10 shows the measured waveforms of the output voltage v_o and output current i_o when the inverter operates with the step load change between 320 W and 160 W. As can be seen, the output voltage can be quickly and stably regulated to a sine wave of 110 V_{rms}, proving that the proposed inverter has good dynamic voltage regulation capability. In addition, the line regulation is 1.26%, and the load regulation is 0.78%, which meets the general specifications of ±3%.

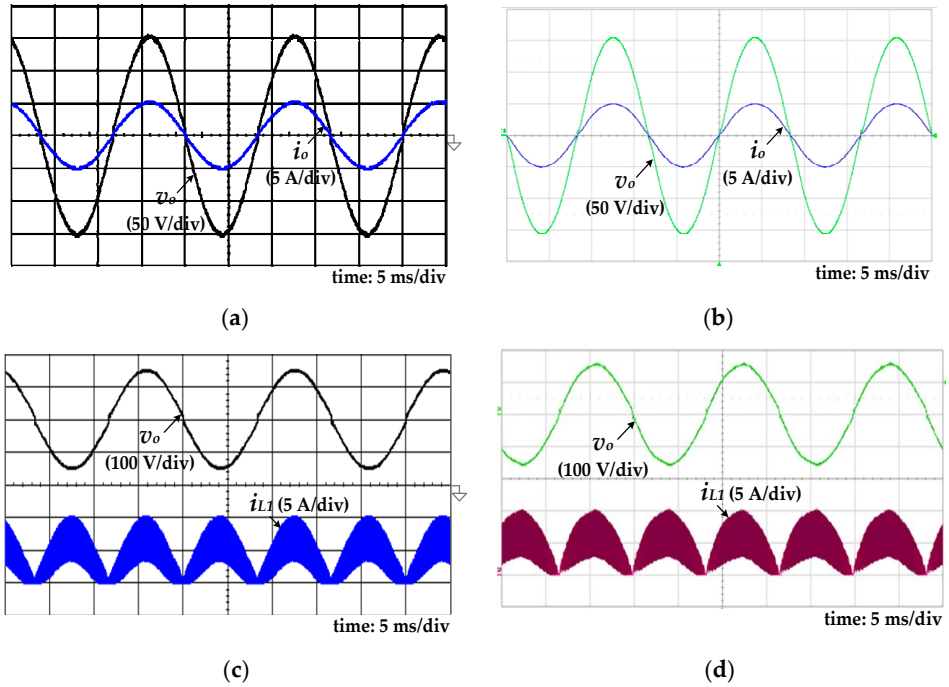


Figure 9. (**a**) Simulation waveforms of v_o and i_o, (**b**) measured waveforms of v_o and i_o, (**c**) simulation waveforms of v_o and i_{L1}, and (**d**) measured waveforms of v_o and i_{L1}, at 48 V input voltage and a full load of 400 W.

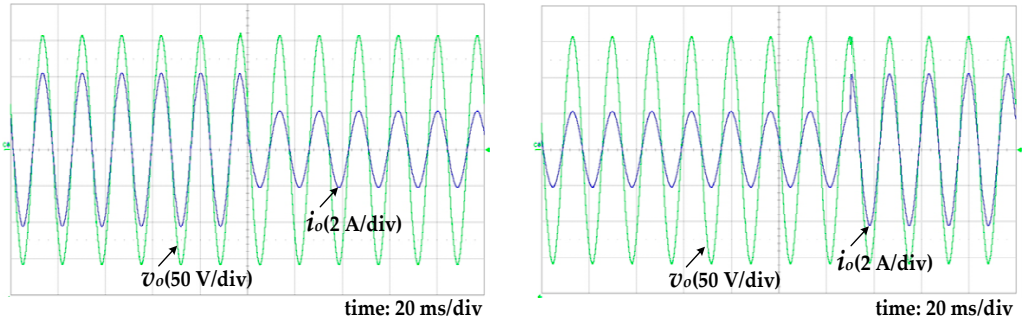


Figure 10. Measured waveforms of output voltage v_o and output current i_o when the inverter is operated with a step-load change of (**a**) from 320 W to 160 W; (**b**) from 160 W to 320 W.

Figure 11 shows the simulation and measured waveforms of the main-switch voltage v_{ds1}, the main-switch current i_{sm1}, and the clamp-capacitor voltage v_{cc1}, when the inverter is operated at 48 V

input voltage and the full load of 400 W. Since the resonant current flows through the anti-parallel diode D_{m1} before the main switch S_{m1} is turned on, it can be seen from Figure 11a,b that the main switch S_{m1} can achieve the characteristics of ZVS turn-on, which can effectively reduce switching loss. In addition, it can be seen from Figure 11c,d that the maximum value of the clamp-capacitor voltage v_{cc1} is about 95 V, which can effectively limit the voltage stress of the main power switch S_{m1}. Therefore, the power MOSFET with lower voltage rating and lower on-resistance can be selected to reduce conduction loss. Table 3 shows the total harmonic distortion (THD) and odd-order harmonics of the output voltage v_o when the inverter is operated at 48 V and 72 V input voltages. The results meet the requirements of electrical standards and verify the correctness of the theoretical analysis again. Figure 12 shows the measured efficiency curve of the active-clamp forward inverter. The highest efficiency is 90.2% at 48 V input and 91.5% at 72 V input, respectively.

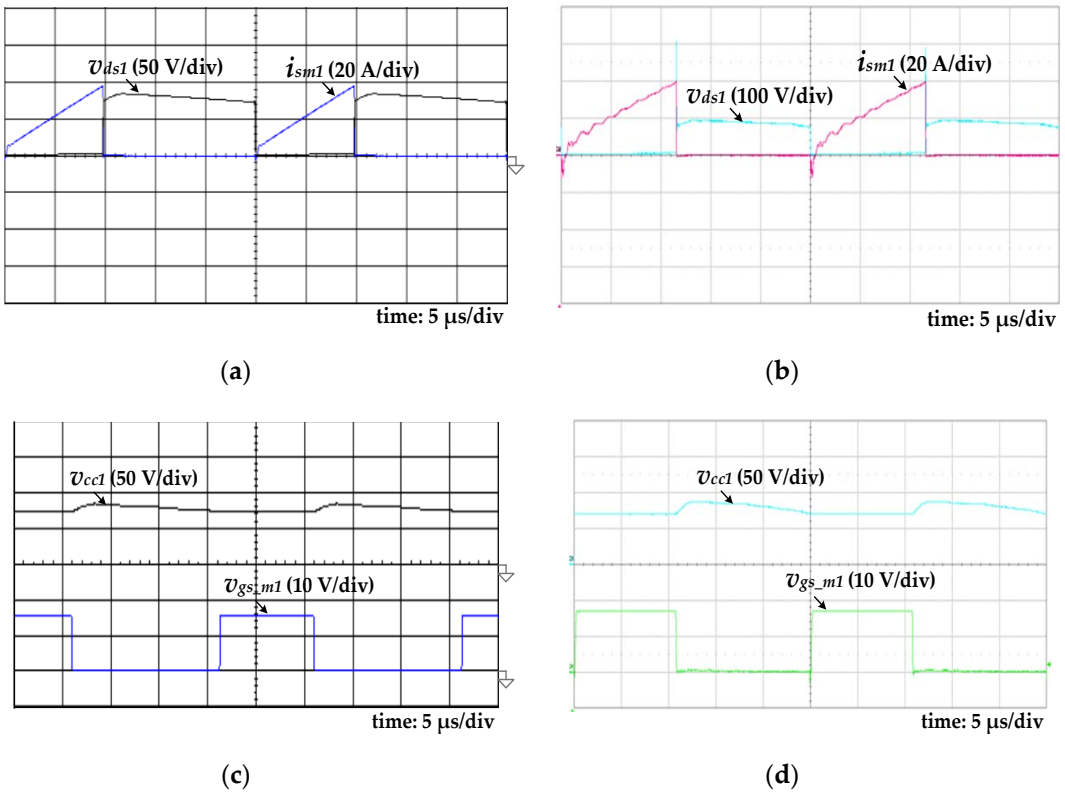


Figure 11. (**a**) Simulation waveforms of v_{ds1} and i_{sm1}, (**b**) measured waveforms of v_{ds1} and i_{sm1}, (**c**) simulation waveforms of v_{cc1} and v_{GS_m1}, and (**d**) measured waveforms of v_{cc1} and v_{GS_m1}, when the inverter is operated at the full load of 400 W.

Table 3. Measured T.H.D. and odd-order harmonics of the output voltage.

Harmonics	48 V	72 V
T.H.D.	2.59%	1.47%
3rd Harmonic	2.42%	1.32%
5th Harmonic	0.83%	0.48%
7th Harmonic	0.32%	0.29%
9th Harmonic	0.18%	0.25%
11th Harmonic	0.15%	0.18%

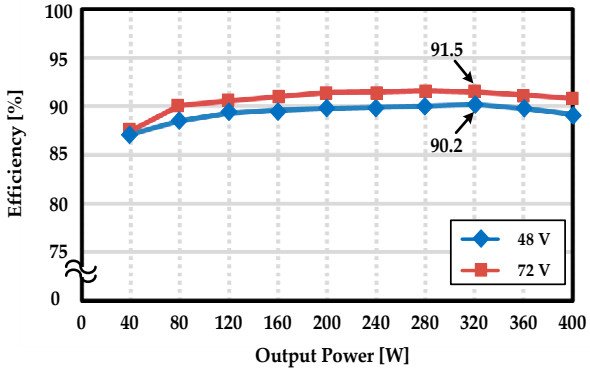


Figure 12. Measured efficiency curve of the active-clamp forward inverter.

Furthermore, Figure 13 shows the measured waveforms of the load current i_L, the inverter output current i_o, the utility-line current i_s and the utility-line voltage v_s, under the operation of grid-connection mode. In this case, the inverter output current i_o is controlled to follow the frequency and the phase of the utility-line voltage v_s. In this way, the power of the PV panel can be delivered to the load and the utility-line by the proposed active-clamp forward inverter. It can be clearly seen from Figure 13 that the output current is close to an ideal sine wave and in phase with the utility-line voltage. At this condition, the inverter outputs about 200 W of power, and utility-line provides approximately 200 W of power to meet the total power requirement of the load. It can prove the feasibility of grid-connection of the proposed inverter. In addition, the power factor, the THD and odd-order harmonics of the output current are measured and recorded in Table 4. Either the THD or each harmonic can meet the specification requirements, and the power factor reaches 0.994. This further confirms the feasibility of the circuit structure and control strategy mentioned in this paper.

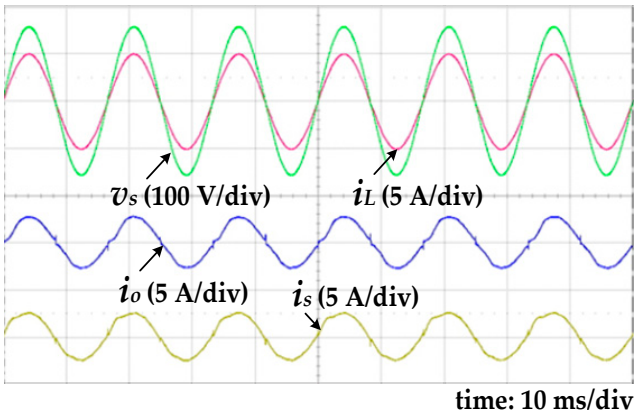


Figure 13. Measured waveforms of the load current i_L, the inverter output current i_o, utility-line current i_s and utility-line voltage vs. during grid-connection operation.

Table 4. Measured power factor, T.H.D. and odd-order harmonics of the output current during grid-connection mode.

Power Factor 0.994	
T.H.D.	2.23%
3rd Harmonic	1.92%
5th Harmonic	0.83%
7th Harmonic	0.65%
9th Harmonic	0.34%
11th Harmonic	0.21%

Many pseudo-dc-link inverters based on forward converters are proposed to improve conversion efficiency and to achieve electrical isolation [20,21]. In order to compare the difference between them and the proposed forward inverter in this paper, a brief discussion is presented as follows according to (1) the reset circuit for residual magnetic flux, (2) the conversion efficiency, (3) the characteristic of switch, and (4) the circuit complexity.

(1) Reset circuit for residual magnetic flux The forward inverter in Reference [20] needs a third winding in series with a diode to reset the residual magnetic flux. Therefore, the maximum duty ratio is limited, resulting in a reduction of boosting capacity. The dual-switch forward inverter in Reference [21] adds an additional power switch and a diode to reset the residual magnetic flux. Since the input current goes through these devices, the volume and cost are greatly increased. In the proposed active-clamp forward inverter, an auxiliary switch and a clamp capacitor are used to reset the residual magnetic flux through the resonance of the clamp capacitor and the magnetizing inductor, which can avoid the problems mentioned above.

(2) Conversion efficiency According to the efficiency curve shown in Figure 12, the efficiency of the active-clamp forward inverter is up to 90.2% at 48 V input and 400 W output power. The measured efficiency of the forward inverter in Reference [20] is 89.5% at 45 V input and 110 W. Besides, the measured efficiency of the dual-switch forward inverter in Reference [21] is only 82% at full load. Therefore, it can be concluded that the proposed inverter has better conversion efficiency than other forward inverters.

(3) Characteristic of switch In the proposed active-clamp forward inverter, both of the main switch and the auxiliary switch have the characteristic of ZVS turn-on. In addition to reducing switching losses, switching noise can also be reduced to avoid electromagnetic interference (EMI) problems. For the forward inverters proposed in References [20,21], the power switches are hard switching, which may increase switching loss and cause serious EMI issues.

(4) Circuit complexity In order to reduce the core size of the transformer, multiple converters with interleaved parallel connections are used in the forward inverter in Reference [20]. Although the efficiency is improved slightly, the circuit complexity and cost are increased significantly. Besides, two dual-switch forward converters are parallel connected in the inverter of Reference [21], and each secondary side of the transformer is center tap, resulting in high circuit complexity. The proposed inverter uses only a single active-clamp forward converter and does not need to add a third winding, so its circuit architecture is much simpler than other forward inverters.

6. Conclusions

A single-phase active-clamp forward inverter has been successfully developed and implemented in this paper. The active-clamp forward converter is controlled by SPWM to generate a rectified sine wave, and the full-bridge unfolding circuit with line-frequency switching is used to switch output polarity. This is because only one main switch and one auxiliary switch perform high-frequency switching, and both of them have ZVS turn-on characteristics, which can effectively reduce switching losses and improve efficiency. An auxiliary switch and a clamp capacitor are used to reset the residual magnetic flux of the transformer, so it can recover the energy of the magnetizing inductor to the input, effectively improving the conversion efficiency. The proposed inverter has a transformer so that it can meet the safety requirements of electrical isolation, and has voltage boost capacity suitable for PV power systems. A DSP chip is used instead of a large number of analog components to implement a compact and programmable control circuit. The experimental results have really verified the feasibility of the proposed active-clamp forward inverter. This inverter can be applied to the PV grid-connection power system, which helps to promote the development of renewable energy.

Author Contributions: C.-H.C. and C.-A.C. conceived and designed the circuit; H.-L.C. performed circuit simulations; Y.-T.W. carried out the prototype of the proposed inverter, and measured as well as analyzed experimental results with the guidance from C.-H.C.; C.-A.C. revised the manuscript for submission. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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