

Article

# Development of 340-GHz Transceiver Front End Based on GaAs Monolithic Integration Technology for THz Active Imaging Array

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**Abstract:** Frequency multipliers and mixers based on Schottky barrier diodes (SBDs) are widely used in terahertz (THz) imaging applications. However, they still face obstacles, such as poor performance consistency caused by discrete flip-chip diodes, as well as low efficiency and large receiving noise temperature. It is very hard to meet the requirement of multiple channels in THz imaging array. In order to solve this problem, 12- $\mu\text{m}$ -thick gallium arsenide (GaAs) monolithic integrated technology was adopted. In the process, the diode chip shared the same GaAs substrate with the transmission line, and the diode's pads were seamlessly connected to the transmission line without using silver glue. A three-dimensional (3D) electromagnetic (EM) model of the diode chip was established in Ansys High Frequency Structure Simulator (HFSS) to accurately characterize the parasitic parameters. Based on the model, by quantitatively analyzing the influence of the surface channel width and the diode anode junction area on the best efficiency, the final parameters and dimensions of the diode were further optimized and determined. Finally, three 0.34 THz triplers and subharmonic mixers (SHMs) were manufactured, assembled, and measured for demonstration, all of which comprised a waveguide housing, a GaAs circuit integrated with diodes, and other external connectors. Experimental results show that all the triplers and SHMs had great performance consistency. Typically, when the input power was 100 mW, the output power of the THz tripler was greater than 1 mW in the frequency range of 324 GHz to 352 GHz, and a peak efficiency of 6.8% was achieved at 338 GHz. The THz SHM exhibited quite a low double sideband (DSB) noise temperature of 900~1500 K and a DSB conversion loss of 6.9~9 dB over the frequency range of 325~352 GHz. It is indicated that the GaAs monolithic integrated process, diodes modeling, and circuits simulation method in this paper provide an effective way to design THz frequency multiplier and mixer circuits.

**Keywords:** terahertz (THz); GaAs monolithic integrated circuits; tripler; subharmonic mixer (SHM); Schottky barrier diodes (SBDs)

## 1. Introduction

Over the past few decades, various terahertz (THz) technologies have been developed rapidly. Among them, THz imaging and sensing technology have broad application prospects in science and other fields, such as safety and security screening, process monitoring, non-contact material testing, radio astronomy, and earth observation [1–9]. In recent years, many active or passive imaging

systems based on all-solid-state electronics technology have been reported at the submillimeter and THz band [9–15]. Transmitters with sufficient output power are inevitably required for active imagers, and the core device is usually frequency multipliers. Low-noise and broadband receivers are necessarily needed in THz imaging systems. These receivers are mainly based on Schottky diodes or III/V compound semiconductor transistors.

THz sources based on gallium nitride (GaN) or complementary metal oxide semiconductor (CMOS) technology have been widely studied. GaN Schottky diode-based sources show better performance in high power dissipation, up to 1.1 W, but the efficiency is much lower than that of GaAs-based circuits [16,17]. THz sources based on silicon/SiGe CMOS around 300 GHz have also been reported, which generally show great advantages of high integration. However, the maximum output power of only  $-4.6$  dBm and  $-6.5$  dBm and optimum efficiency of only 1.4% and 0.052% are presented, respectively [18,19]. THz sources based on Schottky diodes possess many advantages, including compactness, broadband, frequency stability, temperature stability, and capability of room temperature operation [20–22]. In recent years, remarkable progress has been made in the field of solid-state THz sources based on planar Schottky diodes. In pursuit of high working frequency, a tripler operating from 2.5 to 2.7 THz was reported by Jet Propulsion Laboratory [23]. In terms of high efficiency, a 220 GHz tripler with a peak efficiency of 16% was reported by Virginia Diodes, Inc. [24]. However, discrete GaAs Schottky varactor diode chips are used in [24]. Since the highly consistent performance of the circuits is a big concern for subsequent research on active radar imaging arrays, GaAs monolithic integrated diode chips are preferred to design THz triplers.

THz subharmonic mixers (SHMs) based on GaAs Schottky diodes have also been rapidly developed due to the advantage of low noise and broadband performance at room temperature [25–28]. They directly help improve the signal-to-noise rate (SNR) of the entire receiver, especially when there is no proper wideband THz low noise amplifier (LNA) in the system. In [29], a 190–240 GHz Schottky-diode SHM with lower than 1500 K noise temperature is presented. However, the use of flip-chip anti-parallel Schottky diodes may no longer be suitable for higher frequency THz mixers, which face the problems of poor alignment and position uncertainty of the diode and the passive circuits. Therefore, GaAs monolithic integrated technology is an effective and necessary alternative when the operating frequency exceeds 300 GHz.

In this paper, 0.34 THz triplers and SHMs based on GaAs Schottky diodes are proposed for THz active imaging applications. The tripler and mixer are used as the solid-state transmitter and receiver front end, respectively. First, the GaAs process, diodes modeling, and the development of 0.34 THz triplers and SHMs are described in detail in Section 2. Compared with the traditional method of mounting discrete diodes on circuits, the 12- $\mu$ m-thick GaAs monolithic integrated process in this paper reduces manual assembly errors, lowers the defective rate, and improves performance consistency. Moreover, when the frequency goes beyond 0.3 THz, the parasitic parameters introduced by the physical geometry of the Schottky diodes have a non-negligible effect on the frequency conversion efficiency of either multipliers or mixers. To address this issue, a 3D EM model of the diode chip is established in HFSS software to accurately characterize the parasitic parameters. Based on the 3D EM model and the co-simulation method, by analyzing different surface channel widths and anode junction areas, the best frequency conversion efficiency can be obtained, thereby finally determining the dimension of the diode chip. The approach adopted in this paper is a combination of 3D full-wave EM simulation and harmonic balanced simulation. Measurements and results about the output capacity of the triplers and the noise temperature of the SHMs agree well with the simulation results.

## 2. Materials and Methods

### 2.1. Schottky Diodes

As a crucial component in THz multipliers and mixers, GaAs Schottky barrier diodes SBDs were developed first. In this paper, the 12- $\mu$ m-thick GaAs monolithic integrated technology was jointly

developed by the University of Electronic Science and Technology of China (UESTC) and Hebei Semiconductor Research Institute, Shijiazhuang. The main physical and electrical diode parameters for the 0.34 THz tripler and the 0.34 THz mixer are listed in Tables 1 and 2, respectively. Typical cut-off frequency ( $f_T$ ) is also given, which is defined as  $1/(2\pi R_s C_{j0})$ , where  $R_s$  and  $C_{j0}$  represent series resistance and zero-bias junction capacitance of the Schottky-barrier diode, respectively. A detailed description is given about the process and design of the 4-die diode chip for the tripler, and that of the anti-parallel diode chip for the mixer was similar.

**Table 1.** Physical and electrical diode parameters of the 0.34 terahertz (THz) tripler.

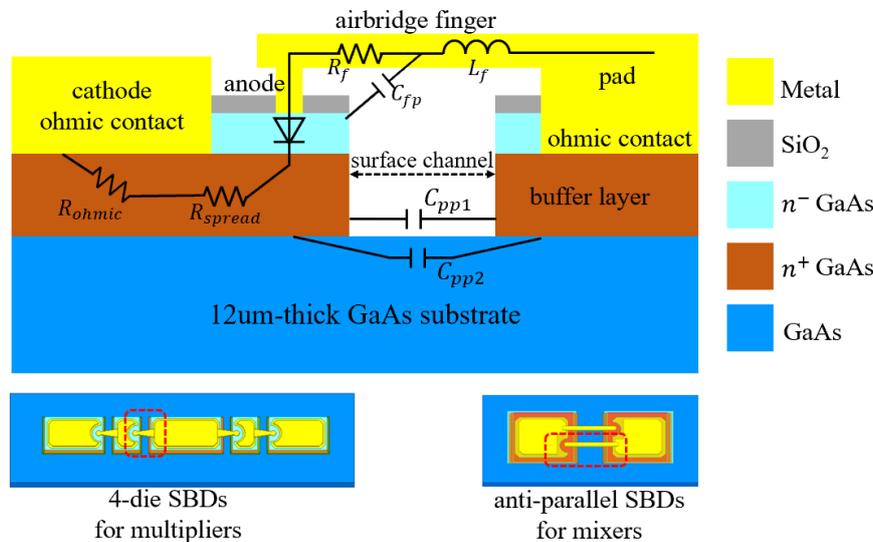
Physical Parameters	Electrical Parameters	
Epilayer doping = $2 \times 10^{17} \text{ cm}^{-3}$	Junction potential ( $V_j$ )	0.9 V
Epilayer thickness = $0.3 \text{ }\mu\text{m}$	Zero-bias junction capacitance ( $C_{j0}$ )	16 fF
N+ layer doping = $5 \times 10^{18} \text{ cm}^{-3}$	Series resistance per anode ( $R_s$ )	6 $\Omega$
N+ layer thickness = $3.5 \text{ }\mu\text{m}$	Reverse saturation current ( $I_{sat}$ )	$2 \times 10^{-17} \text{ A}$
Anode radius = $1.8 \text{ }\mu\text{m}$	Reverse breakdown voltage ( $V_{br}$ )	−9.6 V
SiO <sub>2</sub> layer thickness = $0.5 \text{ }\mu\text{m}$	Reverse breakdown current ( $I_{br}$ )	−10 $\mu\text{A}$
Substrate thickness = $12 \text{ }\mu\text{m}$	Ideality factor per anode ( $\eta$ )	1.2
Chip length = $224 \text{ }\mu\text{m}$	Grading coefficient (M)	0.5
Chip width = $28 \text{ }\mu\text{m}$	Typical cut-off frequency ( $f_T$ )	1.5 THz
Chip height = $6.3 \text{ }\mu\text{m}$		

**Table 2.** Physical and electrical diode parameters of the 0.34 THz mixer.

Physical Parameters	Electrical Parameters	
Epilayer doping = $2 \times 10^{17} \text{ cm}^{-3}$	Junction potential ( $V_j$ )	0.9 V
Epilayer thickness = $0.1 \text{ }\mu\text{m}$	Zero-bias junction capacitance ( $C_{j0}$ )	2 fF
N+ layer doping = $5 \times 10^{18} \text{ cm}^{-3}$	Series resistance per anode ( $R_s$ )	7 $\Omega$
N+ layer thickness = $3 \text{ }\mu\text{m}$	Reverse saturation current ( $I_{sat}$ )	30 fA
Anode radius = $0.55 \text{ }\mu\text{m}$	Reverse breakdown voltage ( $V_{br}$ )	−9.6 V
SiO <sub>2</sub> layer thickness = $0.5 \text{ }\mu\text{m}$	Reverse breakdown current ( $I_{br}$ )	−10 $\mu\text{A}$
Substrate thickness = $12 \text{ }\mu\text{m}$	Ideality factor per anode ( $\eta$ )	1.2
Chip length = $220 \text{ }\mu\text{m}$	Grading coefficient (M)	0.5
Chip width = $70 \text{ }\mu\text{m}$	Typical cut-off frequency ( $f_T$ )	10 THz
Chip height = $6 \text{ }\mu\text{m}$		

Active layers ( $n^-$  GaAs epitaxial layer and the highly doped  $n^+$  GaAs buffer layer) were built on the semi-insulating (SI) GaAs substrate with a thickness of  $12 \text{ }\mu\text{m}$ . The doping concentration of the GaAs buffer layer was  $5 \times 10^{18} \text{ cm}^{-3}$ , which created conditions for the ohmic contact between the cathode and the active layer. The thickness of the buffer layer was  $3.5 \text{ }\mu\text{m}$ , which was slightly larger than the skin depth at the operating frequency. The thickness of the epilayer was set to  $0.3 \text{ }\mu\text{m}$ , which was slightly larger than the thickness of the depletion layer under the reverse breakdown voltage to avoid introducing more series resistance. The cylindrical anode was formed on the epitaxial layer, resulting in the Schottky contact. The anode radius was  $1.8 \text{ }\mu\text{m}$  (corresponding to an area of  $10.8 \text{ }\mu\text{m}^2$ ), which is a key parameter for designing tripler and will be discussed later. The SiO<sub>2</sub> layer was deposited on the epitaxial layer to protect the epilayer. The SiO<sub>2</sub> passivation layer introduced parasitic parameters, and the smaller the thickness, the smaller the parasitic parameters introduced. According to the process conditions, the thickness of the oxide layer was determined to be  $0.5 \text{ }\mu\text{m}$ . The cathode pad and the metal layer of the transmission line were realized and connected by electroplating with a thickness of  $1 \text{ }\mu\text{m}$ . A straight surface channel was etched to lower parasitic capacitance, as shown in Figure 1. The spacing between the two straight mesas was  $8.5 \text{ }\mu\text{m}$ , which is elaborated later in this paper. In addition, the overall size of the 4-die diode chip was  $224 \text{ }\mu\text{m}$  in length,  $28 \text{ }\mu\text{m}$  in width,

and 6.3  $\mu\text{m}$  in height, not counting the thickness of the substrate. It was essential to use those physical parameters to build a three-dimensional modeling of the diode.



**Figure 1.** The cross-sectional view of the planar Schottky diode and a simplified equivalent circuit model.

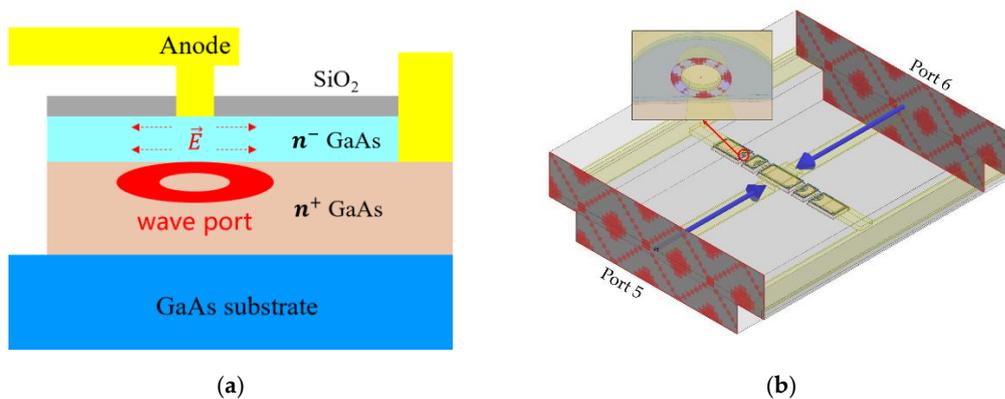
In terms of lumped equivalent circuits, a large amount of literature is available on the modeling of Schottky diodes in millimeter and submillimeter waves operating at room temperature [30–33]. For this design, a simplified equivalent circuit model was used, which is marked on the cross-sectional view in Figure 1. The Schottky junction is represented by a diode symbol, modeled as voltage-dependent junction capacitance ( $C_j$ ) and resistance ( $R_j$ ). The diode's series resistance ( $R_s$ ) consists of airbridge finger resistance ( $R_f$ ), buffer-layer spreading resistance ( $R_{spread}$ ), ohmic-contact resistance ( $R_{ohmic}$ ), and top junction epi-layer resistance. Several parasitic elements were used to characterize parasitic coupling effects dependent of the diode geometry, where the magnetic field coupling within the airbridge finger was modeled as  $L_f$  and electric field coupling near the surface channel was modeled as  $C_{pp1}$ ,  $C_{pp2}$ , and  $C_{fp}$ . Based on these equivalent circuit components, the electrical parameters obtained through measurements are shown in Tables 1 and 2. The equivalent model of the diode had to be slightly different, depending on the specific application. For multipliers, nonlinear junction capacitance  $C_{j0}$  played a leading role, which could be improved by properly increasing the anode junction area and reducing the doping concentration of the epitaxial layer. However, mixers were more dependent on the nonlinear resistance characteristics of the diode junction because broadband impedance matching was easier to achieve when nonlinear resistance dominated. Additionally, the HFSS 3D model of the diode is presented at the bottom of Figure 1, including anti-series 4-die SBDs for 0.34 THz triplers and anti-parallel SBDs for 0.34 THz SHMs.

## 2.2. Geometry Optimization of Diodes

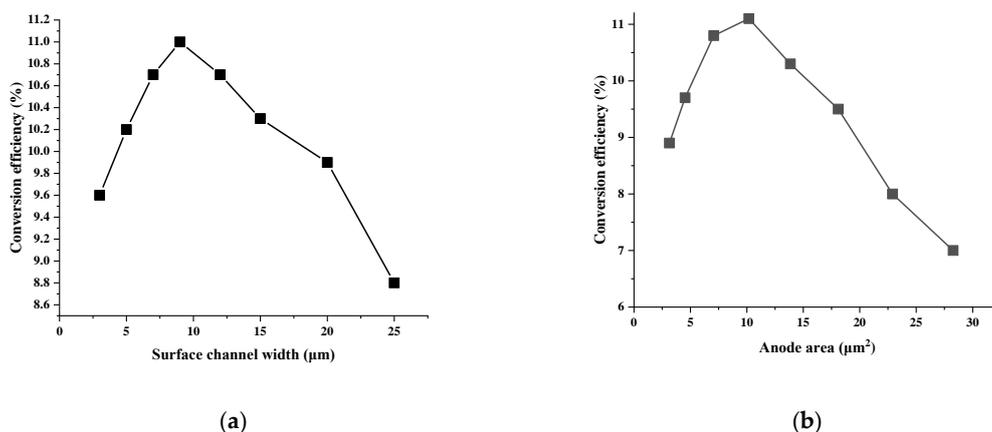
For a given input power and frequency, the best frequency multiplication efficiency varied with the geometry size of the diode, as well as bias conditions of direct current (DC). As shown in Figure 1, the surface channel was approximately equivalent to a plate capacitor and the air bridge finger mainly introduced inductance. When the width increased,  $C_{pp}$  decreased and  $L_f$  increased. On the contrary,  $C_{pp}$  increased and  $L_f$  decreased. Excessive inductance or capacitance increased the difficulty of impedance matching and reduced the cut-off frequency of the diode, thereby degrading the performance of the diode. Moreover,  $R_j$  and  $C_j$  were intrinsic parameters for representing the nonlinear effect of anode junction and they were also contradictory. When one parameter changed with the area of the anode junction, the other parameter changed in the opposite direction. Therefore, the diode geometry had

to be optimized to achieve optimal multiplication efficiency. The area of the anode junction and the width of the surface channel were the main optimization objects.

The schematic diagram of the wave port configuration of the diode anode junction and the setup for high-frequency 3D EM simulations is shown in Figure 2. Each diode’s wave port was defined as a miniature coaxial hollow ring piece surrounding the anode, as illustrated in Figure 2a. The electromagnetic field around the anode junction was calculated with HFSS. The gap between the edge of the anode and the coaxial hollow ring piece must be very narrow to avoid underestimating the parasitic capacitance [34]. The 4-die diode chip was embedded in the suspended microstrip line with both ends of the diode extended toward the two wave ports, numbered as 5 and 6, as shown in Figure 2b. The effect of the transmission line was removed by de-embedding the wave port to the diode chip. Thus, the 3D EM simulation model was set up and measured by the six wave ports. Using the obtained linear S-parameter results already considered the parasitic effects caused by the diode geometry, which is represented by the several parasitic elements in Figure 1. Harmonic balance simulation was then performed in Keysight Advanced Design System (ADS) to calculate the conversion efficiency. Finally, parametric sweep simulations were conducted for the circuit’s optimum performance under a specific channel width and anode junction area. The optimization results are shown in Figure 3a,b, from which we can see the best surface channel width of 8.5  $\mu\text{m}$  and anode junction area of 10  $\mu\text{m}^2$ .



**Figure 2.** Schematic diagram of (a) wave port configuration of diode anode junction and (b) setup for high-frequency 3D EM simulations.

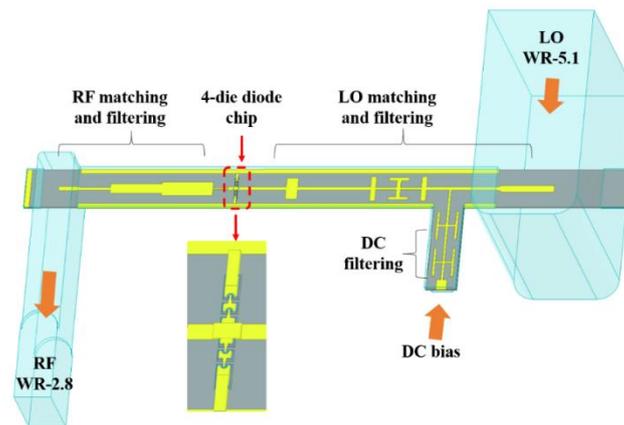


**Figure 3.** Simulated optimum conversion efficiency with (a) different surface channel widths and (b) different anode junction areas.

### 2.3. 0.34 THz Tripler Development

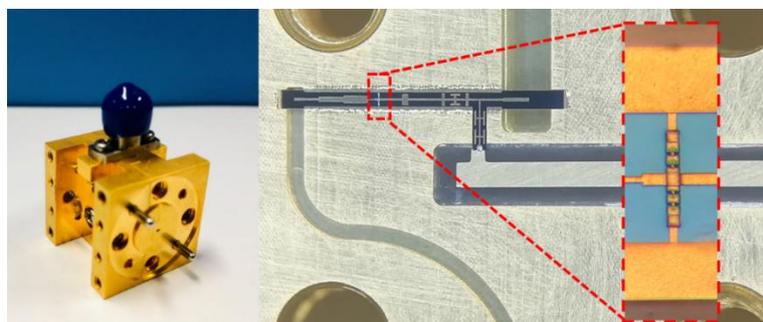
With the geometrically optimized diode chip, a 0.34 THz tripler using GaAs monolithic technology was proposed. The detailed circuit configuration is shown in Figure 4. It can be seen from the figure

that the whole circuit was functionally divided into three parts. The 4-die diode chip generated the fundamental wave and the harmonics. The local oscillator (LO) matching and filtering part consisted of a LO transition probe for input, a filter based on a compact microstrip resonant cell (CMRC) for harmonics energy recovery, a CMRC filter for DC bias, and an intermediate matching circuit to make the input fundamental energy fed into the diode chip as much as possible. Similarly, the radio frequency (RF) matching and filtering part was optimized to maximize the output of the third harmonic. All linear circuit structures, including filters and matching networks, were simulated and designed in HFSS. S-parameter files with seven ports were then imported into ADS for harmonic balance simulation. After several iterations of co-simulation and optimization, the tripler circuit was finalized to suffice requirements, as shown in Figure 4.



**Figure 4.** Circuit configuration of the proposed 0.34 THz tripler in HFSS.

A photograph of the fabricated THz GaAs monolithic integrated tripler circuit within a split block is shown in Figure 5. As can be seen, the 4-die SBDs were integrated with the matching circuits, and the whole tripler circuit was fixed on the block through the beam lead. Due to the large relative dielectric constant of gallium arsenide, it was impractical to connect the tiny DC feeder circuit directly to the external subminiature version A (SMA) connector. Therefore, the transition circuit on Rogers RT/duroid 5880 was fabricated and connected to the GaAs circuit through silver glue. The zoomed view of the diode chip was given as proof that the monolithic integrated diode technology eliminated the manual assembly errors that may have been introduced by the flip-chip mounting of discrete diode chips. Simulation results show that the output power of the tripler was more than 3.6 mW in the frequency range of 324~352 GHz and reached the peak efficiency of 10.7% at 340 GHz under the condition that input power was 100 mW and bias voltage for each die was  $-1.95$  V.



**Figure 5.** Photograph of the assembled tripler block connected with the SMA-connector for DC bias (left). Picture of the fabricated THz GaAs monolithic integrated tripler circuit installed in a split block with the enlarged view of the diode chip (right).

#### 2.4. 0.34 THz SHM Development

Based on the anti-parallel Schottky diode chip for mixers, whose parameters are listed in Table 2, a 0.34 THz SHM using GaAs monolithic technology was proposed. A further look at the 3D diode chip model and diode port configuration in HFSS is given in Figure 6. The integration line had to be assigned in the port definition to specify the current polarity of the diode to ensure that the subsequent construction of the co-simulation diagram was correct. The proposed circuit configuration of the monolithic integrated SHM is shown in Figure 7. As noted in the figure, it mainly consisted of three parts, among which the diode chip had already been designed and determined. The remaining task was to complete the design of RF matching and LO/IF (local oscillator or intermediate frequency) matching circuits distributed on the left and right ends of the diode chip, thereby improving conversion efficiency. After each part was optimized, such as LO/IF CMRC filters and E-plane transition probes, all the sub-circuits were combined with the diode chip for 3D electromagnetic simulation. The S-parameter file with five ports of the whole circuit, as shown in Figure 7, was then exported from HFSS to ADS and schematically reconstructed. Harmonic balance simulation was then carried out for the mixer circuit to predict performance. After several iterations of co-simulation, the SHM circuit was finalized.

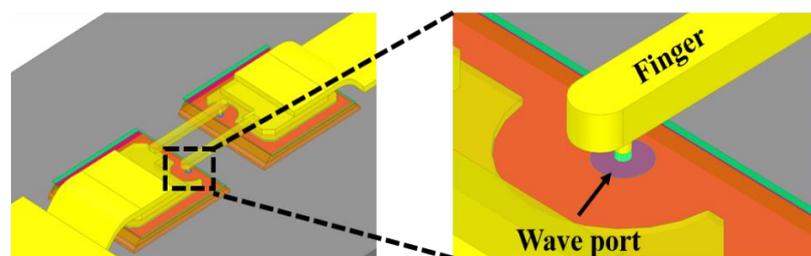


Figure 6. 3D diode chip model and diode port configuration in HFSS.

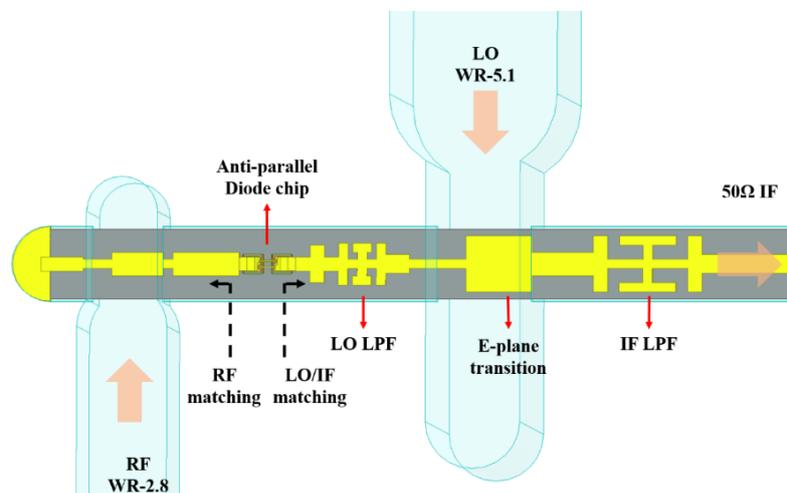
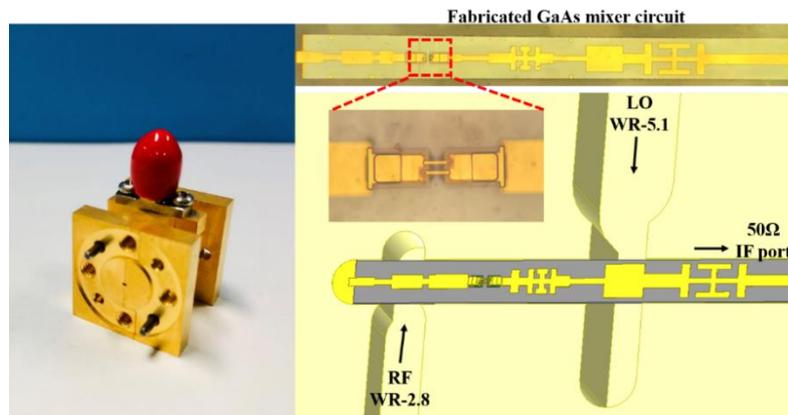


Figure 7. Circuit configuration of the proposed monolithic integrated subharmonic mixer in HFSS.

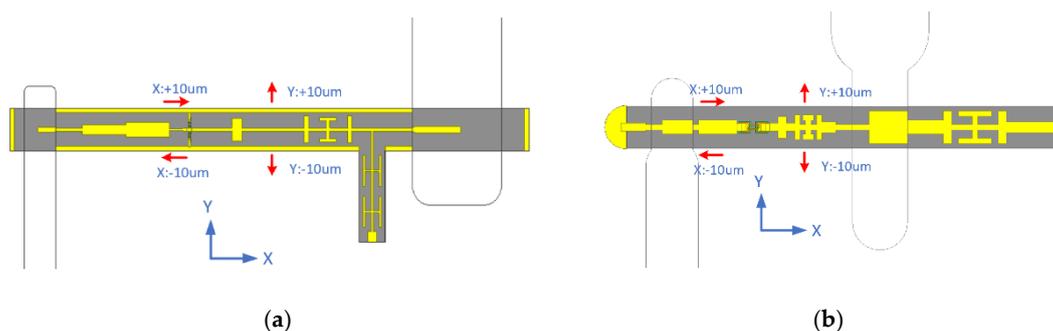
A photograph of the fabricated THz GaAs monolithic integrated SHM circuit and assembly diagram in the split block is shown in Figure 8. When the mixer was assembled, the entire GaAs mixer circuit was aligned, along with a suspended microstrip slot milled by a high-precision computerized numerical control (CNC) process and fixed in the metal block through adhesive silver glue. The IF output port was finally connected to a K connector through a  $50 \Omega$  transmission line realized on Rogers RT/duroid 5880 substrates. The simulation results showed that the double sideband (DSB) noise temperature and DSB conversion loss of SHM were lower than 1500 K and 8 dB, in the range of 321~354 GHz, respectively, and reached the lowest values of 697 K and 6.1 dB at 339 GHz.



**Figure 8.** Photograph of the assembled SHM block with the K-connector for the IF output (**left**). Picture of the fabricated THz GaAs monolithic integrated SHM circuit and assembly diagram in the split block with the enlarged view of diode chip (**right**).

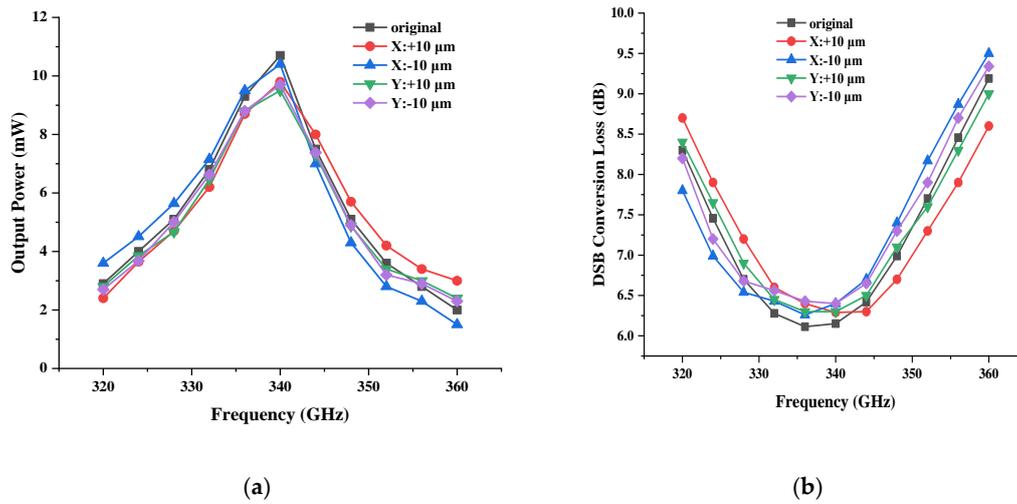
### 2.5. Tolerance Analysis

We conducted tolerance analysis through simulation to estimate the impact of possible errors on device performance. In the actual fabrication process of triplers and mixers, potential errors may occur from substrate processing, cavity machining, and circuit assembly. Among them, the semiconductor technology ensured that the substrate processing error was guaranteed within  $0.5 \mu\text{m}$ , which had a negligible impact on the circuit, working at  $0.34 \text{ THz}$ . However, the tolerance of cavity machining and circuit assembly were generally about  $\pm 5 \mu\text{m}$ , which could not be ignored and would affect the performance of devices. Since the two types of error were relative, cavity machining error could be accumulated to the circuit assembly error, that is  $\pm 10 \mu\text{m}$ . Therefore, it can be simplified to only perform tolerance analysis on the positioning deviation during substrate assembly. Taking the Cartesian coordinate system as a reference, the GaAs integrated circuit moved  $\pm 10 \mu\text{m}$  in the  $x$  and  $y$  directions, as shown in Figure 9. The tolerance analysis simulation results and comparison with original simulation data are presented in Figure 10.



**Figure 9.** Tolerance analysis of (a)  $0.34 \text{ THz}$  tripler and (b)  $0.34 \text{ THz}$  SHM caused by a substrate assembly error. The substrate assembly position deviates from the original position  $\pm 10 \mu\text{m}$  along the  $x$  and  $y$  directions, respectively.

The shape and trend of the simulation curves agreed with the original result after the substrate was shifted, though there were still certain impacts on the center frequency, bandwidth, output power, or conversion loss, mainly caused by impedance variations at RF/LO transition probes, which affected the matching condition at the diode. Additionally, the effect depended more on the  $R_f$  transition structure because the absolute size was smaller. However, the deterioration of the circuit performance due to the substrate assembly error was acceptable, indicating that the circuits had a good tolerance to errors caused by substrate assembly.



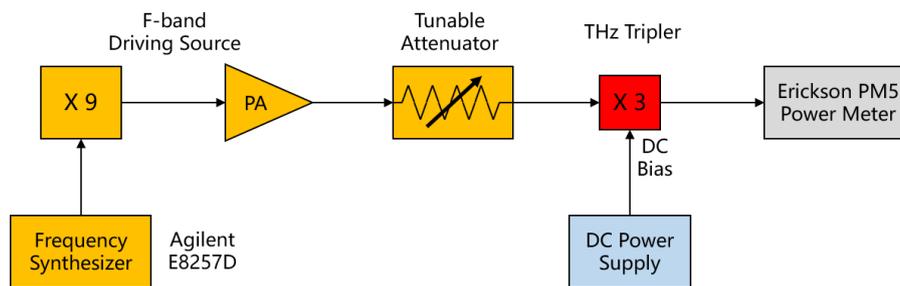
**Figure 10.** Tolerance analysis simulation results and comparison with original simulation data of (a) 0.34 THz tripler and (b) 0.34 THz SHM.

### 3. Results and Discussions

Based on the self-designed Schottky diodes and GaAs monolithic integrated technology, 0.34 THz triplers and sub-harmonic mixers were fabricated. To verify the effectiveness of the diode design method and simulation optimization method proposed in this article, three triplers and three mixers were assembled and measured for the research on performance consistency.

#### 3.1. 0.34 THz Triplers’ Performances

The tripler’s test diagram is shown in Figure 11, in which the frequency synthesizer Agilent E8257D provided frequency reference to the F-band driving source, which mainly featured the  $\times 9$  frequency multiplication and power amplification. A tunable attenuator was inserted between the tripler and the F-band source to easily adjust the wanted input power up to 100 mW. The Erickson PM5 waveguide power meter was used to measure the output power around 0.34 THz and calibrate the input power. When tested, the DC bias voltage was tuned to obtain the best performance within a certain frequency range.



**Figure 11.** Schematic diagram of the 0.34 THz tripler’s output power test setup.

The performance of the tripler with different input power levels is depicted in Figure 12. With known input power and output power, efficiency can be calculated. As can be seen from the measurement results, a peak efficiency of 6.8% and maximum output power of 6.8 mW were obtained at 338 GHz with an input power of 100 mW and a DC bias voltage of  $-2.56$  V. It was found that  $-1.28$  V was the optimum bias voltage for every single Schottky die. In addition, the tripler showed greater than 1 mW output power in the range of 324 GHz–352 GHz when driven by 100 mW. From the perspective of the increasing tendency of output power with increasing input power from 50 mW to 100 mW, there was still room for further improvement in output power. It is indicated that the tripler still did

not reach saturation when driven by 100 mW, which is currently already the highest available power, from 108 GHz to 117.33 GHz, in the lab. Moreover, a comparison between simulated and measured performance with 100 mW input power is given in Figure 13. Note that the measured curves had a similar trend to the simulated curves, though the measured conversion efficiency was a little lower. The frequency corresponding to the measured peak efficiency was close to the simulated frequency, implying the effectiveness of the diode design method and accuracy of performance prediction based on simulations in this work. Moreover, the measured results of the three triplers at room temperature are shown in Figure 13b. Note also that the three different triplers had very similar performance in terms of efficiency and bandwidth. This implies that the monolithic integration process proposed in this article is reliable and can ensure consistency between different products.

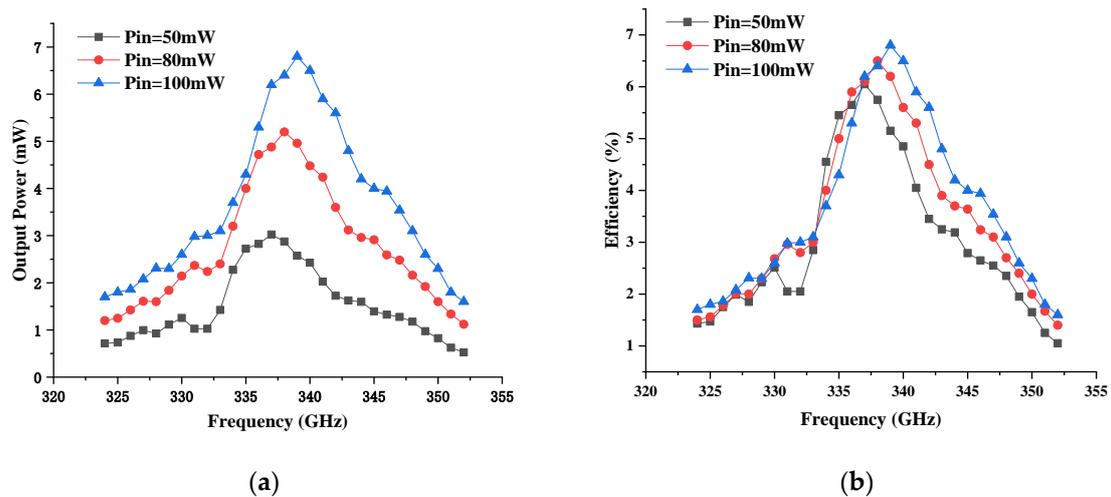


Figure 12. Measured (a) output power and (b) frequency conversion efficiency of the 0.34 THz tripler with different input power levels from 324 GHz to 352 GHz.

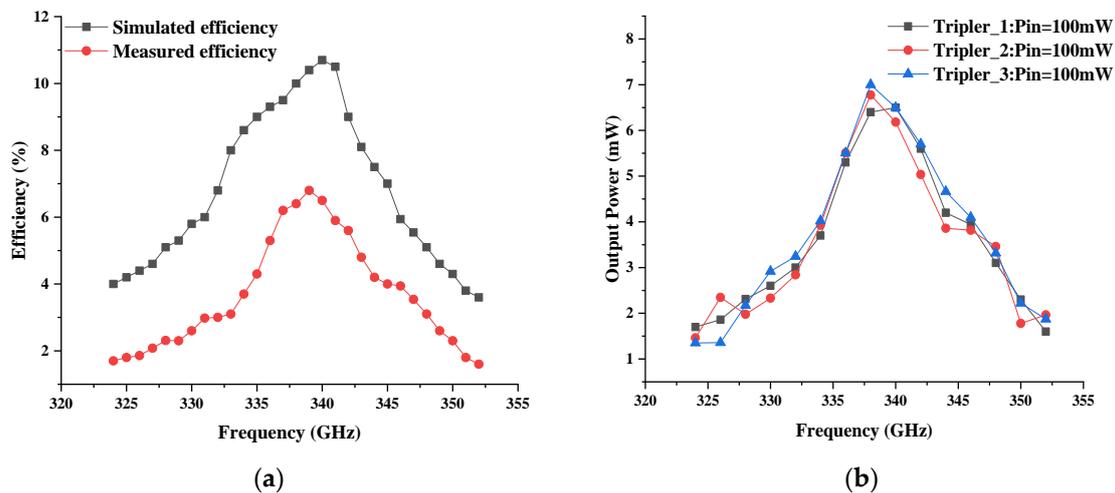
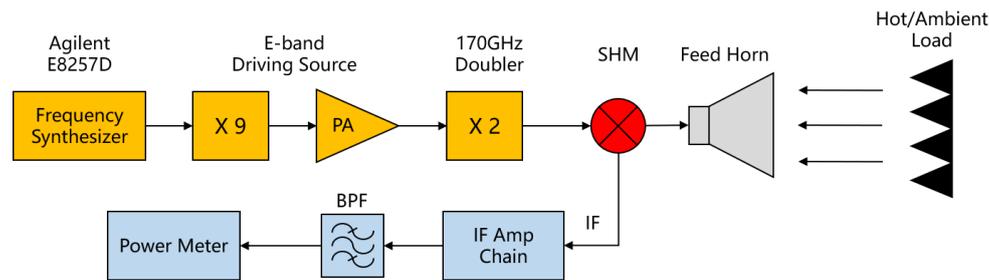


Figure 13. Performance comparison of (a) simulated and measured efficiency with 100 mW input power and (b) measured output power of three different tripler modules with 100 mW input power.

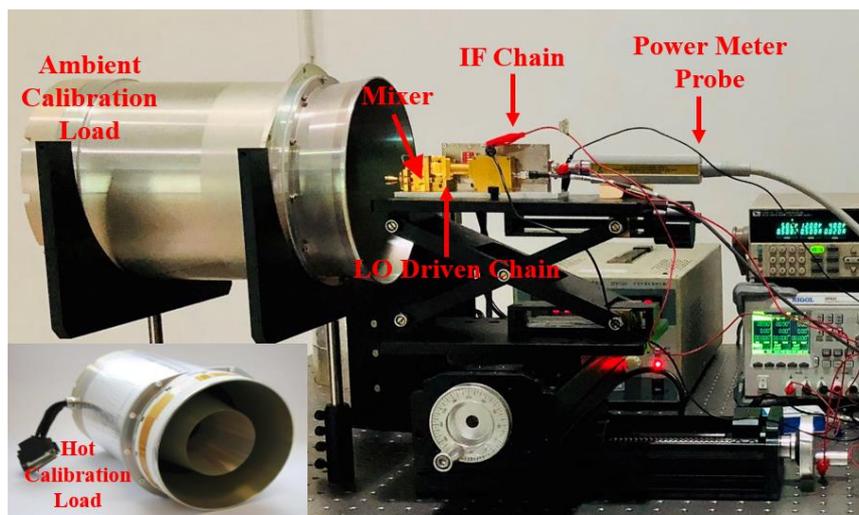
### 3.2. 0.34 THz Mixers' Performances

The SHM performances were characterized by the Y-factor method at room temperature. There have been many excellent reports about noise temperature measurement of THz receivers or mixers, such as [25,35], where the large temperature difference between LN<sub>2</sub> and ambient loads (295/77 K) ensures test accuracy. In this paper, the ambient calibration load (288 K) and the hot calibration

load (361 K) (from TK Inc.) were presented alternately at the input of the receiver through the feed horn antenna. The setup, illustrated in Figures 14 and 15, was mounted on an optical table, and the experimental platform was relatively simpler. Furthermore, in order to reduce the test error, we removed unreliable data, such as too large or too small data when measuring, and the noise temperature at each frequency point was obtained by averaging multiple sets of valid data. The mixer's LO was provided by a 170 GHz doubler driven by an E-band  $\times 9$  multiplication chain, with a maximum LO power up to 6 mW. As the power level radiated from the hot/ambient load was very low, a 60 dB high gain IF amplifier was cascaded at the IF output port of the mixer. The final amplified power was monitored by Agilent P-Series Power Meter N1911A with a wideband power sensor.



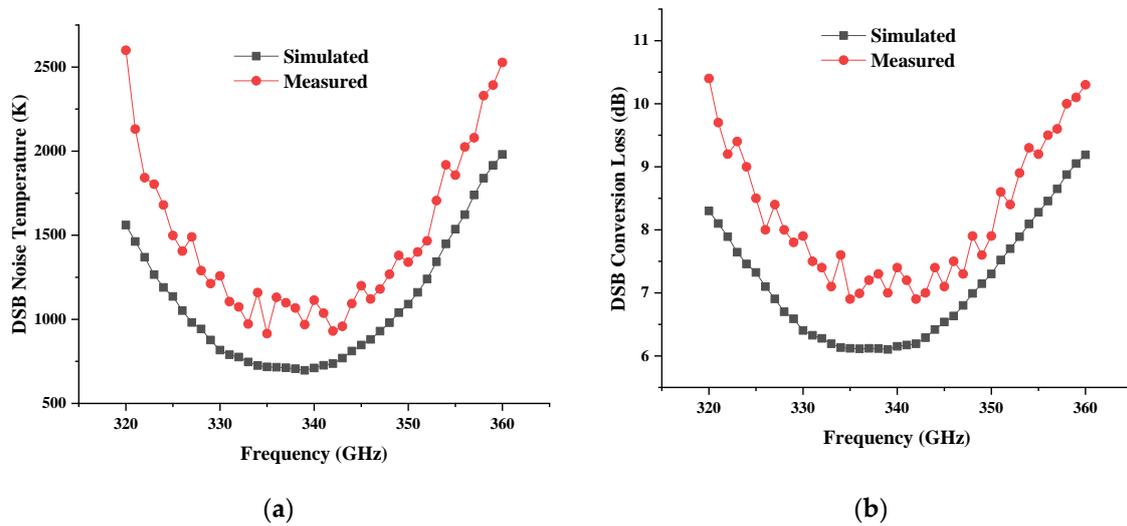
**Figure 14.** Schematic diagram of 0.34 THz SHM's noise temperature test setup.



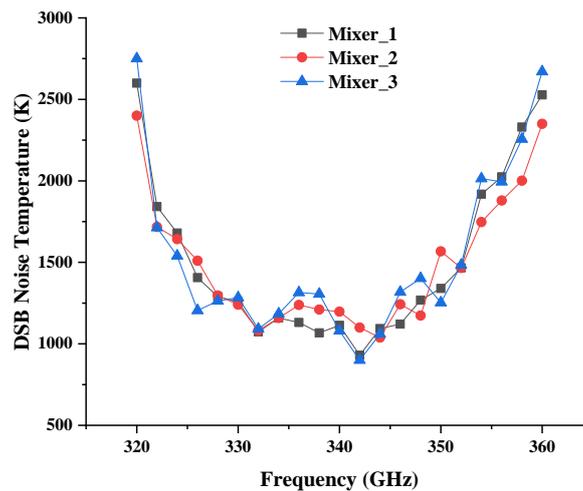
**Figure 15.** Photograph of the 0.34 THz SHM's noise temperature test platform using Y-factor method measurement. The ambient/hot calibration load, respectively, radiates broadband noise energy related to real-time temperature into the receiver through feed horn antenna. Every time the calibration load is exchanged the under-test receiver is position fixed.

The DSB noise temperature and conversion gain of the receiver (including the SHM and IF chain) can be calculated through Y-factor measurement. Since the noise figure and gain of the IF chain were already known, the DSB noise temperature and conversion loss could be extracted according to methods detailed in [36]. Eventually, the measured performances of the SHM, in comparison with simulation results, were curved, as shown in Figure 16. The DSB noise temperature and DSB conversion loss of SHM were lower than 1500 K and 9 dB in the range of 325~352 GHz, respectively, and reached the lowest values of 915 K and 6.9 dB at 335 GHz. In fact, the deviation of the measured noise temperature from the simulation was within expectations. All the measured results included internal waveguide transmission loss, flange connection loss, and feed horn antenna loss. Furthermore, the hot temperature was difficult to ensure precisely and there was an error in the coupling from the horn to calibration loads. Moreover, the measured results of the three mixers at room temperature are

shown in Figure 17. In terms of noise temperature or operating frequency, the performance of different mixer modules was only slightly different.



**Figure 16.** Simulated and measured performances of 0.34 THz SHM from 320 GHz to 360 GHz (a) double sideband (DSB) noise temperature and (b) DSB conversion loss.



**Figure 17.** Comparison of the measured DSB noise temperature of three different mixer modules.

We also investigated published Schottky SHM performances in a similar frequency range, which are listed in Table 3. The DSB noise temperature and conversion loss of this work were close to or better than those reported in the other literature. Additionally, a hybrid integrated circuit with a flip-chip soldered diode chip was adopted in [37–39], which resulted in the inability to guarantee the consistency of multiple channels in a large array.

**Table 3.** Comparison of published Schottky SHM performance in a similar frequency range.

Reference	Frequency Range (GHz)	Noise Temperature (K)	Conversion Loss (dB)
[37]	290–310	2000–2600 (SSB)	9–10 (SSB)
[38]	295–345	900 (DSB) (minimum)	9–13 (SSB)
[39]	320–360	900 (DSB)	9 (SSB)
This work	325–352	900–1500 (DSB)	6–9 (DSB)

#### 4. Conclusions

Taking THz active imaging array as the application background, 0.34 THz triplers, and mixers based on 12- $\mu\text{m}$ -thick GaAs monolithic integrated process and Schottky diode chips, are proposed in this article. The diodes' geometry was optimized first to achieve the best performance by quantitatively analyzing the physical dimensions of diodes. Based on the use of precise simulation tools, such as Ansoft HFSS and Agilent ADS, accurate electromagnetic modeling of the diode was carried out and the performance of triplers or mixers was predicted through co-simulation. Experimental results show that, at room temperature, by injecting 100 mW, the THz tripler could achieve a peak efficiency of 6.8% at 338 GHz. The output power of greater than 1 mW was achieved in the range of 324 GHz to 352 GHz. The THz SHM showed good performance, in that the DSB noise temperature was lower than 1500 K and the DSB conversion loss was lower than 9 dB in the frequency range of 325–352 GHz. Three frequency triplers and three mixers were processed and assembled and their performance was tested and compared. It is shown that they all show a high consistency in performance. The results of both the THz tripler and SHM agreed well with the simulations, thus verifying the validity of the design method proposed in this paper. To sum up, the GaAs monolithic integrated THz tripler and SHM proposed in this paper show good performance and provide support for future applications to THz active imaging arrays. However, in actual THz imaging applications, we are still facing challenges, such as limited operating range caused by large atmospheric attenuation, which can be tackled by power combining technology and III/V compound-based power amplifications to further increase transmit power.

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