

## Article

# A Voltage Multiplier Circuit Based Quadratic Boost Converter for Energy Storage Application

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**Abstract:** In this paper, a new transformerless high voltage gain dc-dc converter is proposed for low and medium power application. The proposed converter has high quadratic gain and utilizes only two inductors to achieve this gain. It has two switches that are operated simultaneously, making control of the converter easy. The proposed converter's output voltage gain is higher than the conventional quadratic boost converter and other recently proposed high gain quadratic converters. A voltage multiplier circuit (VMC) is integrated with the proposed converter, which significantly increases the converter's output voltage. Apart from a high output voltage, the proposed converter has low voltage stress across switches and capacitors, which is a major advantage of the proposed topology. A hardware prototype of 200 W of the proposed converter is developed in the laboratory to validate the converter's performance. The efficiency of the converter is obtained through PLECS software by incorporating the switching and conduction losses.

**Keywords:** energy storage system; high gain; voltage multiplier circuit (VMC); continuous current mode (CCM); efficiency

## 1. Introduction

High gain dc to dc converters have increasingly become popular due to their suitability in solar Photovoltaic (PV) systems, electric vehicles, and HVDC transmission systems. The output voltage from solar PV modules, fuel cells, and batteries is generally low and needs to be boosted up to maintain the dc-link voltage at the inverter's input. Conventional boost converters suffer from high voltage stress across the switch, low gain, and poor efficiency at higher duty ratios [1]. The high gain dc-dc boost converter uses a combination of inductors, capacitors, diodes, and switches to transfer the power between capacitors and inductors to increase the output voltage. These converters use various combinations, such as voltage multiplier cells (VMCs), coupled inductors, switched capacitors, and switched inductors to increase the output voltage. Each of these techniques has its own merits and demerits [1]. Many topologies utilizing different strategies to increase the output voltage are reported in the literature.

Moreover, the challenge is to keep the number of components in the converter low to decrease the cost and increase the converter's efficiency. The dc-dc converter's isolated topologies are used in low

and medium power applications where isolation is not necessary and very high efficiency [2] is not required. VMC is also a very popular way to increase the voltage of the circuit substantially. To get very high output voltage isolated topologies with transformer and coupled inductor are used to increase the converter's voltage gain. These problems are addressed in the new high gain boost topologies. A dc-dc switched-capacitor based VMC is employed in [3] to increase the gain of the boost converter. Although it utilizes many capacitors and diodes, the technique is very simple and effective in increasing the converter's output voltage gain. A new buck-boost converter derived from conventional boost and buck-boost converter is proposed in [4], but the stress across one switch is high, and the voltage gain in boost range is limited. In [5], a modified boost converter is proposed for electric vehicle applications, but the converter utilizes three inductors; its gain is still less than the converter proposed in this paper. A boost converter with continuous input current and low voltage stress across switching devices is presented in [6]. The converter is suitable for solar PV applications. Switched inductors and switched capacitors-based topologies are proposed in [7,8]. The switched capacitor-based topologies have higher gain than the switched inductor-based topologies. A hybrid converter using switched inductors and capacitors is proposed in [9]. The combination has substantially increased the gain of the converter of the proposed hybrid converter. Other structures of the dc-dc converter with switched-capacitor are presented in [10,11].

However, high inrush current through capacitors while charging is the main disadvantage of the switched capacitor topologies. Different dc-dc converters can be connected in differential connection [12] mode to obtain very high gain with reduced voltage stress. To get high voltage gain at low duty ratios, a coupled inductor is used in dc-dc converters. By changing the turn ratio " $n$ " of the coupled inductor, the converter's gain can be increased to very high values. These circuits have high efficiency and low values of stress across switching elements, but the energy stored in leakage inductance may cause severe voltage spikes across the switch, for which a proper resonant or clamp circuit needs to be designed. The coupled inductor can also be incorporated with VMC to increase the converter's gain further, but in this case, the number of components may increase, making the circuit bulky and costly [13–15]. Another high gain converter suitable for electric vehicle applications is proposed in [16]. High gain and low stress across capacitors and continuous input current are desirable features required in the dc-dc converter [17,18] used in fuel cell and electric vehicle applications.

Interleaved boost converters [19–21] are derived from H-bridge structures and have very low voltages stress across devices. The input current drawn from the source is also very small; however, these structures need multiple VMCs to increase the voltage to desirable limits. In some interleaved structures, the number of components may increase to obtain high voltage at the output. Z-source dc-dc converters can be employed to get continuous input current with reduced voltage stress [22,23] with moderate voltage gain. The parasitic resistance of the inductor influences the voltage gain and efficiency of the converter. The higher the value of parasitic resistance, the lower the voltage gain and losses will increase, resulting in a drop of efficiency at higher [24] duty ratios. Some other new dc-dc converter structures with high voltage gain are proposed in [25,26]. Quadratic boost converters provide high voltage gain, especially at low duty ratios. The non-isolated configurations of these structures do not use any transformer and are suitable in solar PV applications for medium power applications. The voltage stress across switch, diodes, and capacitors is generally low in these structures, which is another advantage apart from high-gain; however, the number of components may increase [27–30] if a very high quadratic gain is required.

The paper's main contribution is the proposed new dc-dc converter with desirable characteristics like high voltage gain with a reduced number of components, low voltage stress on switching devices, and continuous input current. Further, the proposed converter has a quadratic gain, which is achieved by using only two inductors. It is to be noted that a smaller number of inductors in the circuit makes the circuit less bulky. The other key feature of the proposed converter is that the duty ratio can be changed widely to obtain the desired output voltage which is not possible in Z-source type of converters [22,23].

The main advantages of the proposed topology are as follows:

- (1) The voltage gain is higher than the conventional quadratic boost converter (CQBC) [18], and twice the quadratic boost converter (TCQBC) proposed in [30]. The voltage gain of more than 10 times can be achieved for the duty of less than 0.5.
- (2) The voltage stress across switches of the proposed converter is much less than the output voltage  $V_o$ , which is an improvement over the quadratic converters proposed in [18,30] in which the voltage stress is equal to  $V_o$ . Moreover, the diodes and capacitors also have low voltage stress, leading to the selection of low voltage rating devices and subsequently improving the converter's efficiency.
- (3) To achieve this high voltage gain, the coupled inductor is not used, and hence the problem of leakage inductance and the need for a snubber circuit is avoided.
- (4) The input current is continuous, which is another significant advantage of the proposed topology.
- (5) The control of the proposed converter is easy, as two switches are turned ON and OFF simultaneously.

In Section 2 the structure and working of the proposed converter is discussed. In Section 3 losses in the converter and non-ideal gain of the converter are shown. In Section 4 comparison of the proposed converter with other converters are shown. In Sections 5 and 6, hardware results and conclusions are discussed.

## 2. Proposed Topology

### 2.1. Structure

The circuit of CQBC and TCQBC are shown in Figure 1a,b. It can be seen that both these converters use two inductors, but their gain is less than the proposed topology. The switch is also directly connected across the load, which makes the voltage stress across the switch equal to output voltage  $V_o$ . The proposed converter structure is presented in Figure 1c with a voltage multiplier cell, which increases the output voltage gain. Two Inductors ( $L_1$  and  $L_2$ ), four diodes ( $D_1, D_2, D_3, D_4$ ), four capacitors ( $C_1, C_2, C_3$ , and  $C_4$ ), and two switches ( $S_1$  and  $S_2$ ) are used to realize the proposed converter. This VMC can also be placed before diode  $D_1$ , but the voltage gain would not be that high, as in the converter case presented in Figure 1c. One more configuration is also possible in which the VMC is placed at two points before diode  $D_1$  and before diode  $D_4$ . This increases the voltage gain further but makes the circuit more complex and less efficient.

The VMC integration increases the output voltage and reduces the voltage stress on the diodes and switches with respect to the output voltage. This VMC can also be placed before diode  $D_1$ , but the voltage gain would not be that high, as in the converter case presented in Figure 1c. One more configuration is also possible in which the VMC is placed at two points before diode  $D_1$  and before diode  $D_4$ . This increases the voltage gain further but makes the circuit more complex and less efficient.

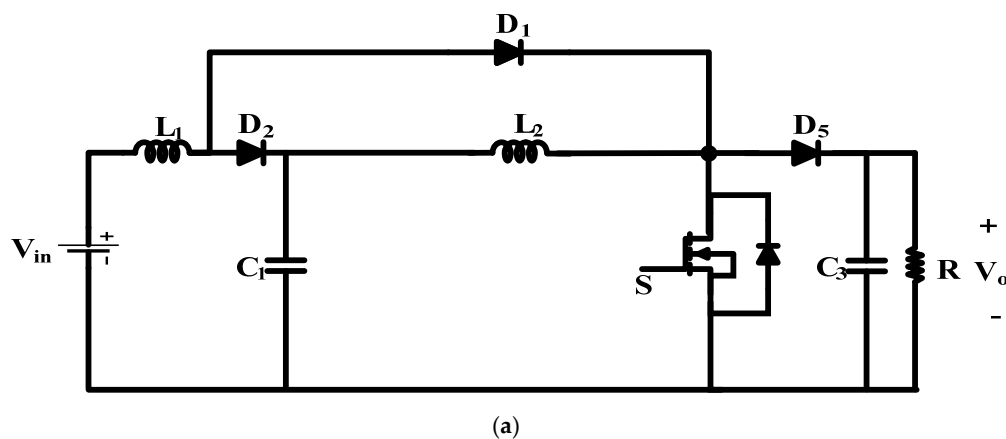
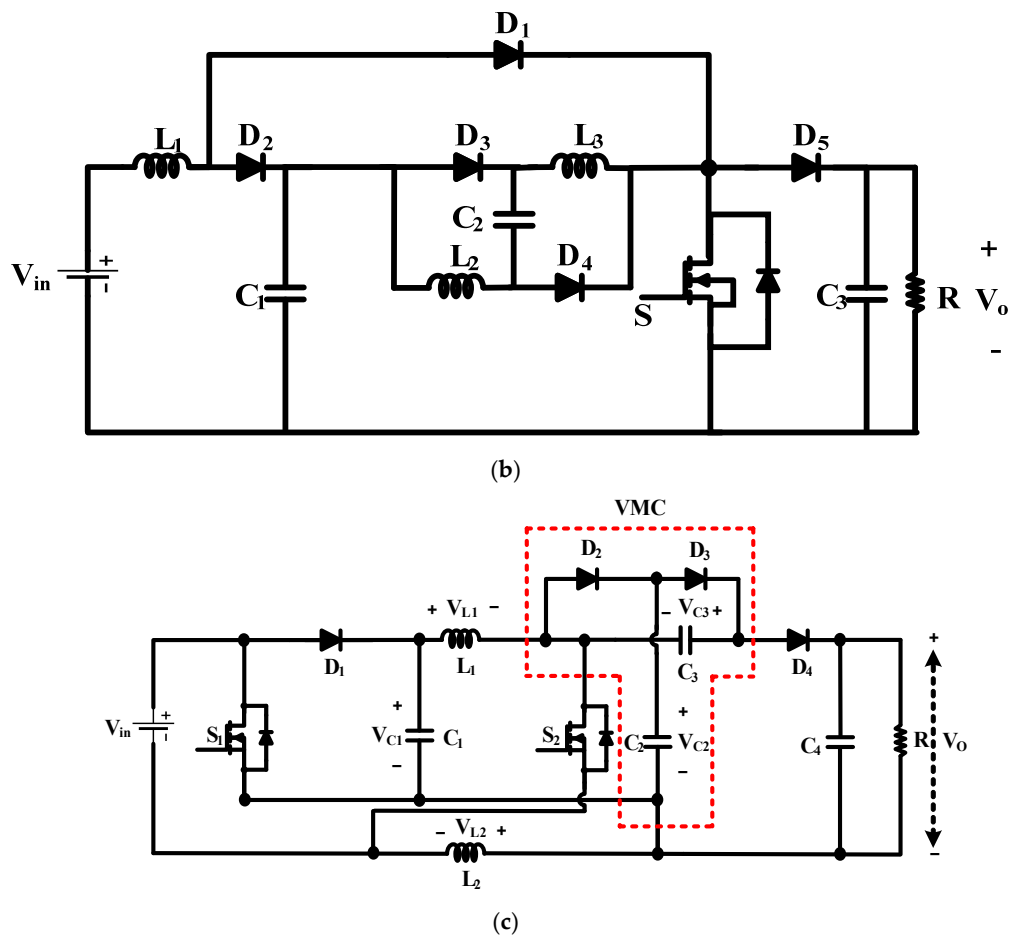


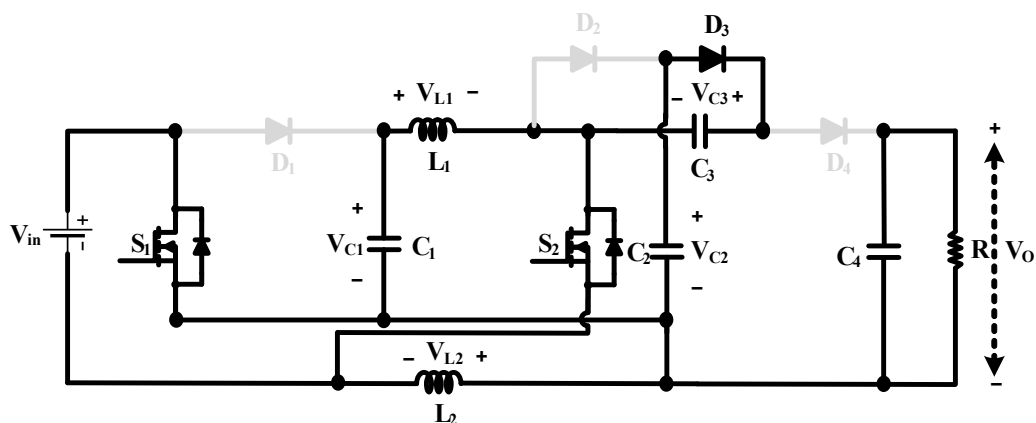
Figure 1. Cont.



**Figure 1.** (a) Conventional quadratic boost converter [18]. (b) Twice the Quadratic boost converter proposed in [30] (c). Proposed converter.

## 2.2. Working

**Mode 1:** In this mode, both the switches are ON, and diode  $D_3$  conducts. This interval exists for a time interval of  $DT$  where  $D$  is the duty ratio, and  $T$  is the time period. The equivalent circuit for the first mode of operation is shown in Figure 2. During the first mode of operation, the inductor  $L_1$  is energized by the capacitor  $C_1$ , and the charge of the capacitor  $C_1$  decreases during the first mode of operation, as shown in Figure 3. While the DC supply energizes inductor  $L_2$ , capacitor  $C_2$  discharges into  $C_3$ , and the energy of capacitor  $C_4$  is transferred to the load.



**Figure 2.** The first mode of operation.



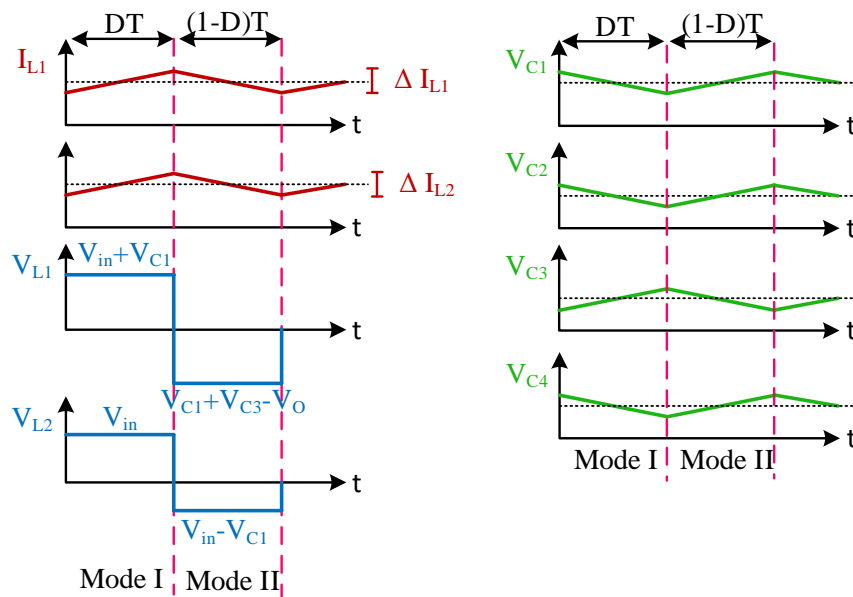


Figure 3. Related waveforms of the proposed converter.

The related equations during the first mode of operation are as follows:

$$V_{L1} = V_{in} + V_{C1} \quad (1)$$

$$V_{L2} = V_{in} \quad (2)$$

$$V_{C3} = V_{in} + V_{C2} \quad (3)$$

**Mode 2:** When both the switches are turned off during the second mode of operation, the diode  $D_1$ ,  $D_2$ , and  $D_4$  are conducting while diode  $D_3$  is reversed biased. During the second mode of operation, the capacitor  $C_1$  is charged by the DC power supply, the energy of the inductors is transferred to the capacitor  $C_2$  while the capacitor  $C_3$  charges  $C_4$ . The equivalent circuit for the second mode of operation is shown in Figure 4. The related equations are as follows:

$$V_{L1} = V_{C1} + V_{C3} - V_O \quad (4)$$

$$V_{L2} = V_{in} - V_{C1} \quad (5)$$

$$V_{C3} = V_O - V_{C2} \quad (6)$$

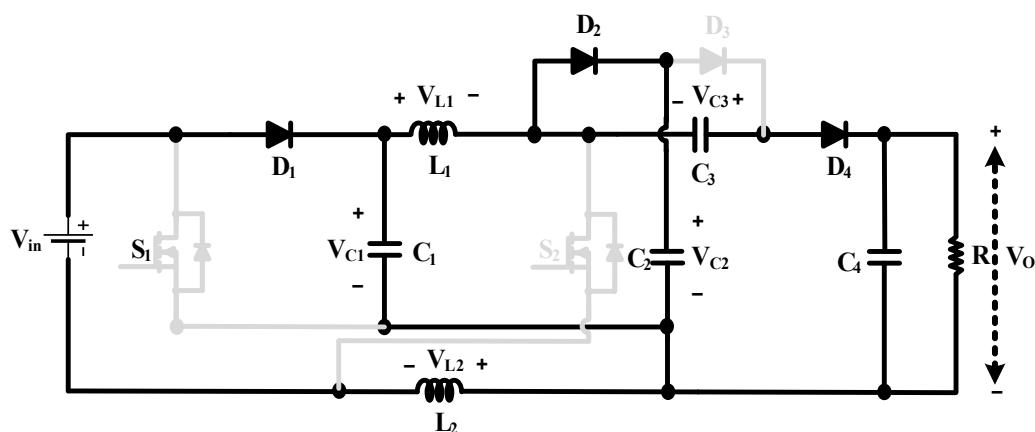


Figure 4. The second mode of operation.

Now applying volt-sec balance in inductor  $L_2$

$$\int_0^T V_{L2}(t) \cdot dt = 0 \quad (7)$$

$$V_{in} \times DT + (V_{in} - V_{C1}) \times (1 - D)T = 0 \quad (8)$$

$$V_{C1} = \frac{V_{in}}{1 - D} \quad (9)$$

Now applying volt-sec balance in inductor  $L_1$

$$\int_0^T V_{L1}(t) \cdot dt = 0 \quad (10)$$

$$(V_{in} + V_{C1}) \times DT + (V_{C1} + V_{C3} - V_O) \times (1 - D)T = 0 \quad (11)$$

After combining the above equations, the voltage gain ( $M$ ) of the converter can be written as:

$$M = \frac{V_O}{V_{in}} = \frac{(3 - D^2)}{(1 - D)^2} \quad (12)$$

The voltage across the capacitors are as follows:

$$V_{C1} = \frac{V_{in}}{1 - D} = \frac{V_O(1 - D)}{(3 - D^2)} \quad (13)$$

$$V_{C2} = \frac{V_{in}(1 + D - 2D^2)}{(1 - D)^2} = \frac{V_O(1 + D - 2D^2)}{(3 - D^2)} \quad (14)$$

$$V_{C3} = \frac{V_{in}(2 - D)}{(1 - D)^2} = \frac{V_O(2 - D)}{(3 - D^2)} \quad (15)$$

For the continuous mode of operation, the value of the inductors and capacitors should be selected as follows

$$L_1 \geq \frac{R(1 - D)^2(2 - D)D}{4f_s(3 - D^2)} \quad (16)$$

$$L_2 \geq \frac{R(1 - D)^4D}{4f_s(3 - D^2)} \quad (17)$$

$$\begin{aligned} C_1 &= \frac{2V_OD}{R(1 - D)f_s\Delta V_{C1}} = \frac{2V_{in}(3 - D^2)D}{R(1 - D)^3f_s\Delta V_{C1}} \\ C_2 &= \frac{V_O}{Rf_s\Delta V_{C2}} = \frac{V_{in}(3 - D^2)}{R(1 - D)^2f_s\Delta V_{C2}} \\ C_3 &= \frac{V_O}{Rf_s\Delta V_{C3}} = \frac{V_{in}(3 - D^2)}{R(1 - D)^2f_s\Delta V_{C3}} \\ C_4 &= \frac{V_OD}{Rf_s\Delta V_{C4}} = \frac{V_{in}(3 - D^2)D}{R(1 - D)^2f_s\Delta V_{C4}} \end{aligned} \quad (18)$$

### 2.3. Voltage and Current Stress across Components

The voltage and current stress across the switches and diodes are presented in Table 1. The voltage across the diode and switches is lower than the output voltage, which is not valid in the conventional quadratic boost converter. The selection of the lower rating components means a reduction in the manufacturing cost.

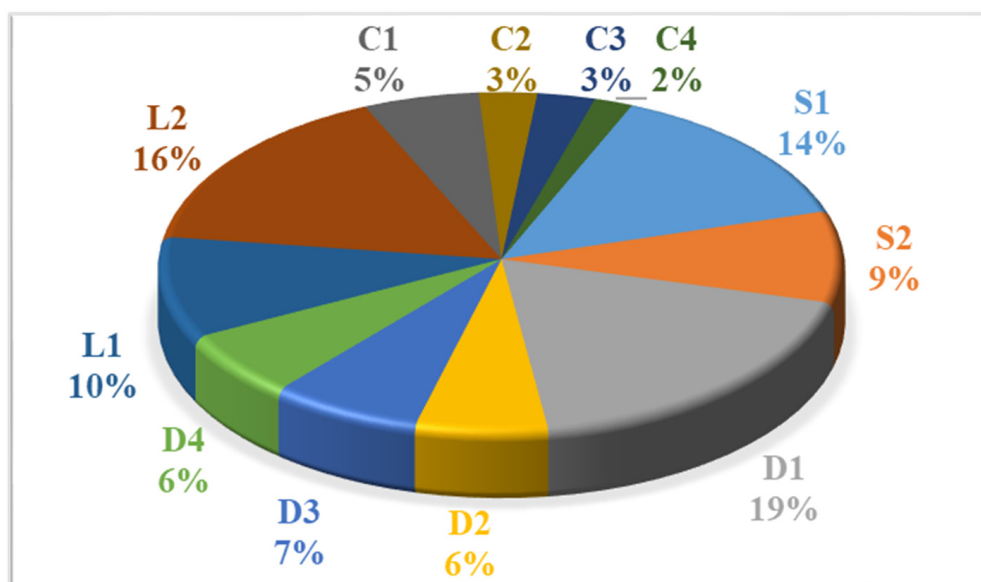
**Table 1.** Voltage stress and current across the switches and diodes.

Component	Voltage Stress (Volt)	Average Current During Their Conduction (Amp)	Average Current for the Complete Cycle (Amp)	RMS Current (Amp)
$S_1$	$\frac{V_{in}}{(1-D)} = \frac{V_o(1-D)}{(3-D^2)}$	$\frac{V_o(1+D-D^2)}{R(1-D)^2D}$	$\frac{V_o(1+D-D^2)}{R(1-D)^2}$	$\frac{V_o(1+D-D^2)}{R(1-D)^2\sqrt{D}}$
$S_2$	$\frac{V_{in}}{(1-D)^2} = \frac{V_o}{(3-D^2)}$	$\frac{V_o(1+D)}{RD(1-D)}$	$\frac{V_oD(1+D)}{RD(1-D)}$	$\frac{V_o(1+D)}{R(1-D)\sqrt{D}}$
$D_1$	$\frac{V_{in}}{(1-D)} = \frac{V_o(1-D)}{(3-D^2)}$	$\frac{2V_o}{R(1-D)^2}$	$\frac{2V_o}{R(1-D)}$	$\frac{2V_o}{R(1-D)^{3/2}}$
$D_2$	$\frac{V_{in}(2-D-D^2)}{(1-D)^2} = \frac{V_o(2-D-D^2)}{(3-D^2)}$	$\frac{V_o}{R(1-D)}$	$\frac{V_o}{R}$	$\frac{V_o}{R\sqrt{1-D}}$
$D_3$	$\frac{V_{in}(2-D-D^2)}{(1-D)^2} = \frac{V_o(2-D-D^2)}{(3-D^2)}$	$\frac{V_o}{RD}$	$\frac{V_o}{R}$	$\frac{V_o}{R\sqrt{D}}$
$D_4$	$\frac{V_{in}(2-D-D^2)}{(1-D)^2} = \frac{V_o(2-D-D^2)}{(3-D^2)}$	$\frac{V_o}{R(1-D)}$	$\frac{V_o}{R}$	$\frac{V_o}{R\sqrt{1-D}}$

### 3. Loss and Non-Ideal Gain Analysis

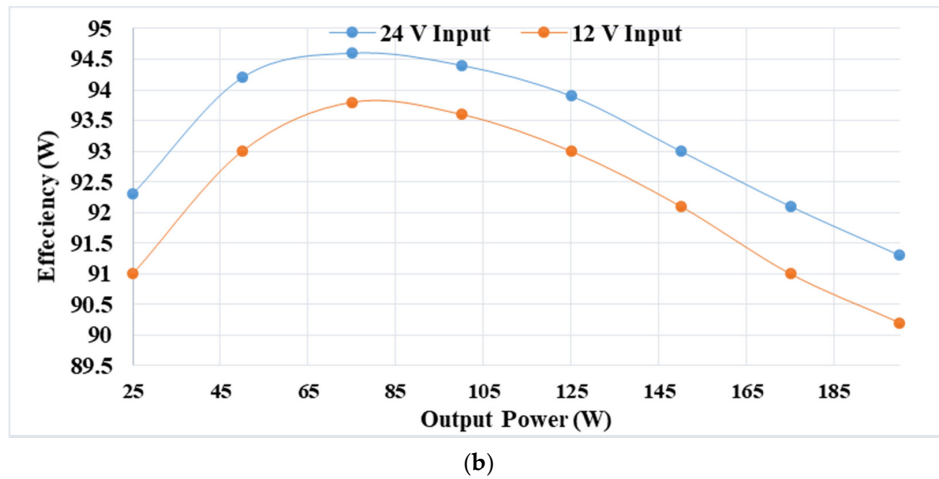
#### 3.1. Bifurcation of Losses

The bifurcation of losses at 45 W is shown in Figure 5a. Switches and diodes constitute more than 60% of the total losses. Loss analysis is done in PLECS software by developing a converter's thermal model and putting the switching and conduction loss data in the look-up table from the datasheet. The converter's efficiency is 92.6% at 45 W and 12 V. From Figure 5b, as  $V_{in}$  increases, the converter's maximum efficiency improves substantially. This is because at higher input voltages, a small duty ratio is required to get the same amount of voltage gain, and hence conduction losses are significantly reduced. Higher input voltage leads to lower current in the circuit for the same output voltage, improving efficiency by reducing the conduction losses.



(a)

**Figure 5.** Cont.



**Figure 5.** (a) Bifurcation of losses in the proposed converter at 45 W, (b) efficiency of the proposed converter.

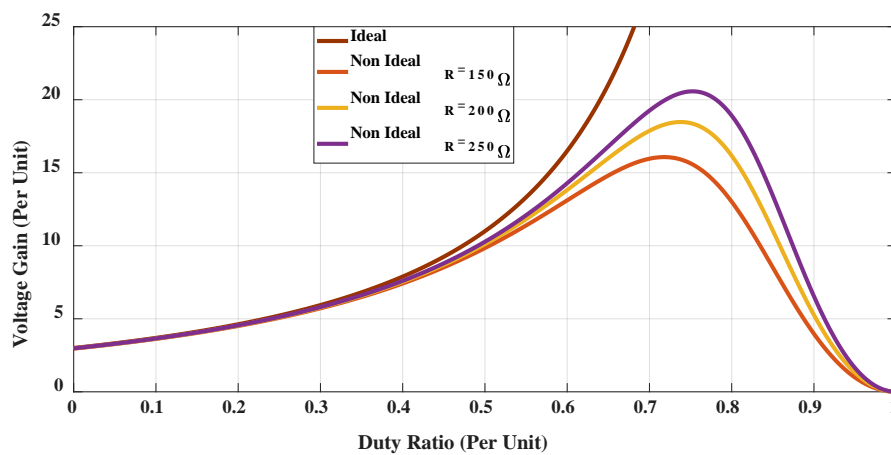
### 3.2. Non-Ideal Gain

Using the principle of energy conservation, the proposed converter's non-ideal gain with parasitic inductor resistance can be derived as follows.

$$\begin{aligned}
 P_{in} &= P_o + P_{L_{total}} \\
 P_{in} &= \frac{V_{in} V_o (3 - D^2)}{R(1 - D)^2} \\
 P_{L_{loss_{total}}} &= \left( \frac{2V_o}{R(1 - D)} \right)^2 r_{L1} + \left( \frac{2V_o}{R(1 - D)^2} \right)^2 r_{L2} \\
 P_o &= \frac{V_o^2}{R} \\
 V_o &= \frac{V_{in} R (1 - D)^2 (3 - D^2)}{R(1 - D)^4 + 4r_{L1}(1 - D)^2 + 4r_{L2}}
 \end{aligned} \tag{19}$$

where  $r_{L1}$  and  $r_{L2}$  are parasitic resistances of  $L_1$  and  $L_2$ .

It can be seen that the non-ideal gain depends on load resistance ( $R$ ) and parasitic resistances. The variation of this gain with duty-cycle is as shown in Figure 6. As the load resistance is decreased, the voltage gain also reduces for the same value parasitic resistances.



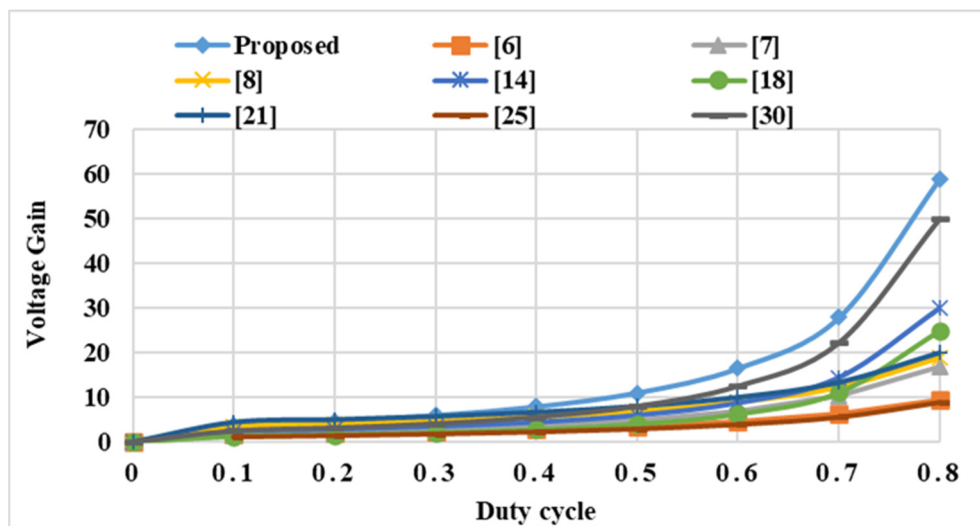
**Figure 6.** Non-ideal gain of the proposed converter.

#### 4. Comparison with Other Recent Topologies

The comparison of the proposed converter with similar kinds of existing converters is shown in Table 2. The voltage gain of the proposed is compared with the other converters and presented in Figure 7. The proposed converter can achieve a voltage gain of 16 at a low duty ratio of around 0.6, which is relatively high compared to the other converter presented in Figure 7. The converter proposed in [7] has four inductors, but its gain is much less than the proposed converter. As discussed earlier, the gain of the CQBC presented in [18] is much less than the proposed converter.

**Table 2.** Comparison of the proposed topology with other similar topologies.

Topology	N <sub>L</sub> (Inductors)	N <sub>C</sub> (Capacitors)	N <sub>SW</sub> (Switches)	N <sub>D</sub> (Diodes)	M (V <sub>o</sub> /V <sub>in</sub> )	S (V <sub>s</sub> /V <sub>in</sub> )
[6]	2	4	1	4	$\frac{3+D}{2(1-D)}$	$\frac{1}{1-D}$
[7]	4	1	2	7	$\frac{1+3D}{(1-D)}$	$\frac{1+D}{1-D}$
[8]	2	3	2	3	$\frac{3+D}{(1-D)}$	$\frac{1}{1-D}$
[14]	1+1 coupled inductor	3	1	5	$\frac{2-D}{(1-D)^2}$ $n = 1$	$\frac{2}{1-D}$
[18]	2	2	1	3	$\frac{1}{(1-D)^2}$	$\frac{1}{(1-D)^2}$
[21]	2	4	2	4	$\frac{4}{(1-D)}$	$\frac{1}{1-D}$
[25]	2	3	1	2	$\frac{1+D}{1-D}$	$\frac{1}{1-D}$
[30]	3	3	1	5	$\frac{2}{(1-D)^2}$	$\frac{1}{(1-D)^2}$
[31]	3	3	1	5	$\frac{1}{(1-D)^3}$	$\frac{1}{(1-D)^3}$
Proposed	2	4	2	4	$\frac{3-D^2}{(1-D)^2}$	$S_1 = \frac{1}{1-D}$ $S_2 = \frac{1}{(1-D)^2}$



**Figure 7.** Ideal voltage gain comparison with other existing topologies.

Similarly, the converter proposed in [21] has utilized two switches, and the total number of components used in the converter is also the same as the proposed converter; still, its gain is high. The converter proposed in [30] has twice the gain as compared to CQBC, but even with three inductors and the same number of components, its gain is less than the proposed converter. The normalized voltage stress across the proposed converter switches as a function of voltage gain is plotted in Figure 8.

The voltage stress across switch  $S_1$  is the lowest among all the topologies, and the stress across switch  $S_2$  up to a gain of 11 times is also less than the topologies proposed [7,14,18,25,30]

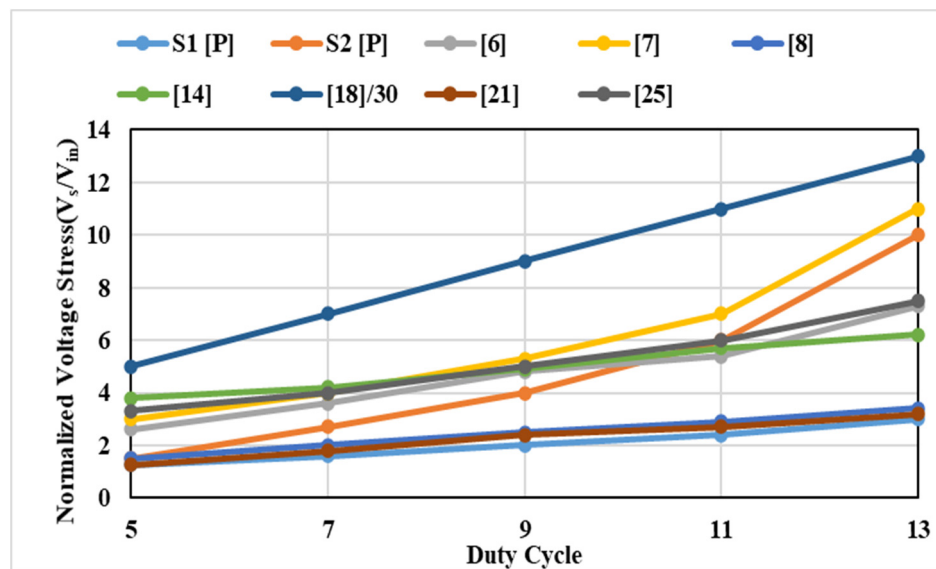


Figure 8. Normalized Voltage stress vs. Voltage Gain.

## 5. Experimental Verification of the Proposed Converter

A laboratory prototype is developed by using the power circuit board technique (PCB). The main circuit and gate driver circuit with various components are soldered on the power circuit board, as shown in Figure 9. The testing parameters are shown in Table 3, and the experimental setup is presented in Figure 10. Two power supplies are used—one for the gate driver circuit and another for the main converter circuit.

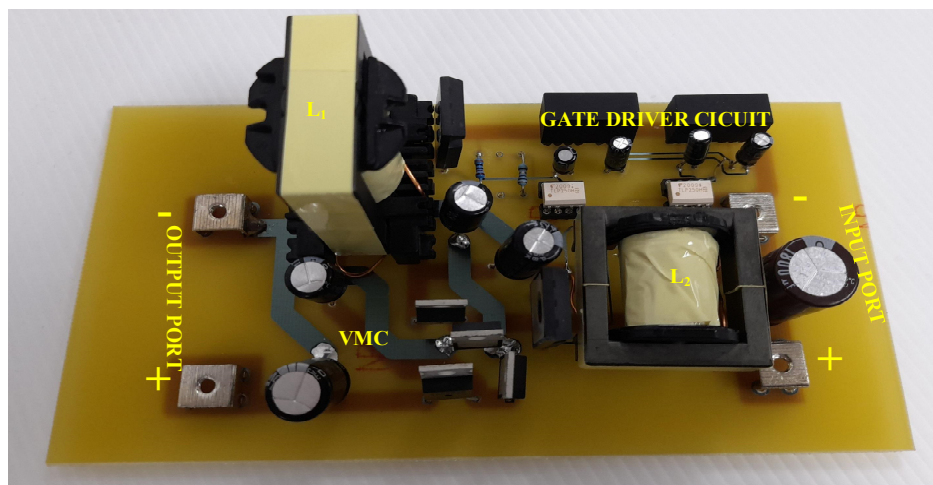
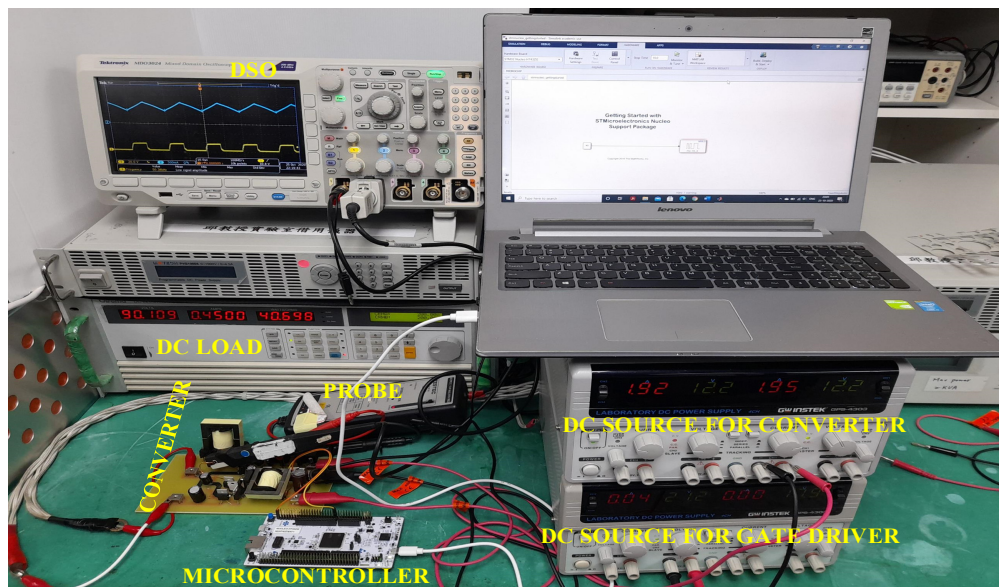


Figure 9. Prototype of the proposed converter.

**Table 3.** Specifications of the proposed converter.

Elements	Specification
Input Voltage ( $V_{in}$ )	12 V/20 V
Maximum Output Power	200 W
Switching Frequency	50 kHz
Load Resistance	$R = 200/250 \, \Omega$ , Electronic load simulator
Inductors	$L_1 = 550 \, \mu\text{H}$ and $L_2 = 330 \, \mu\text{H}$
Capacitors	$C_1 = 220 \, \mu\text{F}/63\text{V}$ , $C_2 = C_3 = 47 \, \mu\text{F}/100 \text{ V}$ and $C_4 = 47 \, \mu\text{F}/200 \text{ V}$
Power MOSFET ( $S_1$ and $S_2$ )	SPW52N50C3
Diodes ( $D_1$ , $D_2$ , $D_3$ and $D_4$ )	PFCD86
Gate Drivers IC	TLP250H
Gate Driver Voltage Regulator IC	MCWI03-48S15
Microcontroller	STM32 Nucleo H743ZI2

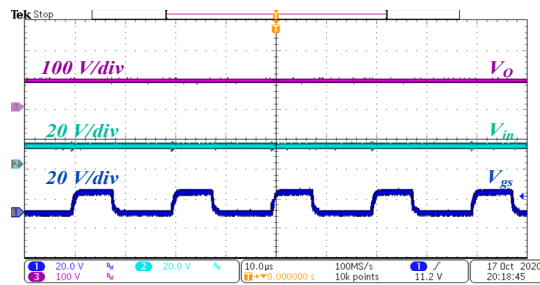
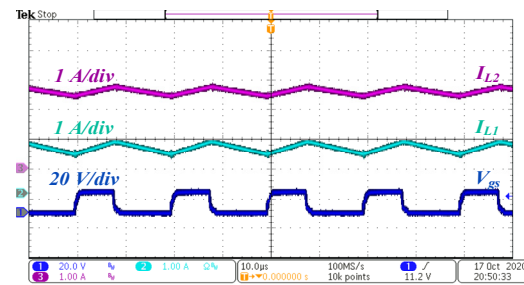
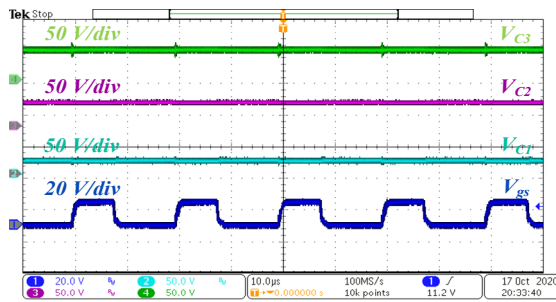
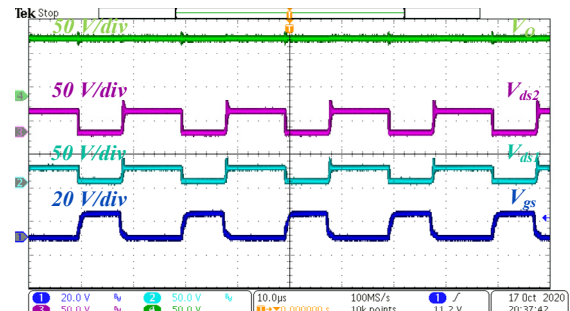
**Figure 10.** Experimental Setup.

The hardware prototype tested at a duty ratio of 0.4, and the results are presented in Figure 10.

### 5.1. Experimental Results at $V_{in} = 12 \text{ V}$

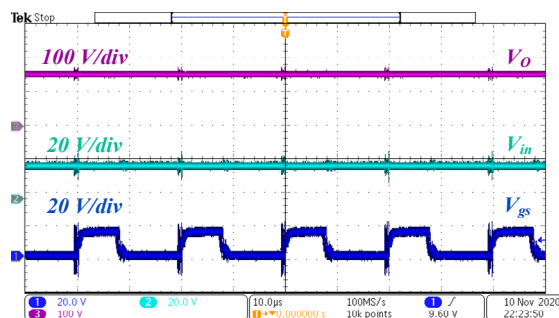
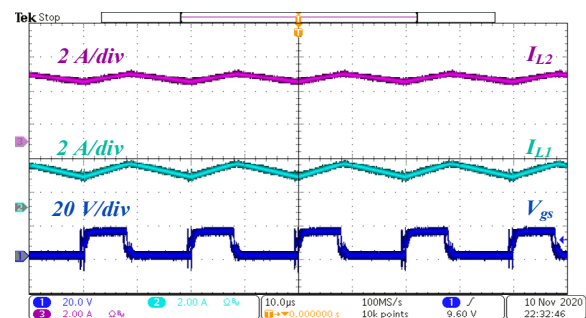
As shown in Figure 11a, the measured output voltage is 90 volts, which is slightly lower than the ideal calculated voltage at 0.4 duty ratio and 12 volts input. It can further be observed that the inductor currents are continuous, and the converter is operating in CCM. The capacitor voltages are shown in Figure 11c. The measured voltage across capacitor  $C_1$  is 19.9 volts; for  $C_2$ , it is 37.5 volts, and for  $C_3$ , it is 49 volts. The voltage stress across the switches is lower than half of the output voltage. In the case of the first switch, the stress is around 20 volts and in the case of the second switch is around 35 volts, as shown in Figure 11d. It can be validated from hardware results that the converter is working satisfactorily and the high voltage gain along with reduced voltage stresses.

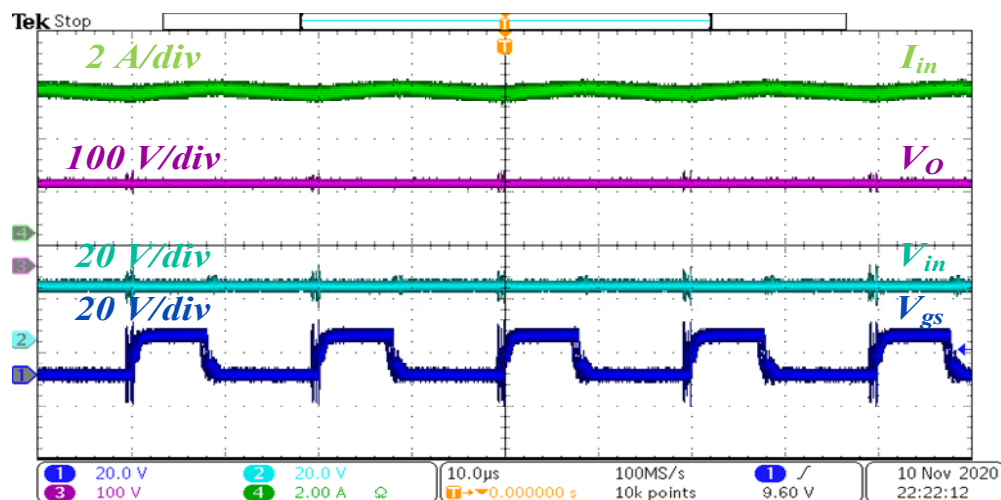


(a) Output voltage at 12V input and  $D = 0.4$ (b) Inductor currents of  $L_1$  and  $L_2$  at  $D = 0.4$ (c) Capacitor voltages of  $C_1$ ,  $C_2$ , and  $C_3$  at  $D = 0.4$ (d) Output voltage and voltage stress across switch  $S_1$  and  $S_2$  at  $D = 0.4$ **Figure 11.** Related waveforms of the proposed converter at  $V_{in} = 12$  V.

## 5.2. Experimental Results at $V_{in} = 20$ V

Figure 12 shows the experimental waveforms of the proposed converter at  $V_{in} = 20$  V. The output voltage is found to be 155 V. The inductor currents are also continuous and are shown in Figure 12b. In Figure 12c, the input current is shown. The average value of input current is equal to 4.8 A. It can be observed that the input current is continuous, which is another advantage of the converter. The continuous input current is a desirable feature of this converter, especially for solar PV applications.

(a) Output voltage at 20 V input and  $D = 0.4$ (b) Inductor currents of  $L_1$  and  $L_2$  at  $D = 0.4$ **Figure 12.** Cont.

(c) Output voltage at 20 V input and  $D = 0.4$ **Figure 12.** Related waveforms of the proposed converter at  $V_{in} = 20$  V.

## 6. Conclusions

A voltage multiplier circuit based quadratic boost converter has been realized, and a prototype is developed for energy storage application. Comparing the proposed topology with other recently proposed boost and quadratic boost topology shows its better performance in terms of voltage gain and voltage stress across the switch for a wide range of duty cycles. Loss analysis with the converter's thermal model also shows efficiency above 91% for the entire 200 Watt input power operation. The peak efficiency of 94.5% is obtained for an input voltage of 24 Volts. The proposed converter with continuous input current would be a strong candidate for energy storage and renewable energy application.

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