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# Comparison of Temperature Dependent Carrier Transport in FinFET and Gate-All-Around Nanowire FET

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**Abstract:** The temperature dependent carrier transport characteristics of n-type gate-all-around nanowire field effect transistors (GAA NW-FET) on bulk silicon are experimentally compared to bulk fin field effect transistors (FinFET) over a wide range of temperatures (25–125 °C). A similar temperature dependence of threshold voltage ( $V_{TH}$ ) and subthreshold swing ( $SS$ ) is observed for both devices. However, effective mobility ( $\mu_{eff}$ ) shows significant differences of temperature dependence between GAA NW-FET and FinFET at a high gate effective field. At weak  $N_{inv}$  ( $= 5 \times 10^{12} \text{ cm}^2/\text{V}\cdot\text{s}$ ), both GAA NW-FET and FinFET are mainly limited by phonon scattering in  $\mu_{eff}$ . On the other hand, at strong  $N_{inv}$  ( $= 1.5 \times 10^{13} \text{ cm}^2/\text{V}\cdot\text{s}$ ), GAA NW-FET shows 10 times higher  $d\mu_{eff}/dT$  and 1.6 times smaller mobility degradation coefficient ( $\alpha$ ) than FinFET. GAA NW-FET is less limited by surface roughness scattering, but FinFET is relatively more limited by surface roughness scattering in carrier transport.

**Keywords:** GAA NW-FET; FinFET; temperature dependence; effective mobility; surface roughness scattering

## 1. Introduction

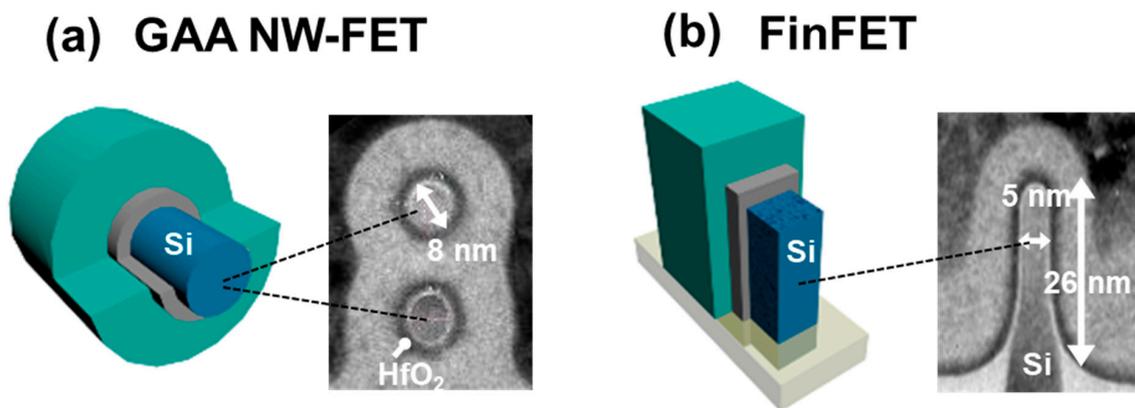
For several years, fin field effect transistors (FinFETs) have been used industry to continue CMOS down-scaling. However, as FinFETs also have been look forward to being further scaled, critical issues such as drain-induced barrier lowering, threshold voltage ( $V_{TH}$ ) roll-off and parasitic resistance occur, etc. [1]. In order to alleviate these issues, the gate-all-around nanowire field effect transistors (GAA NW-FETs) have been recently proposed as a promising device to replace FinFETs, due to their superior gate control [2,3]. The better electrostatic gate control provided by the surrounding gate enables a more aggressive gate length scaling than FinFETs [4–6]. However, advanced fabrication technologies remain challenging, e.g., the GAA structure formation [7] and doping process [8] to restrain a naturally formed parasitic channel based on bulk FinFETs. Such device fabrication directly affects key device parameters ( $V_{TH}$ , subthreshold swing ( $SS$ ) and effective mobility ( $\mu_{eff}$ ), etc.). Furthermore, the electrical characteristics of semiconductors such as band gap [9], carrier density [10], mobility [11], velocity saturation [12],  $V_{TH}$  [13], and leakage current [14] depend strongly on the temperature resulting in a change of circuit performance as a function of the operating temperature. Therefore, it is important to explore the possible degradation at a high temperature which might lead to performance degradation

in a hot temperature corner. It is helpful to understand and to model the temperature dependence of GAA devices to enable the design of circuits in this technology.

In this study, we investigated the high temperature characteristics of vertical 2-stacked n-channel metal oxide semiconductor (NMOS) GAA NW-FETs and FinFETs in order to understand the potential differences between the two devices.

## 2. Materials and Methods

The cross-sectional transmission electron microscopy (TEM) images [8,15] of the devices under test are shown in Figure 1. Both GAA NW-FETs and FinFETs were fabricated using the high-k replacement metal gate (HK-RMG) process [7,16,17]. The diameter of nanowire ( $D_{nw}$ ) is 8 nm for GAA NW-FETs. In the case of FinFETs, the fin width ( $W_{fin}$ ) is 5 nm and the fin height ( $H_{fin}$ ) was 26 nm.



**Figure 1.** TEM cross-sectional images of NMOS: (a) gate-all-around nanowire field effect transistors (GAA NW-FETs); and (b) fin field effect transistors (FinFETs). Two nanowires are stacked in GAA NW-FETs.

Both GAA NW-FETs and FinFETs were fabricated based on a conventional bulk FinFETs process flow [15] with the following particularities in the case of GAA NW-FETs, as shown in Figure 2. First, in order to suppress the short channel effect, a ground plane (GP) isolation implant was used [8]. Implanted boron reduced the punch through via a parasitic channel underneath the bottom of the nanowire so that it improves the gate control in the subthreshold region. The second difference is the channel formation process. For fin formation on both devices, a self-aligned double patterning (SADP) process is conducted using SiN spacers while maintaining uniform shallow trench isolation (STI) filling. To make nanowires, SiGe/Si/SiGe/Si epitaxial layers were grown before the SADP process, and the sacrificial SiGe layer was removed with the vapor HCl etch process before the HK-RMG process. Furthermore, the temperature of the STI densification step was reduced from 1050 to 750 °C to avoid SiGe/Si intermixing and a consequent loss of nanowire shape controllability [18]. In this study, gate lengths  $L_G = 30$  nm and 70 nm were used for the electrical characterization.

The Keysight B1500A was used for the electrical measurements. The gate-source bias ( $V_{GS}$ ) was swept from  $-0.5$  to  $1.5$  V (step = 50 mV) in the linear region at  $V_{DS} = 50$  mV. The electrical characterizations were carried out under various temperature conditions from 25 to 125 °C.

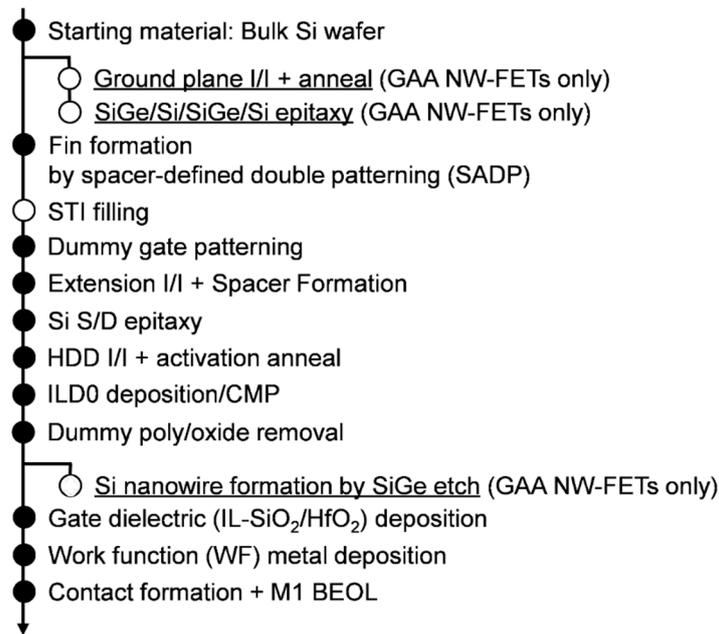


Figure 2. Fabrication process flow in FinFET and GAA NW-FET.

### 3. Results

The drain current ( $I_{DS}$ ) at different temperature conditions are shown for NMOS GAA NW-FET (Figure 3a) and FinFET (Figure 3b). A slightly higher  $I_{DS}$  is observed for GAA NW-FET (~6%, at 25 °C) compared to FinFET. For both GAA NW-FET and FinFET, the  $I_{DS}$  decreased as the temperature increased at the same overdrive voltage ( $V_{OV} = V_{GS} - V_{TH}$ ), which shows the phonon scattering limited mobility behavior [19].

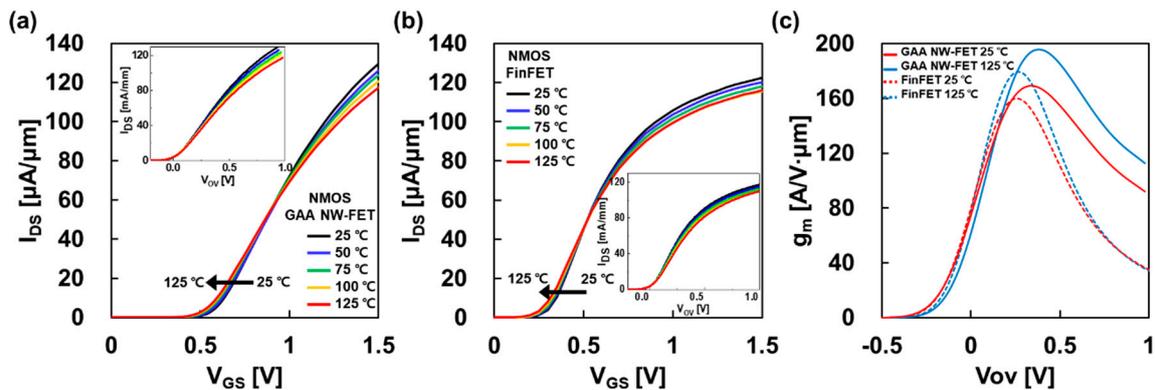
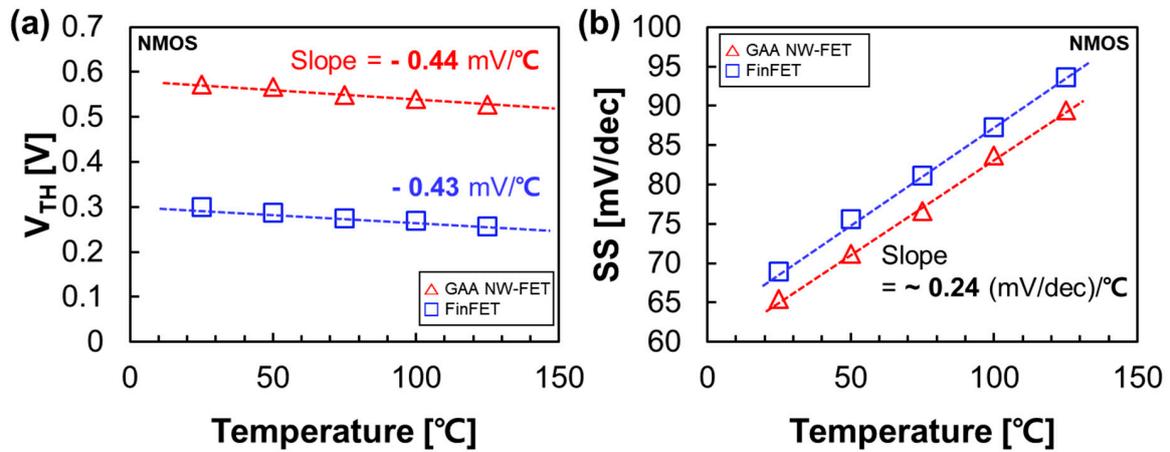


Figure 3. Measured  $I_{DS}$ - $V_{GS}$  curves (linear region,  $V_{DS} = 50$  mV) under various temperature conditions from 25 to 125 °C for (a) GAA NW-FET. (b) FinFET with  $L_G = 30$  nm. Insets:  $I_{DS}$ - $V_{OV}$  ( $V_{OV} = V_{GS} - V_{TH}$ ) curves. (c)  $g_m$ - $V_{GS}$  curves for GAA NW-FET and FinFET for 25 and 125 °C.

It can also be seen that  $V_{TH}$  down-shifted from 0.56 to 0.52 V for GAA NW-FET and 0.30 to 0.27 V for FinFET as the measurement temperature increases. In Figure 3c, compared to the transconductance ( $g_m$ ) at different temperatures, FinFET and GAA NW-FET show the disparate degree of reduction at the same  $V_{OV}$ . For example, as the measurement of the temperature increases, the  $g_m$  of FinFET and GAA NW-FET decreases 0.4% (from 127.1 to 126.6  $\mu\text{S}/\mu\text{m}$ ) and 12.8% (from 188.2 to 164.1  $\mu\text{S}/\mu\text{m}$ ) at  $V_{OV} = 0.5$  V, respectively.

The temperature dependences of  $V_{TH}$  for GAA NW-FET and FinFET are plotted using the maximum transconductance method [20] in Figure 4a.



**Figure 4.** (a)  $V_{TH}$  as a function of temperature for GAA NW-FET and FinFET from Figure 3. Similar temperature sensitivities of  $V_{TH}$  are observed for both GAA NW-FET and FinFET. (b) Subthreshold swing (SS) as a function of temperature also shows same slopes for both GAA NW-FET and FinFET.

The  $V_{TH}$  as a function of temperature can be explained by the following equation [13]:

$$\frac{dV_{TH}}{dT} = \frac{d\phi_F}{dT} \left[ k \sqrt{\frac{q\epsilon_{si}N_{eff}}{\phi_F C_{ox}^2} + 2} + \frac{C_{it}}{C_{ox}} \right] \quad (1)$$

where  $\phi_F$  [eV] is the Fermi potential,  $q$  [C] the electron charge,  $\epsilon_{si}$  [F/cm] the silicon permittivity,  $N_{eff}$  [cm<sup>-3</sup>] the effective doping level,  $C_{ox}$  [F/cm<sup>2</sup>] the oxide capacitance, and  $C_{it}$  [F/cm<sup>2</sup>] the interface trap density, respectively, in Equation (1). The fitting parameter  $k$  is 1 for partially depleted devices and closed to 0 for fully depleted channels. The  $V_{TH}$  is predicted to decrease at a high temperature due to the reduction of  $\phi_F$  [21]. The  $\phi_F$  decreased by excited carriers from the valence band to conduction band when the temperature rises. In this study, a similar temperature dependent  $V_{TH}$  is observed between GAA NW-FET ( $dV_{TH}/dT = -0.44$  mV/°C) and FinFET ( $dV_{TH}/dT = -0.43$  mV/°C). In the case of bulk planar NMOS,  $dV_{TH}/dT$  was approximately  $-0.7$  mV/°C [22]. For the GAA NW-FET and FinFET, the lowering of  $dV_{TH}/dT$  is attributed to the fully depleted channel with the thinning of the channel.

#### 4. Discussion

To understand the temperature dependence of SS, the parameter of the on-off switching capability, the following equation is used [23]:

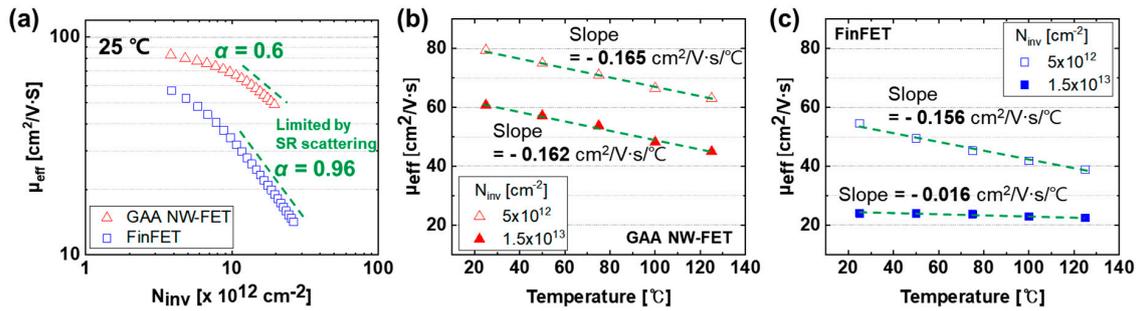
$$SS \approx \frac{k_B T}{q} \ln 10 \left[ 1 + \frac{(C_D + C_{it})}{C_{ox}} \right] \quad (2)$$

Here,  $C_D$  is the depletion capacitance,  $k_B$  the Boltzmann's constant, and  $T$  the temperature, respectively. The channel region of GAA NW-FET and FinFET is sufficiently shallow ( $D_{nw} = 8$  nm for GAA NW-FET and  $W_{fin} = 5$  nm for FinFET) so that the channel is fully depleted. Thus, the depletion charge ( $Q_D$ ) of these devices are not a function of  $V_G$ , and  $C_D (= dQ_D/dV_G)$  is negligible [23]. GAA NW-FET shows smaller SS at any temperature condition (SSs of GAA NW-FET and FinFET are about 65 and 69 mV/dec at 25 °C, respectively). The large SS is induced by poor gate control, punch through, and  $C_{it}$ . Similar to  $dV_{TH}/dT$ , the  $dSS/dT$  for both devices is approximately equal to  $\sim 0.24$  mV/dec/°C, as shown in Figure 4b. Thus, the identical slope of Figure 4b shows  $\ln 10 [1 + C_{it}/C_{ox}]$  is same for both devices. By considering identical  $dSS/dT$  and similar  $dV_{TH}/dT$  between GAA NW-FET

and FinFET,  $C_{it}$  is also regarded as identical ( $C_{it} = 6.28 \times 10^{-7}$  F/cm<sup>2</sup> when the capacitance equivalent thickness was 1.1 nm for both devices). In Figure 5, the temperature dependent  $\mu_{eff}$  is investigated for  $L_G = 70$  nm. The  $\mu_{eff}$  was experimentally extracted from [24]:

$$\mu_{eff} = \frac{L_{eff}}{W_{eff}} \frac{g_D}{qN(V_{GS})} \Big|_{V_{DS} \rightarrow 50 \text{ mV}} \quad (3)$$

where  $g_D$  [A/V] is the drain conductance,  $V_{GS}$  the gate-source voltage,  $V_{DS}$  the drain-source voltage, and  $W_{eff}$  and  $L_{eff}$  the effective width and length of the channel, respectively.  $qN(V_{GS})$  was calculated in the strong inversion region assuming by  $qN(V_{GS}) = C_{ox} (V_{GS} - V_{TH})$ .



**Figure 5.** Effective mobility ( $\mu_{eff}$ ) behavior comparison between GAA NW-FET and FinFET with  $L_G = 70$  nm; (a)  $\mu_{eff}$ - $N_{inv}$ . Temperature dependence of  $\mu_{eff}$  for (b) GAA NW-FET and (c) FinFET.

From Matthiessen’s rule, the  $\mu_{eff}$  is composed of several mobility limited scattering mechanisms such as Coulomb, phonon, and surface roughness (SR) [25]. When a device is suffering from serious SR scattering, a large mobility degradation can be observed at high  $V_{OV}$  compared to the mobility behavior limited by phonon scattering, etc. [26].

The mobility limited by SR scattering is analyzed quantitatively by the following relationship [11,27]:

$$\mu_{SR} \propto \frac{E_{eff}^{-\alpha}}{\Delta^2 \lambda^2} \quad (4)$$

where  $E_{eff}$  is the effective field across the channel, which can be substituted to  $N_{inv}$  proportional to  $E_{eff}$ ,  $\Delta$  the rms value of the SR, and  $\lambda$  its correlation length. The  $\mu_{SR}$  is inversely proportional to the mobility degradation coefficient  $\alpha$ . The extracted  $\alpha$  of GAA NW-FET is 0.6, which is smaller than that of FinFET (0.96). This means that less SR scattering is shown for GAA NW-FET compared to FinFET (Figure 5a). In addition, the  $\mu_{SR}$  has weak temperature dependence compared to the mobility limited by phonon scattering [28]. GAA NW-FET (Figure 5b) shows a stronger temperature dependent  $\mu_{eff}$  than FinFET (Figure 5c). These are investigated with two operating conditions: at weak  $N_{inv} = 5 \times 10^{12}$  and strong  $N_{inv} = 1.5 \times 10^{13}$  cm<sup>2</sup>/V.s. At weak  $N_{inv}$ , similar  $d\mu_{eff}/dT$  is observed between both devices ( $-0.165$  for GAA NW-FET and  $-0.156$  cm<sup>2</sup>/V.s/°C for FinFET) because the phonon scattering is dominant than the SR scattering at low  $E_{eff}$ . At strong  $N_{inv}$ , on the other hand, the  $\mu_{eff}$  of GAA NW-FET is further degraded for a rising temperature than FinFET. This is another evidence that FinFETs are suffering from the SR scattering than GAA NW-FETs ( $-0.162$  for GAA NW-FET and  $-0.016$  cm<sup>2</sup>/V.s/°C for FinFET). At strong  $N_{inv}$ , the  $d\mu_{eff}/dT$  is moderated approximately 18% compared to the weak  $N_{inv}$  region for GAA NW-FET, but it is dramatically changed (90%) for FinFET. At 25 °C, the  $\mu_{eff}$  of GAA NW-FET decreases by 23.4% between weak  $N_{inv}$  and strong  $N_{inv}$ , whereas FinFET’s decrease is more pronounced (56.1%). At  $V_{OV} = 0.5$  V, the smaller  $g_m$  for FinFET ( $= 127.1$  at 25 °C, but 188.2  $\mu\text{S}/\mu\text{m}$  in the case of GAA NW-FET) is consistent with such different degrees of SR scattering for both devices.

The reduced SR scattering for GAA NW-FET could be assisted by a round-shaped NW channel formation process using a vapor HCl etch. The surface roughness of GAA NW-FET channel is softened

by the vapor HCl etching process. Thus, at a large  $V_{OV}$ , the relatively higher value and slower degradation of  $g_m$  (in Figure 3c) and  $\mu_{eff}$  (in Figure 5a) in GAA NW-FET could be from the suppression of SR scattering in the channel compared to FinFET.

## 5. Conclusions

In this work, the temperature dependent characteristics of NMOS GAA NW-FETs have been investigated comparing with FinFET. In GAA NW-FET, the experimental  $I_{DS}$ - $V_{GS}$  characteristics show higher  $I_{DS}$  and better SS than in FinFET from 25 to 125 °C. The modulation trend of  $V_{TH}$  and SS with temperature is not significantly different between GAA NW-FET and FinFET. At weak  $N_{inv}$ ,  $\mu_{eff}$  is mainly limited by phonon scattering for both GAA NW-FET and FinFET. However, at strong  $N_{inv}$ , the  $\mu_{eff}$  of GAA NW-FET is less impacted by the SR scattering. FinFET shows smaller  $d\mu_{eff}/dT$  ( $\sim -0.162$  cm<sup>2</sup>/V·s/°C) and higher mobility degradation coefficient  $\alpha$  (0.96), compared to that of GAA NW-FET ( $\sim -0.016$  cm<sup>2</sup>/V·s/°C and 0.6, respectively). This means that the carrier transport in GAA NW-FET is not mainly limited by SR scattering but phonon scattering at high  $N_{inv}$ . In the case of FinFET, the SR scattering mainly limits the carrier transport at high  $N_{inv}$ .

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**Conflicts of Interest:** The authors declare no conflicts of interest.

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