

Article

A Full Ka-Band CMOS Amplifier Using Inductive Neutralization with a Flat Gain of 13 ± 0.2 dB

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Abstract: This paper presents a CMOS wideband amplifier operating in the full Ka-band, with a low gain variation. An inductive neutralization is applied to the amplifier to compensate for the gain roll-off in the high-frequency region. Neutralization inductance is carefully determined considering the tradeoff between stability and gain. To achieve a low gain variation over the full Ka-band, the amplifier employs the frequency staggering technique in which impedance matching for three gain stages is performed at different frequencies of 26, 34, and 42 GHz. The experimental results show that a peak gain of 13.2 dB is achieved at 39.2 GHz. The 3 dB bandwidth is from 23.5 to 41.7 GHz, which fully covers the Ka-band. Especially, the gain ripple of the amplifier is only 13 ± 0.2 dB over a wide bandwidth from 26.2 to 40.2 GHz. The input and output return loss values are better than -10 dB from 26.3 to 40.1 GHz and from 25.3 to 50 GHz, respectively. The DC power consumption is 18.6 mW.

Keywords: Ka-band; CMOS amplifier; inductive neutralization technique; frequency staggering technique; wideband flat gain



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1. Introduction

Owing to the demand for high-speed data transfer, 5G communication based on the millimeter wave has been actively developed. The global spectrum allocated for the 5G millimeter wave is mainly distributed in the Ka-band (26.5–40 GHz) [1,2]. Therefore, a wideband flat-gain amplifier operating in the full Ka-band is needed for implementing multistandard or ultrawideband radio systems supporting the global spectrum.

Conventionally, wideband amplifiers operating at several gigahertz have been implemented using a resistive feedback technique [3–5]. The resistive feedback makes the input impedance more resistive, thereby allowing wideband input matching and enhancing the linearity [6]. However, a disadvantage of the resistive feedback is that the gain decreases in the upper end of the bandwidth [7]. Therefore, multiple amplifying stages must be cascaded to compensate for the gain roll-off, which increases the overall DC power consumption. Recently, a feedback technique based on a transformer balun was proposed to achieve a wideband gain response with a compact size [8,9]. However, the complicated structure of the transformer balun makes it challenging to optimize the transformer parameters such as the primary and secondary inductances and the coupling coefficient to achieve both the wideband input matching and flat-gain response at the same time.

This paper presents a full Ka-band amplifier with a low gain variation. In the first gain stage, the inductive neutralization is adopted to compensate for the gain roll-off in the upper end of the Ka-band, while the frequency staggering is employed in the subsequent gain stages for wideband and flat-gain responses. In Section 2, the analysis and design of the amplifier are presented. The experimental results are presented in Section 3. Finally, the conclusions are drawn in Section 4.

2. Circuit Analysis and Design

Figure 1 shows a schematic of the full Ka-band flat-gain CMOS amplifier using the inductive neutralization and frequency staggering techniques. Three common-source (CS)

gain stages (M_1 , M_2 , and M_3) were cascaded to secure a sufficient gain. To accomplish a wideband flat-gain response over the full Ka-band, the inductive neutralization was applied to the first stage, while the frequency staggering was employed in the following interstage and output matching networks.

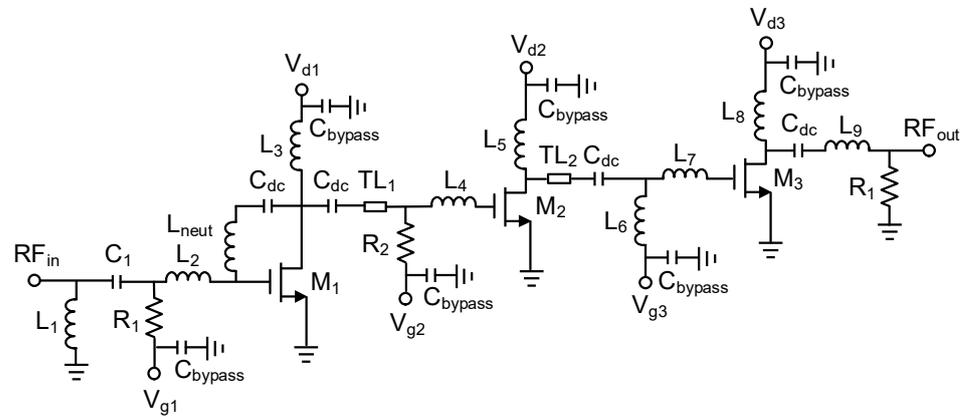


Figure 1. Schematic of the full Ka-band amplifier with flat gain.

2.1. Inductive Neutralization Technique

To achieve a high flat gain, the optimum transistor topology was determined first. Figure 2 shows the maximum stable gain (MSG) (or the maximum available gain (MAG)) [10] of various transistor topologies in the given 65 nm CMOS technology.

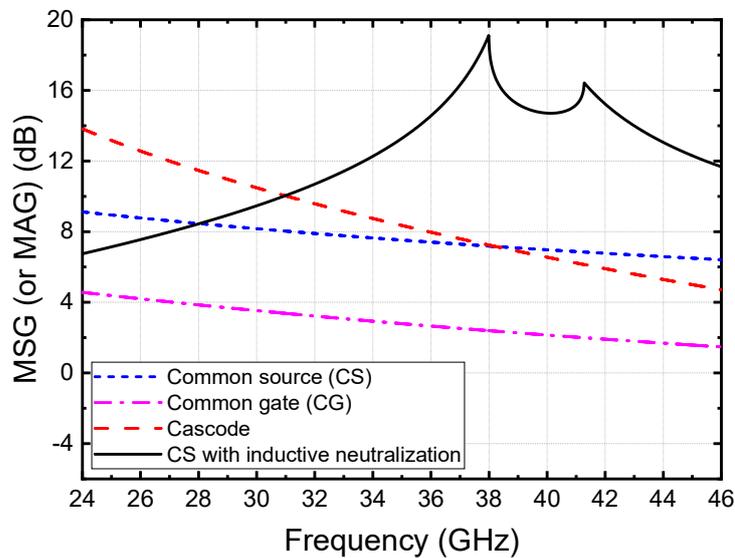


Figure 2. Comparison of MSG (or MAG) of different transistor topologies in a 65 nm CMOS technology.

For a fair comparison, the simulation conditions were set identical: the gate width and drain bias current of each transistor are 30 μm and 3.1 mA, respectively. Among the CS, common-gate (CG), and cascade topologies, the CS topology provides the highest gain beyond 38 GHz. However, the gain of the CS still gradually decreases as the frequency increases further than 38 GHz. To achieve a flat gain over the full Ka-band, a gain-boosting technique should be used to compensate for the gain roll-off at the upper end of the Ka-band.

In this research, we adopted the inductive neutralization technique in the CS to boost the gain. It is well known that the gate-drain capacitance C_{gd} degrades the forward gain of the transistor [11]. Therefore, by connecting a neutralization inductor (L_{neut}) between the gate and drain, C_{gd} is resonated with the inductor, and thus the MSG (or MAG) can

be boosted [12,13]. In Figure 2, the MSG (or MAG) of the CS topology with the inductive neutralization ($L_{\text{neut}} = 1.3 \text{ nH}$) is shown, which is higher than that of other topologies beyond 31 GHz. Moreover, the inductive neutralization changes the behavior of the MSG (or MAG) over the frequency. It is observed in Figure 2 that the peak of the MSG (or MAG) is pushed to a higher frequency region and, thus, can be located almost at the upper end of the Ka-band. This offsets the high loss of passive matching components and the resulting gain roll-off at the high frequencies.

While boosting the gain by resonating out the feedback capacitance C_{gd} , the inductive neutralization may disrupt the stability of the transistor. This is because positive feedback can be reinforced when the $C_{\text{gd}}-L_{\text{neut}}$ network operates far from the resonance. Therefore, the value of L_{neut} should be carefully determined considering a tradeoff between the gain and the stability. Figure 3 shows the simulated MSG (or MAG) and stability factor K at 39 GHz versus L_{neut} . The MSG (or MAG) has two peaks at $L_{\text{neut}} = 1.23$ and 1.44 nH , respectively. On the other hand, the K has a single peak at $L_{\text{neut}} = 1.3 \text{ nH}$ and decreases rapidly as L_{neut} deviates from 1.3 nH . The K becomes even below unity when $L_{\text{neut}} < 1.23 \text{ nH}$ or $L_{\text{neut}} > 1.44 \text{ nH}$. Hence, we chose L_{neut} of 1.3 nH , which results in MAG of 15.1 dB and K of 11.2 at 39 GHz . Notably, both MAG and K are boosted by inductive neutralization. The inductive neutralization with L_{neut} of 1.3 nH was applied to the first gain stage (M_1), which presents a high gain at the upper end of the Ka-band. It should be noted that the second and third gain stages (M_2 and M_3) have no inductive neutralization because they should present a high gain at lower frequencies, as described in Section 2.2.

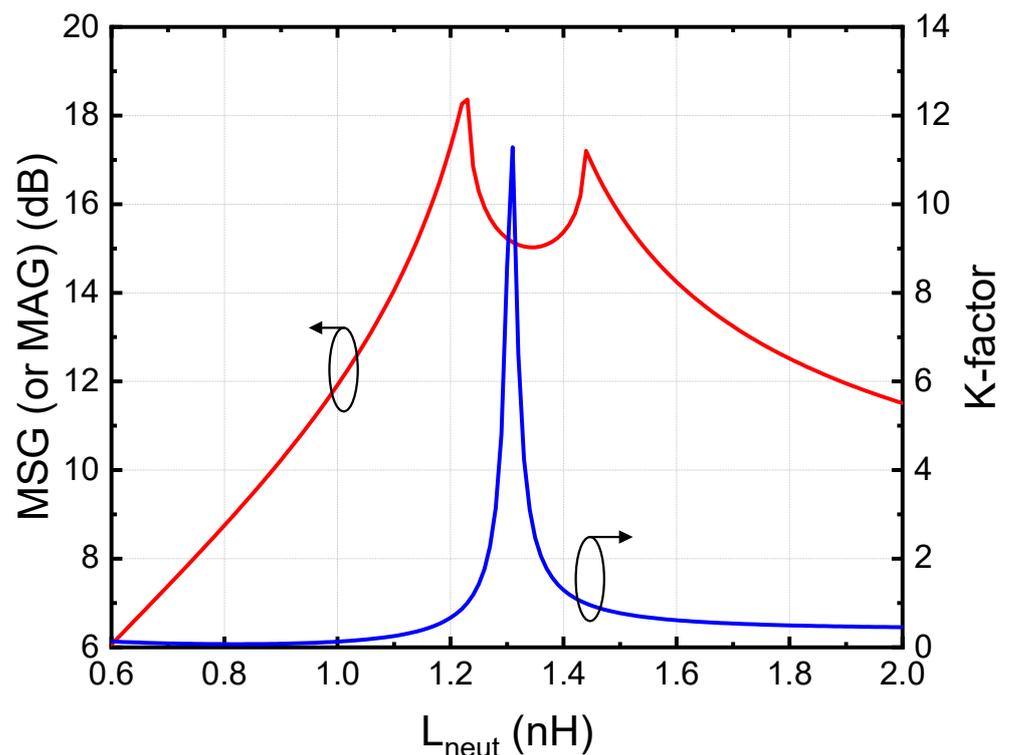


Figure 3. Simulated MSG (or MAG) and stability factor K at 39 GHz versus L_{neut} .

The input matching of the amplifier should operate in a wide bandwidth to suppress mismatch loss that occurs in the interconnection with other circuit blocks. The inductive neutralization of the first gain stage alters the input impedance of M_1 ; therefore, it should be considered in the input matching design shown in Figure 4. Specifically, the $C_{\text{gd}}-L_{\text{neut}}$ network brings the load impedance of M_1 (Z_{L1}) to the input of M_1 ($Z_{\text{in}1}$) when the operation is off the resonance frequency. Z_{L1} includes the drain bias network of M_1 (L_3 and C_{bypass}), the input impedance looking into M_2 , and the interstage matching between M_1 and M_2 . In

Figure 5, the impedances of the input matching network are shown as the frequency is swept from 26 to 40 GHz. The Z_{in1} with no Z_{L1} and L_{neut} included is dominantly determined by the gate capacitance and resistance, as expected, shown in line (a). However, Z_{in1} with Z_{L1} included, shown in line (b), and with both Z_{L1} and L_{neut} included, shown in line (c), are substantially different from line (a). Fortunately, L_{neut} induces a resonance behavior in Z_{in1} , thereby providing a wideband characteristic to the input reflection coefficient. Finally, the input impedance at the port (Z_{in}) is matched to 50Ω with L_1 , C_1 , and L_2 , shown in line (d).

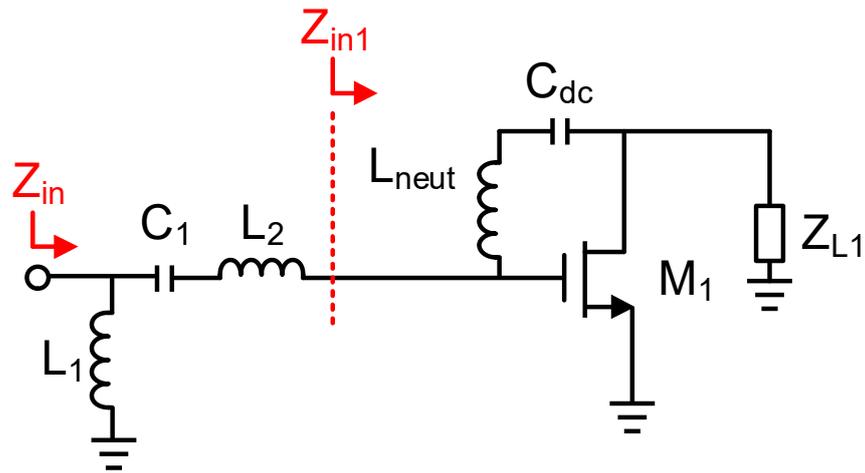


Figure 4. Input matching network of the first gain stage.

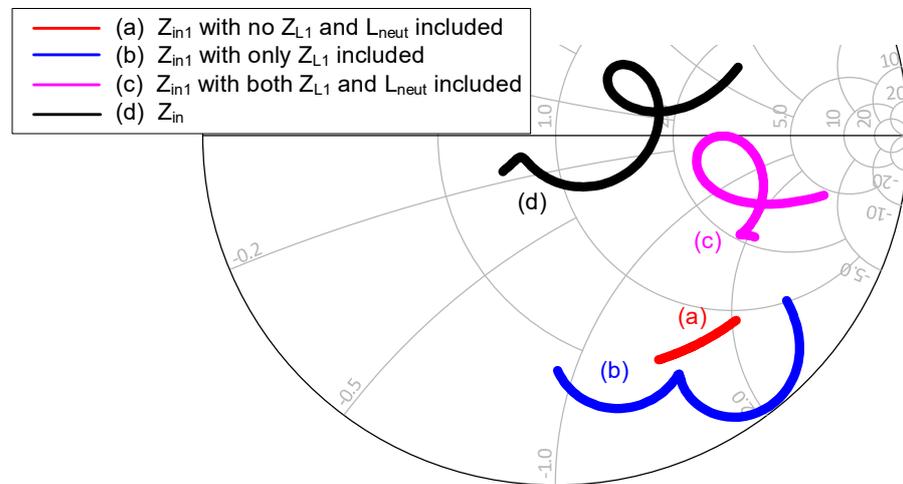


Figure 5. Loci of the input impedances from 26 to 40 GHz.

2.2. Frequency Staggering Technique

To achieve a flat gain over a wide frequency range, the center frequencies of three gain stages (M_1 , M_2 , and M_3) are intentionally staggered. Through the interstage and output impedance matching described below, the peak-gain frequencies of the first, second, and third stages are tuned to 42, 25.5, and 30.5 GHz, respectively, as shown in Figure 6.

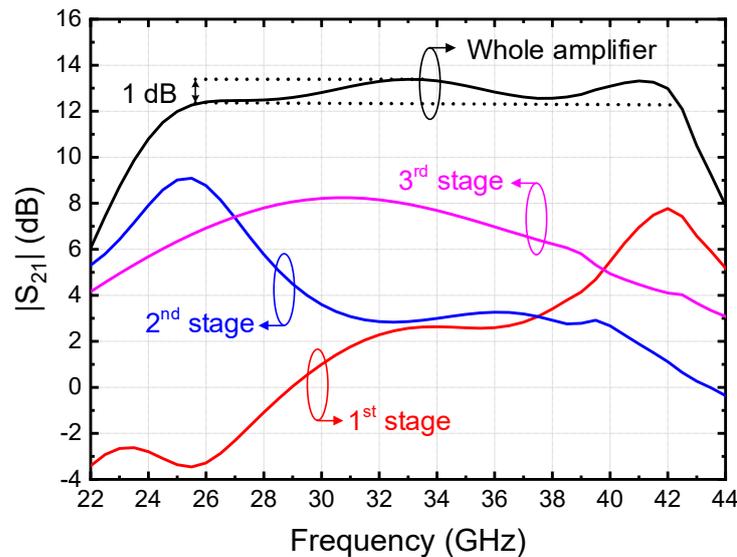


Figure 6. Gain of the three individual stages and the whole amplifier.

The ac equivalent circuit of the amplifier is drawn in Figure 7a. For the first interstage matching between M_1 and M_2 , the impedances seen looking into the output of M_1 (Z_{out1}) and the input of M_2 (Z_{in2}) are simulated as $Z_{out1} = 48.3 - j89.2 \Omega$ and $Z_{in2} = 14.2 - j71.9 \Omega$ at 42 GHz. For conjugate matching, Z_{in2} is transformed to Z_{out1}^* by an L-section network consisting of L_3 , L_4 , and TL_1 . As shown in Figure 7b, the series inductive components (L_4 and TL_1) bring Z_{in2} to $Z_{in2,1}$, which is located on a constant conductance circle of $\text{Re}\{1/Z_{out1}^*\}$. Then, a shunt inductor (L_3) transforms $Z_{in2,1}$ to $Z_{in2,2}$, which completes the conjugate matching to Z_{out1}^* . It should be noted that the value of L_3 determines the frequency at which the conjugate matching is satisfied. In Figure 7b, the locus of $Z_{in2,2}$ at 42 GHz is depicted as L_3 decreases from infinity to 0.1 nH. According to the plot, L_3 is chosen as 0.8 nH to achieve conjugate matching at 42 GHz. The final matching point of $Z_{in2,2}$ slightly deviates from Z_{out1}^* after fine optimization of the whole amplifier. The conjugate interstage matching between M_1 and M_2 at 42 GHz results in the gain peak of the first gain stage at the same frequency as that shown in Figure 6.

The second interstage matching between M_2 and M_3 is performed in a similar way to the first interstage matching. However, the matching frequency is intentionally changed to 26 GHz. As shown in Figure 7c, the input impedance of M_3 (Z_{in3}) is transformed to the conjugate of the output impedance of M_2 (Z_{out2}^*). The center frequency of the matching is tuned to 26 GHz by choosing the value of a shunt inductor (L_5) as 0.3 nH. It is noted that the second interstage matching is supposed to have the matching performance sensitive to the adjacent stages more than the first interstage matching. This is because the adjacent impedances are seen through C_{gd} of M_2 and M_3 , while C_{gd} of M_1 is diminished by the neutralization inductor L_{neut} . Therefore, an extra shunt inductor (L_6) is added as an additional degree of design freedom in the second interstage matching while minimizing the influence on the adjacent matching. The second interstage matching results in the gain peak of the second stage at 25.5 GHz, as observed in Figure 6.

The output matching is fulfilled by L_8 and L_9 at 34 GHz, which leads to the peak gain of the final stage at 30.5 GHz shown in Figure 6. It is noted that there is a slight difference between the matching frequency and the peak gain frequency of each individual stage. This is because the gain and bandwidth of the whole amplifier were re-optimized after combining the individual stages.

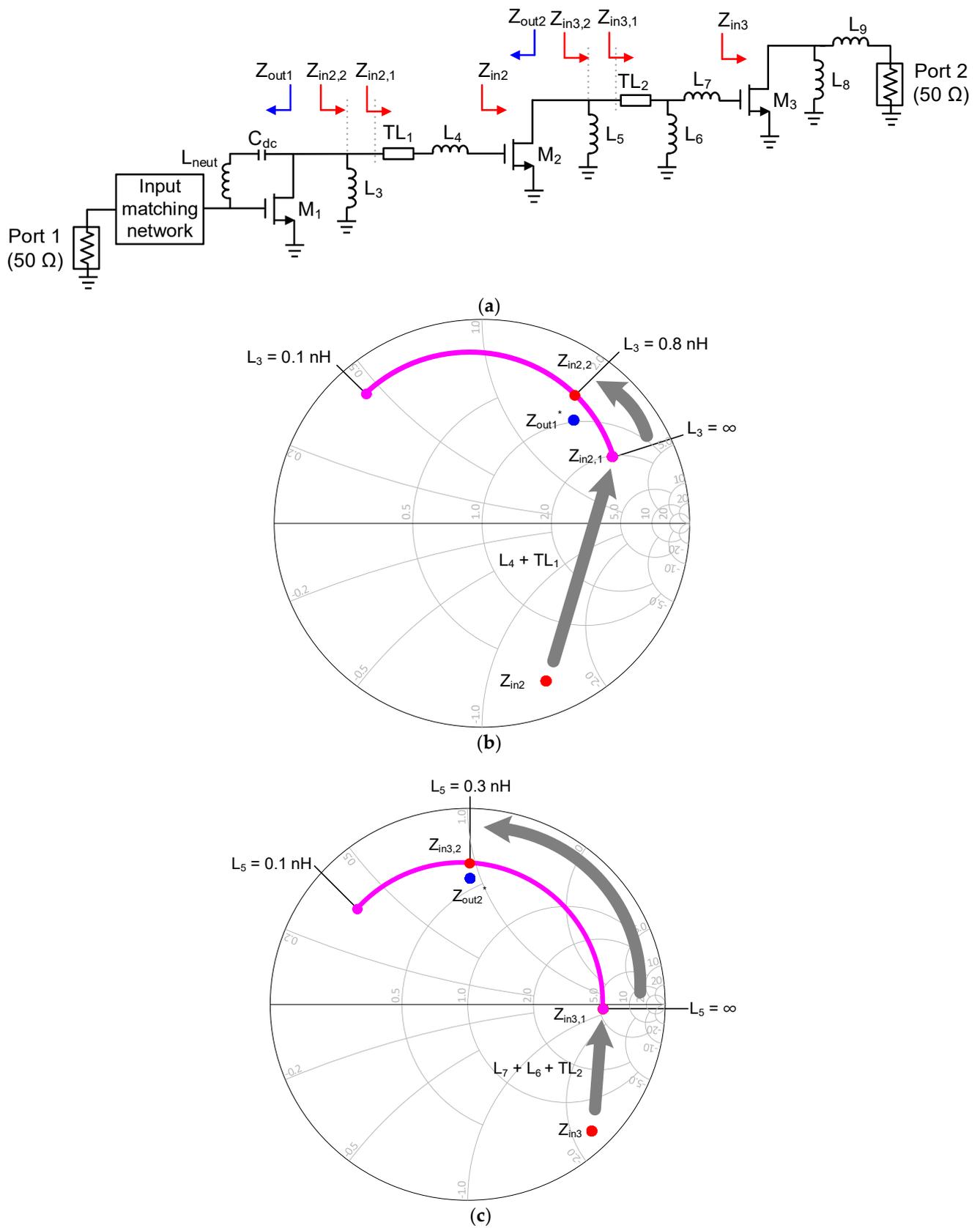


Figure 7. Interstage matching: (a) AC equivalent circuit of the amplifier; (b) first interstage matching at 42 GHz; (c) second interstage matching at 26 GHz.

Through the frequency staggering, the overall gain of the whole amplifier exhibits a flat response of 12.8 ± 0.5 dB from 25.6 to 42.4 GHz, covering the full Ka-band, as shown in Figure 6. After full electromagnetic simulation with Keysight ADS Momentum, the values of the matching components are slightly reoptimized considering the undesired magnetic and electric coupling between matching components and interconnection lines. The design parameter values of the full Ka-band amplifier are listed in Table 1.

Table 1. Design parameter values of the full Ka-band amplifier.

Parameters	Values	Parameters	Values
L_1	0.6 nH	C_1	0.41 pF
L_2	0.68 nH	R_1	200 Ω
L_3	0.8 nH	R_2	1000 Ω
L_4	0.45 nH	TL_1	265 μm
L_5	0.3 nH	TL_2	120 μm
L_6	0.7 nH	M_1 – M_3	$1 \times 30 \mu\text{m}$
L_7	0.2 nH	V_{g1}	1.1 V
L_8	0.65 nH	V_{g2}	1.1 V
L_9	0.27 nH	V_{g3}	0.9 V
L_{neut}	1.3 nH	V_{d1}	1.1 V
C_{bypass}	1.36 pF	V_{d2}	1.1 V
C_{dc}	1.36 pF	V_{d3}	1.1 V

3. Experimental Results

The full Ka-band amplifier was fabricated using a 65 nm CMOS technology. The chip micrograph is shown in Figure 8. The whole chip area including the probing pads and the core chip area were 1×0.7 and $0.5 \times 0.75 \text{ mm}^2$, respectively.

The measured S-parameters are shown in Figure 9. A peak gain of 13.2 dB was measured at 39.2 GHz. The 3 dB bandwidth was 18.2 GHz from 23.5 to 41.7 GHz, which covered the entire Ka-band frequencies. Specifically, from 26.2 to 40.2 GHz, the gain exhibited a flat response with a small variation, i.e., 13 ± 0.2 dB. The measured $|S_{11}|$ and $|S_{22}|$ were smaller than -10 dB from 26.3 to 40.1 GHz. The stability K-factor was calculated from the measured S-parameters, as shown in Figure 10. It was observed that the Ka-band amplifier was stable over the frequencies from DC to 50 GHz, which include both the operation and the out-of-band frequencies. The measured group delay is shown in Figure 11. The group delay was fairly flat in the frequency range between 22 and 46 GHz. The power measurement of the amplifier at 34 GHz is shown in Figure 12. The input 1 dB compression point (IP1dB) was -13.2 dBm. Figure 13 shows the measured IP1dB over the frequency. The IP1dB ranged from -13.2 to -16.6 dBm between 26 and 40 GHz.

In Table 2, the measured performances are summarized and compared with those of the previously reported CMOS Ka-band amplifiers. The amplifier in this study exhibited a superior gain flatness in the full Ka-band frequencies to the other state-of-the-art amplifiers.

Table 2. Performance comparison with previous CMOS-based Ka-band amplifiers.

Ref.	Technology	Peak Gain (dB)	$ S_{21} $ 3-dB BW (GHz)	$ S_{11} $ -10 dB BW (GHz)	Gain Flatness over Frequency	IP1dB (dBm)	DC Power Consumption (mW)	Core Chip Area ** (mm^2)
This work	65-nm CMOS	13.2	18.2 (23.5–41.7)	13.8 (26.3–40.1)	13 ± 0.2 dB over 26.2–40.2 GHz	-13.2	18.6	0.37

Table 2. Cont.

Ref.	Technology	Peak Gain (dB)	S ₂₁ 3-dB BW (GHz)	S ₁₁ −10 dB BW (GHz)	Gain Flatness over Frequency	IP1dB (dBm)	DC Power Consumption (mW)	Core Chip Area ** (mm ²)
[8]	65-nm CMOS	13.5	23.4 (19.2–42.6)	22.1 (16.8–38.9)	12.65 ± 0.85 dB over 21–41 GHz *	−9.8	6.36	0.13
[14]	65-nm CMOS	22.1	8.5 (24–32.5)	10 (30–40 *)	20.6 ± 1.5 dB over 24–32.5 GHz	−19	19.3	0.12
[15]	22 nm SOI CMOS	12.6	17 (23–40)	6 (25–31 *)	20.6 ± 1.5 dB over 24–32.5 GHz	−6	13	0.12
[16]	22 nm SOI CMOS	18.2	19 (24–43)	24 (20–44 *)	18 ± 1.1 dB over 24–29 GHz	−20.4	12.1	0.21
[17]	28-nm CMOS	18.6	4.3 (28.2–32.5 *)	7 (30–37)	17.1 ± 1.5 dB over 28.2–32.5 GHz	−25	9.7	0.23
[18]	40-nm CMOS	18.4	9.3 (25–34.3 *)	14 (26–40)	16.9 ± 1.5 dB over 25–34.3 GHz *	−13.4	21.5	0.26
[19]	45 nm SOI CMOS	20	20 (27–47.5 *)	19 (27–48)	19 ± 1.5 dB over 27–47.5 GHz	−19	58	0.2
[20]	90 nm SOI CMOS	13.8	15 (29–44)	21 (29–50 *)	12.3 ± 1.5 dB over 29–44 GHz	−10	18	0.48 ***

* Estimated from a plot of the article; ** excluding probing pads; *** including probing pads.

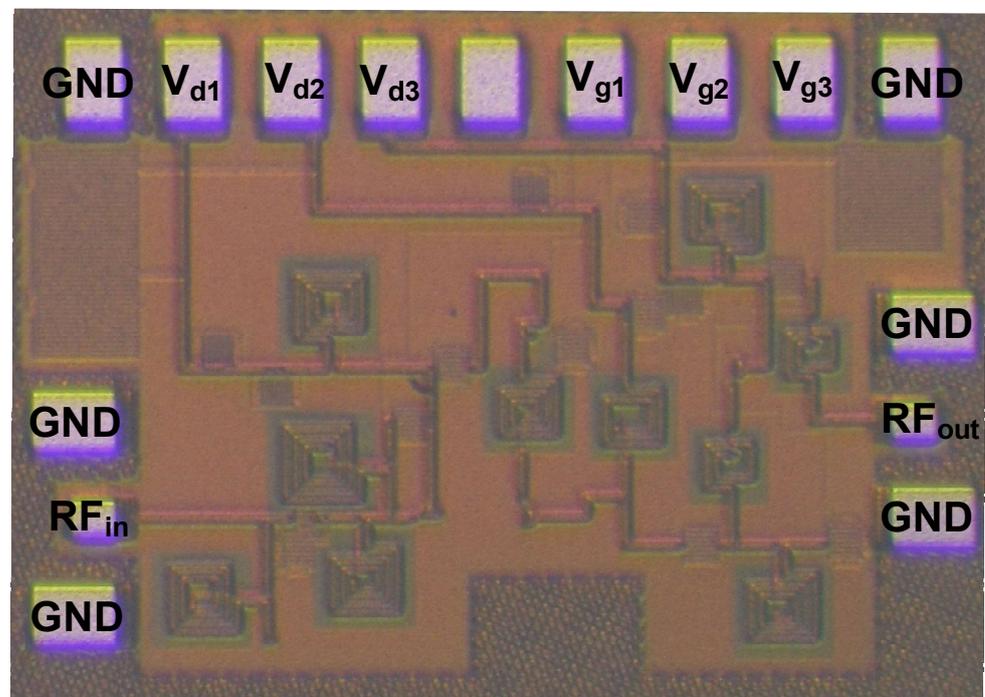


Figure 8. Chip micrograph of the full Ka-band amplifier.

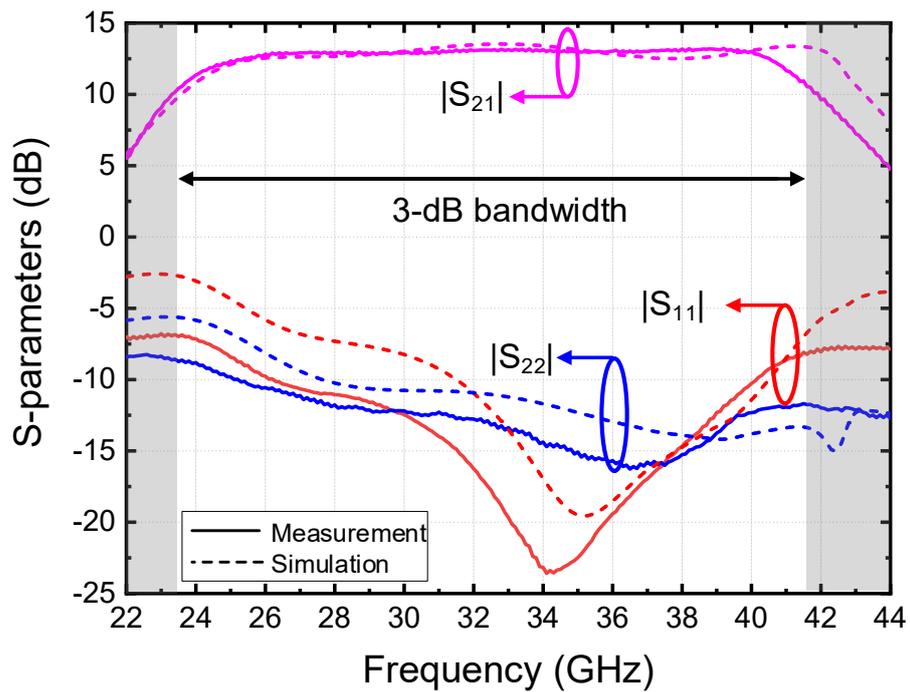


Figure 9. Measured S-parameters of the full Ka-band amplifier.

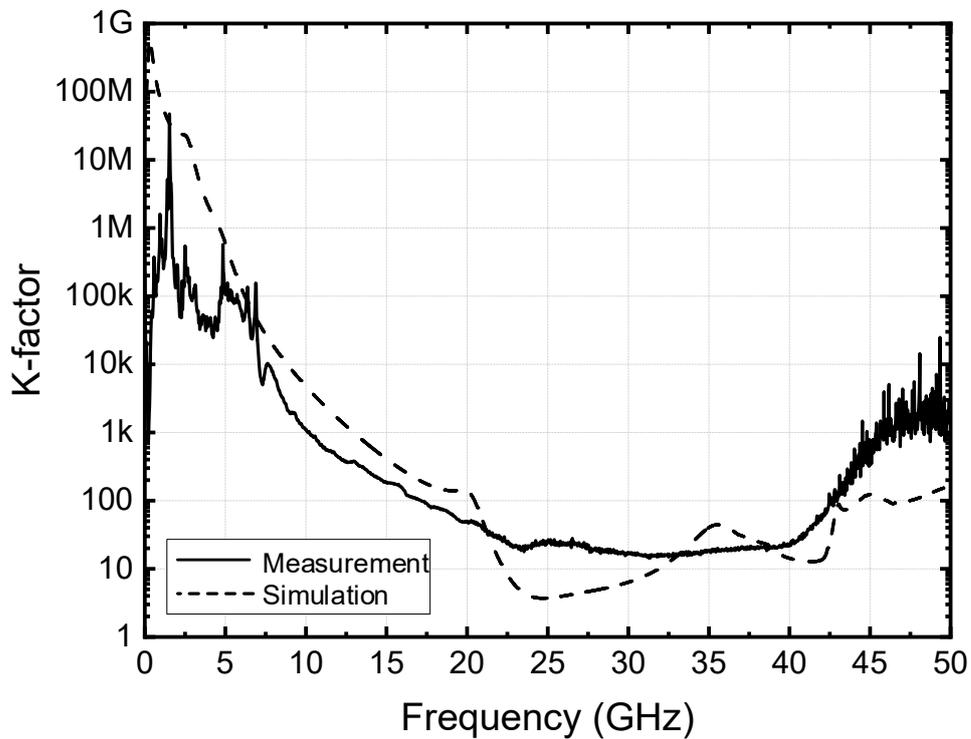


Figure 10. Stability factor based on the measured S-parameters.

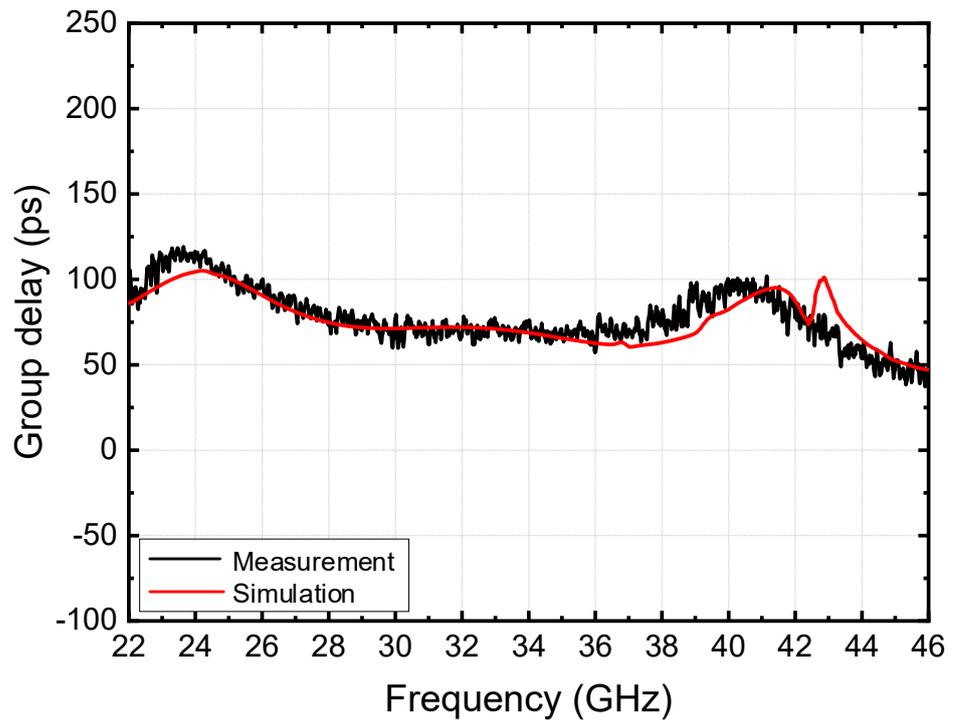


Figure 11. Measured group delay.

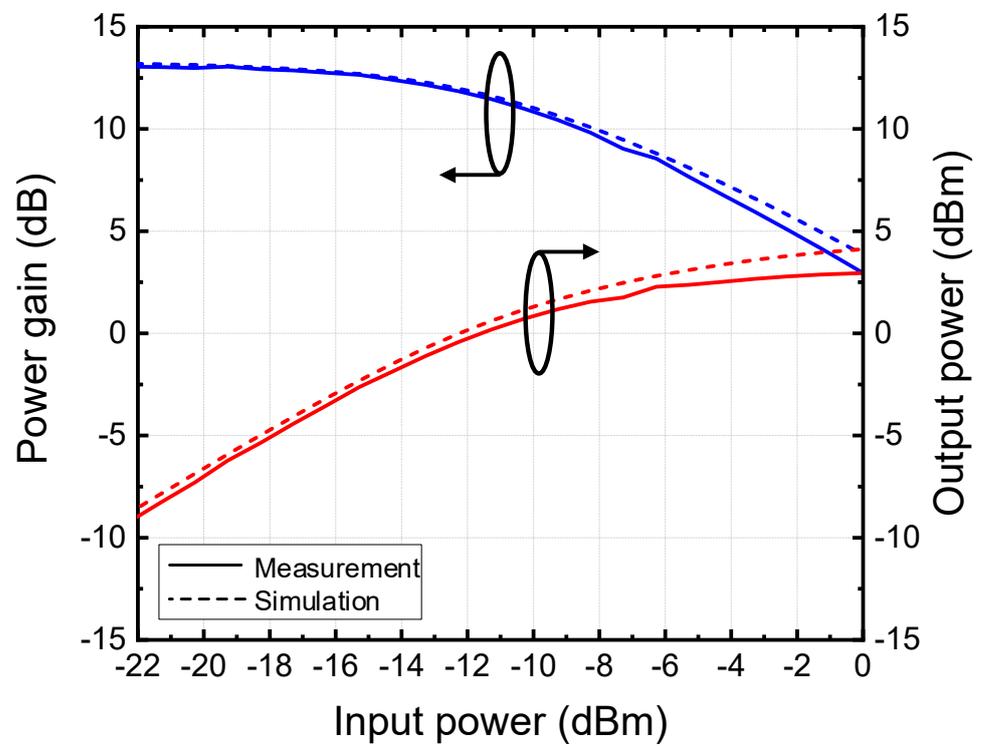


Figure 12. Measured output power and gain versus input power at 34 GHz.

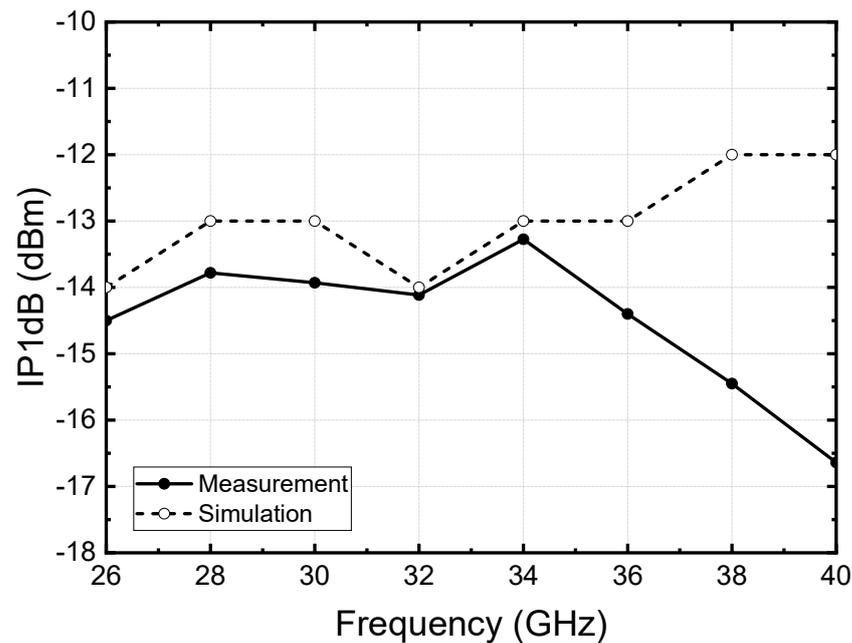


Figure 13. Measured IP1dB versus frequency.

4. Conclusions

In this research, a full Ka-band amplifier with a flat-gain response was fabricated using a 65 nm CMOS technology. To compensate for the gain roll-off in the upper end of the bandwidth, an inductive neutralization technique was used in the first stage. Neutralization inductance was carefully determined by considering gain and stability. To achieve a wideband flat gain, three CS stages designed at different center frequencies of 26, 34, and 42 GHz were cascaded. Using the frequency staggering technique, we found that the whole amplifier exhibited a flat-gain response of 13 ± 0.2 dB over the full Ka-band frequencies.

Author Contributions: Conceptualization, B.K. and S.J.; methodology, B.K. and S.J.; investigation, B.K. and S.J.; data curation, B.K. and S.J.; formal analysis, B.K. and S.J.; writing—original draft preparation, B.K.; writing—review and editing, S.J.; supervision, S.J.; project administration, S.J.; funding acquisition, S.J. All authors have read and agreed to the published version of the manuscript.

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