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A Study on Stability Control of Grid Connected DC Distribution System Based on Second Order Generalized Integrator-Frequency Locked Loop (SOGI-FLL)

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Abstract: This paper studies a second order generalized integrator-frequency locked loop (SOGI-FLL) control scheme applicable for 3-phase alternating current/direct current (AC/DC) pulse width modulation (PWM) converters used in DC distribution systems. The 3-phase AC/DC PWM converter is the most important power conversion system of DC distribution, since it can boost 380 V_{rms} 3-phase line-to-line AC voltage to 700 V_{dc} DC output with various DC load devices and grid voltages. The direct-quadrature (*d*-*q*) transformation, positive sequence voltage extraction, proportional integral (PI) voltage/current control, and phase locked loop (PLL) are necessary to control the 3-phase AC/DC PWM converter. Besides, a digital filter, such as low pass filter and all pass filter, are essential in the conventional synchronous reference frame-phase locked loop (SRF-PLL) method to eliminate the low order harmonics of input. However, they limit the bandwidth of the controller, which directly affects the output voltage and load of 3-phase AC/DC PWM converter when sever voltage fluctuation, such as sag, swell, etc. occurred in the grid. On the other hand, the proposed control method using SOGI-FLL is able to do phase angle detection, positive sequence voltage extraction, and harmonic filtering without additional digital filters, so that more stable and fast transient control is achieved in the DC distribution system. To verify the improvement of the characteristics in the unbalanced voltage and frequency fluctuation of the grid, a simulation and experiment are implemented with 50 kW 3-phase AC/DC PWM converter used in DC distribution.

Keywords: DC distribution; 3-phase AC/DC PWM converter; SOGI-FLL; phase detection

1. Introduction

In recent years, a distributed power generation system using a new, renewable energy source, and an eco-friendly electric vehicle has been attracted. The production and consumption of DC power have thus inevitably increased, and studies on the energy efficiency of DC power have been actively conducted.

In order to implement a DC distribution system with the conventional AC distribution infrastructure, a high efficiency power conversion system using a power semiconductor device is required. In general, diode rectifiers have been used to convert AC power to DC power because of their relatively simple structure and operation. However, the diode rectifier is not suitable for a DC distribution system because the constant output voltage cannot be controlled when the power factor

of AC input varies according to the type and size of the load. In addition, regenerative operation is not possible due to the unidirectional characteristic. Therefore, the 3-phase AC/DC pulse width modulation (PWM) converter is widely used to compensate for these drawbacks [1,2].

The 3-phase AC/DC PWM converter used for the DC distribution, as shown in Figure 1, is composed of six insulated gate bipolar transistors (IGBTs), dc-link capacitors, and an LCL filter to the reduce harmonics on the grid side. For bidirectional power control and power factor control of this system, phase angle information of the input power source is required. In many studies [3–5], a positive sequence voltage detector using an all pass filter (APF) and synchronous reference frame phase locked loop (SRF-PLL) have been widely used; however, not only do these devices have a complicated configuration, but they are also weak in lower order harmonics [6]. In addition, problems of the grid side, such as sag, swell, and frequency fluctuation directly affect the output of the 3-phase AC/DC PWM converter. As a result, it is difficult to maintain a stable condition in the DC distribution system in which various loads are repeatedly connected [7]. In order to solve the frequency variation of the grid for the DC distribution system, improved SRF-PLL method has been researched, but the unbalanced grid voltage and voltage drop condition are not taken into account [8].

Meanwhile, the second order generalized integrator (SOGI) algorithm was introduced by Prof. Rodriguez [9]. One of SOGI applications, SOGI-frequency locked loop (SOGI-FLL) has functions, such as the positive sequence voltage extraction and phase angle detection, as well as robust filtering characteristic. Therefore, phase synchronization can be performed using only the SOGI-FLL and it does not need any additional digital filters, such as the low pass filter (LPF) that is used in the conventional method [10,11].

Therefore, in this paper, we propose advanced control method using the SOGI-FLL that can be applied to a 3-phase AC/DC PWM converter for the DC distribution. The proposed control method is applied to improve the stability and transient characteristic of the DC distribution system, and it is verified that the DC distribution system achieves stable and fast transient characteristics, even though unbalanced grid voltage, frequency variation, and voltage drop occur.

This paper is organized as follows. In Section 2, we analyze the 3-phase AC/DC PWM converter, which constitutes the DC distribution system and describes the conventional method. In Section 3, we describe the phase detection and positive sequence voltage extraction while using the proposed SOGI-FLL technique. Sections 4 and 5 give the simulation and experimental results for the proposed control method based on the SOGI-FLL control, and Section 6 provides the conclusion.

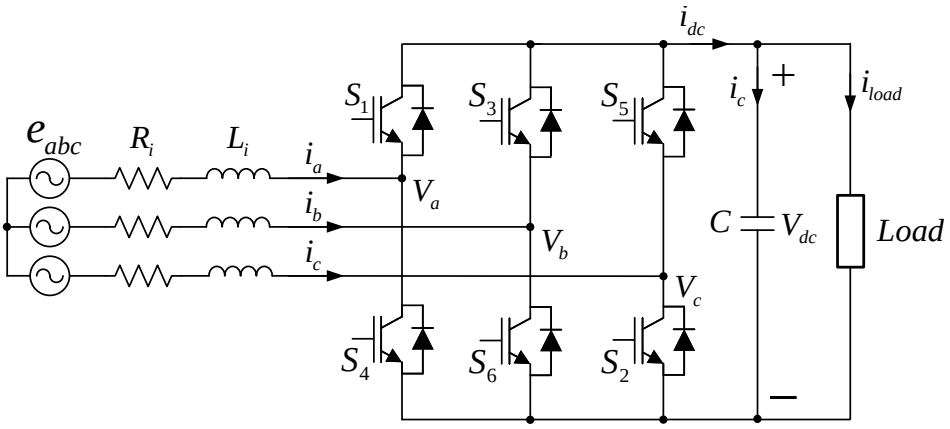


Figure 1. Configuration of 3-phase alternating current/direct current (AC/DC) pulse width modulation (PWM) converter.

2. 3-Phase AC/DC PWM Converter Used in DC Distribution System

2.1. 3-Phase AC/DC PWM Converter [12–14]

The 3-phase AC/DC PWM converter that is used for DC distribution is an AC/DC step-up converter that outputs a boost DC while using an appropriately designed AC input side reactor. Using this 3-phase AC/DC PWM converter, the grid side AC current can be maintained at a waveform that is close to a sinusoidal waveform with a relatively low total harmonic distortion (THD), and the power factor can be freely controlled. In addition, a bi-directional energy flow is possible by using a power semiconductor switch capable with bidirectional power flow, such as IGBT instead of a diode, so it can operate as both a DC/AC inverter and an AC/DC inverter.

Figure 2 shows the equivalent circuit of the 3-phase AC/DC PWM converter that is shown in Figure 1. The AC input voltage of each phase satisfies Equation (1), and the relationship between the input current i_{abc} and the voltage across the AC input reactor V_{Labc} is expressed, as shown in Equation (2).

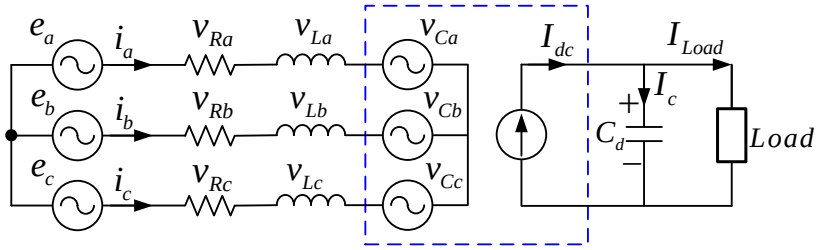


Figure 2. Equivalent circuit of 3-phase AC/DC PWM converter.

$$e_{abc} = v_{Rabc} + v_{Labc} + v_{Cabc} \tag{1}$$

$$v_{Labc} = j\omega L_{abc} i_{abc} \tag{2}$$

As can be seen from Equation (2), increasing the V_{Labc} increases the AC input side current, i_{abc}. Conversely, if the value of V_{Labc} becomes negative, the direction of i_{abc} is reversed and a regenerating operation is thus performed, the power of which flows from the DC load to the grid side. If the switching loss and harmonic loss of the 3-phase AC/DC PWM converter are ignored, the input power and the DC output power have the relationship that is shown in Equation (3).

$$V_C \cdot C \frac{dV_C}{dt} = v_{Ca} i_a + v_{Cb} i_b + v_{Cc} i_c = e_a i_a + e_b i_b + e_c i_c \tag{3}$$

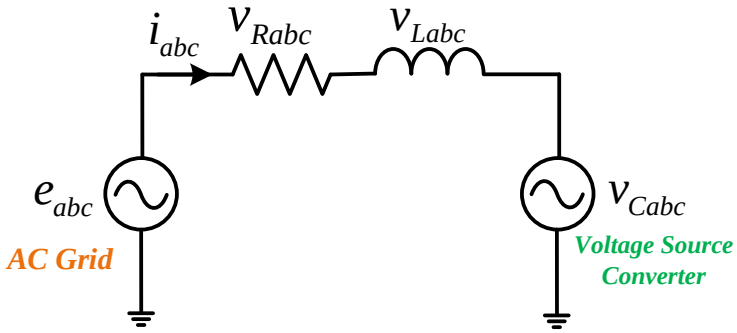


Figure 3. Equivalent circuit of a 3-phase AC/DC PWM converter.

Figure 3 shows a single-phase equivalent circuit of a 3-phase AC/DC PWM converter for analyzing the grid voltage and the current in a phasor diagram. When the converter performs a

regenerative operation, the power factor angle of the AC power source in the steady state can be varied from leading to lagging, as shown in the phasor diagram of Figure 4 by controlling the AC side of the 3-phase AC/DC PWM converter. Figure 4 shows that the AC voltage is the smallest when the lagging operation is conducted. If the DC voltage is smaller than the maximum value of the AC input voltage, the constant DC output voltage can be controlled by lagging operation.

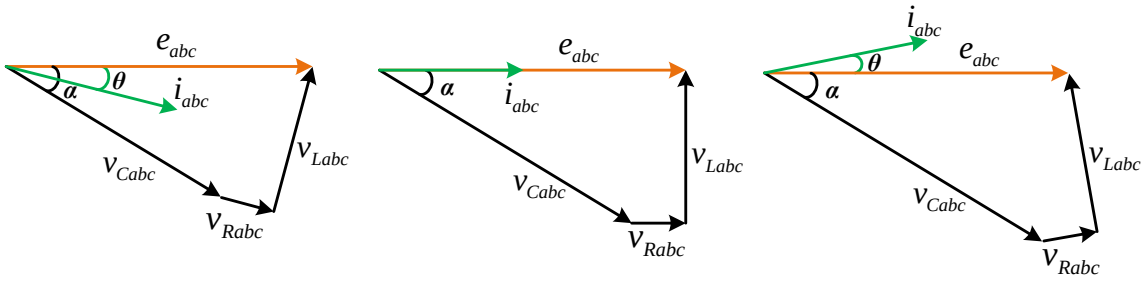


Figure 4. Phasor diagram of a 3-phase AC/DC PWM converter.

2.2. Positive Sequence Voltage and Phase Detector [15,16]

The phase angle information of the grid is needed in a grid-connected DC distribution system. In the case of power factor control, active/reactive power control, and harmonic current compensation, the current or voltage reference must be synchronized with the phase angle of the input voltage. A PLL is used for this phase synchronization. If the 3-phase power source is balanced, then the phase angle can be obtained by calculating the period between the zero-crossing points where the voltage of one phase or any line-to-line voltage changes from negative to positive. However, in the case of unbalanced 3-phase source, a miscalculated phase angle can result in harmonic components of voltage and current, which can lead to unforeseen problems. To avoid this problem that is caused by the unbalanced 3-phase source, the phase angle is detected by calculating the positive sequence voltage.

The equation for calculating the positive sequence voltage is given by the following Equation (4):

$$\begin{bmatrix} v_{pa} \\ v_{pb} \\ v_{pc} \end{bmatrix} = \frac{1}{3} \cdot \begin{bmatrix} 1 & \alpha & \alpha^2 \\ \alpha^2 & 1 & \alpha \\ \alpha & \alpha^2 & 1 \end{bmatrix} \cdot \begin{bmatrix} v_{as} \\ v_{bs} \\ v_{cs} \end{bmatrix} \tag{4}$$

where $\alpha = e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$ and $\alpha^2 = e^{j\frac{4\pi}{3}} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$.

α and α^2 can be substituted into Equation (4), and Equation (5) is then defined, as follows:

$$\begin{bmatrix} v_{pa} \\ v_{pb} \\ v_{pc} \end{bmatrix} = \begin{bmatrix} \frac{1}{2}v_{as} - \frac{1}{2\sqrt{3}j}(v_{bs} - v_{cs}) \\ -(v_{pa} + v_{pc}) \\ \frac{1}{2}v_{cs} - \frac{1}{2\sqrt{3}j}(v_{as} - v_{bs}) \end{bmatrix} \tag{5}$$

Figure 5 shows the control block diagram of the positive sequence voltage and PLL while using Equations (4) and (5). As shown in the figure, the *d*-*q* transformation is performed after extracting the positive sequence voltage while using the 3-phase voltage of the input power source. In the *d*-*q* transformation, the information on the *q* axis refers to the magnitude of the voltage output of the converter, and the information on the *d* axis is related to the phase error between the converter output voltage and the grid voltage. Therefore, the phase output voltage of the converter must control the *d*-axis voltage to zero for phase synchronization with the grid voltage. The *d*-axis voltage in the synchronous reference frame, as calculated by the PI controller, then performs a PLL that controls the phase angle to be zero so that the phase angle matches the actual phase angle of the grid side. When the input power source includes harmonics due to noise, the harmonics also appear in the *d*-axis

voltage used as an input of the PLL. Therefore, as shown in Figure 6, the first order low pass filter is used to prevent pulsation.

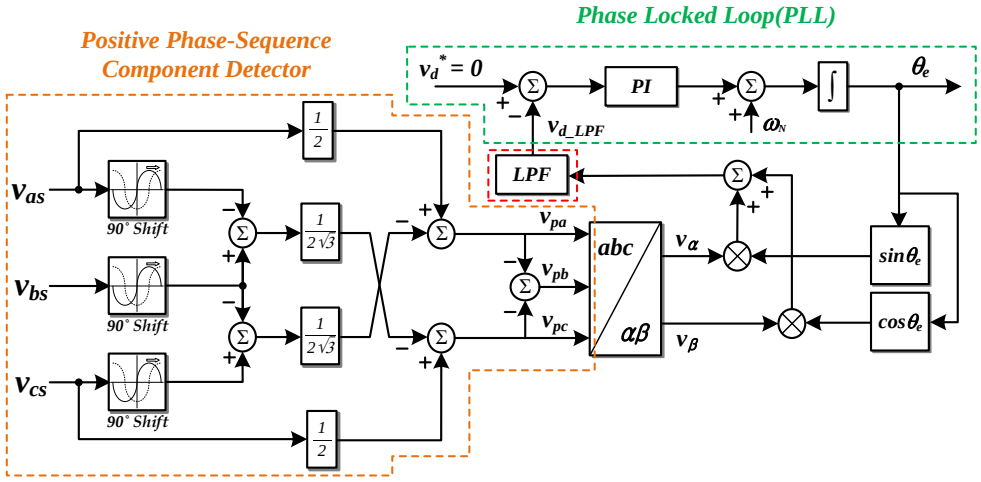


Figure 5. Control block diagram of positive sequence voltage and phase detector.

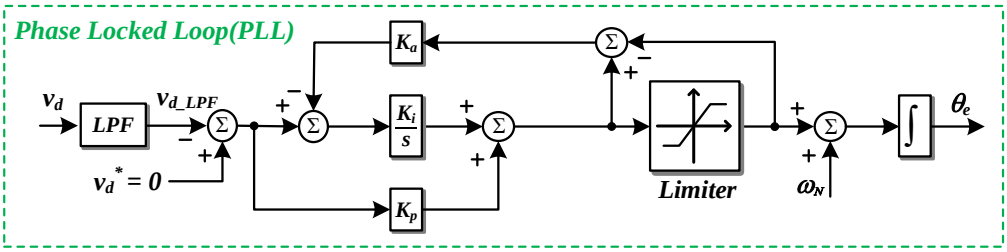


Figure 6. Control block diagram of phase detector using first order low pass filter and proportional integral (PI) controller.

3. Proposed Control Scheme of 3-Phase AC/DC PWM Converter Using SOGI-FLL

In the conventional PLL method that is discussed in Section 2.2, the sensed 3-phase input voltage is divided into magnitude and phase angle information by d-q transformation and the d-axis voltage in the synchronous reference frame is used to obtain phase angle information. However, the conventional PLL method is difficult to use in single-phase systems. In addition, if the cut-off frequency of the low pass filter is decreased to reduce the low frequency harmonics of the input power source, the total control bandwidth of the PLL will be reduced, which is disadvantageous to the sudden change of phase angle [17].

Therefore, this section describes the FLL method using SOGI, which is applicable to both single-phase and 3-phase systems and has excellent performance for low frequency harmonics reduction [18–20]. This section also introduces a method of detecting positive sequence voltage while using SOGI-FLL and it describes the design of the controller.

3.1. Second Order Generalized Integrator

Figure 7 shows the structure of the SOGI-based adaptive filter (AF) in a control block diagram [21]. The transfer function of the SOGI that is shown in Figure 7 can be expressed as Equation (6), and the transfer function for the output signals v' and qv' of the SOGI-based AF is defined as Equation (7). As can be seen from the transfer function $D(s)$ in Equation (7), the bandwidth of the SOGI-based AF is independent of the frequency ω' and it is only determined by the gain k. Also, the output signal qv' generates a signal that is delayed by 90 degrees from the phase of the output v', irrespective of the

frequency of the center frequency ω' and the input signal v. Therefore, Equation (7) can be expressed as the bode plot as shown in Figure 8.

$$SG(s) = \frac{v'}{k\varepsilon_v}(s) = \frac{\omega' s}{s^2 + \omega'^2} \tag{6}$$

$$D(s) = \frac{v'}{v}(s) = \frac{k\omega' s}{s^2 + k\omega' s + \omega'^2}, \quad Q(s) = \frac{qv'}{v}(s) = \frac{k\omega'^2}{s^2 + k\omega' s + \omega'^2} \tag{7}$$

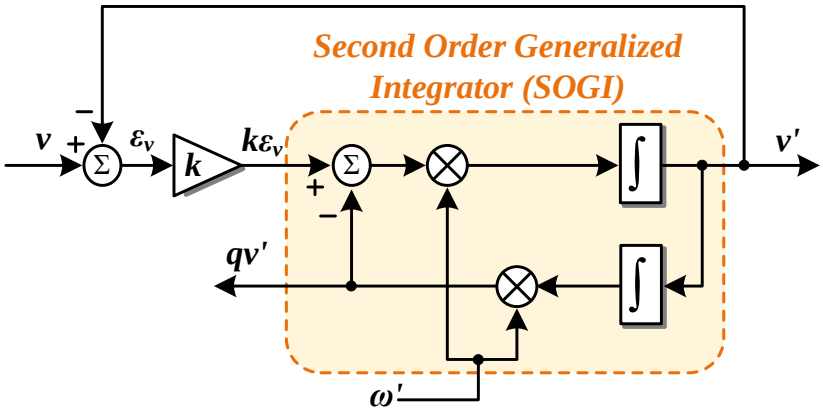


Figure 7. Control block diagram of second order generalized integrator (SOGI)-based adaptive filter (AF) (= SOGI-quadrature signal generator (QSG)).

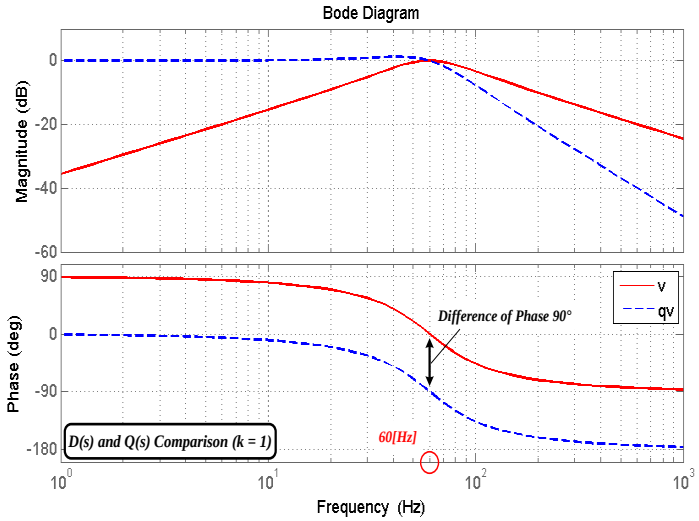
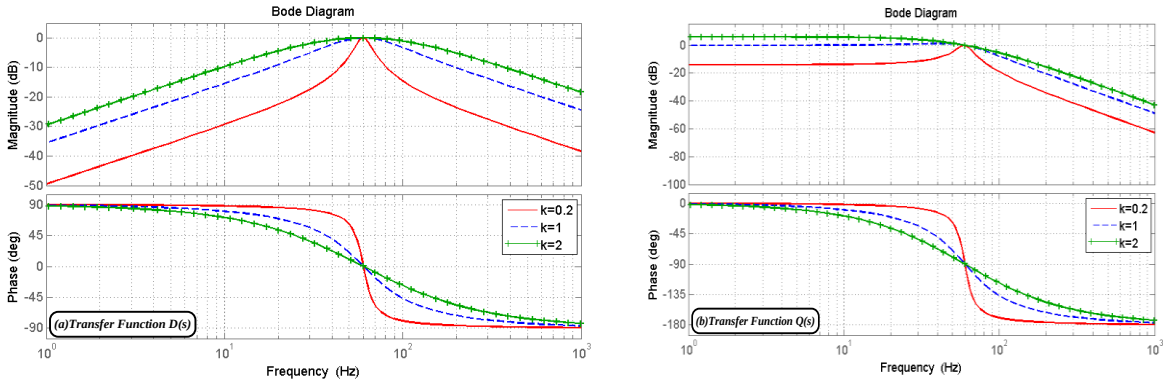


Figure 8. Comparison of transfer function $D(s)$ and $Q(s)$.

Figure 9 shows the bode plot of the transfer function of Equation (7). From the figure, it can be seen that as the gain k decreases, the filtering effect improves, but the stability according to the frequency change decreases. The SOGI-based AF, as shown in Figure 7, is also called the SOGI-quadrature signal generator (SOGI-QSG).



(**a**) Bode plot of transfer function $D(s)$ (**b**) Bode plot of transfer function $Q(s)$

Figure 9. Characteristics of SOGI-based AF various gain k.

3.2. SOGI-FLL

SOGI-FLL is used for detecting input voltage exactly, even if input frequency is varied and due to grid distortion or fault. Configuration and discretization of the SOGI-FLL technique in single-phase grid-connected inverter system is introduced in [22]. In this subsection, not only introducing the structure of SOGI-FLL, but also how SOGI-FLL extracts information of input voltage and tracks frequency variation based on its mathematical explanation and bode plot. If the center frequency ω' is set to the same frequency as the input signal, the SOGI-based AF outputs v' having the same amplitude and phase as the input signal and qv' delayed only by 90 degrees from the input signal. However, if the frequency of the input signal varies, the amplitudes of v' and qv' is changed. Therefore, it is not appropriate to use SOGI only for power conversion systems that use AC power such as grid-connected systems. In order to apply SOGI to a system where the input frequency is possibly changed, the center frequency must be able to follow the frequency change of the input signal.

In the FLL method, frequency information is extracted using the phase delayed signal of SOGI qv', which is used as the center frequency ω' of SOGI. FLL can be operated without the PI controller and trigonometric function calculations that were used in PLL. Figure 10 shows the control block diagram of SOGI-FLL, where ω_N is the angular frequency of the input voltage in steady state, as used in the PLL.

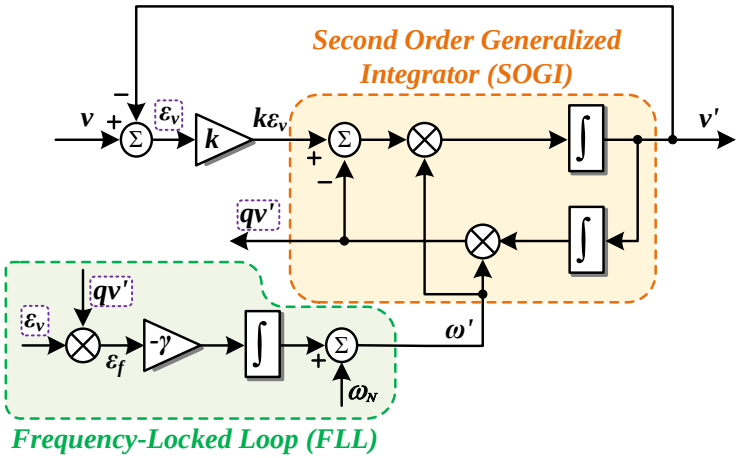


Figure 10. Control block diagram of SOGI-frequency locked loop (FLL) for phase synchronization.

In order to explain the SOGI-based AF with FLL, the error signal ε_v, which is the relation between the output signals qv', v', and v, should be analyzed. The transfer function for the input signal v and the error signal ε_v is shown in Equation (8).

$$E(s) = \frac{\varepsilon_v}{v}(s) = \frac{s^2 + \omega\prime^2}{s^2 + k\omega' s + \omega\prime^2} \tag{8}$$

The transfer function $E(s)$ is illustrated in the bode plot that is shown in Figure 11.

As shown in Figure 11, if the frequency of the input signal ω is lower than the center frequency ω', qv', and ε_v have the same phase. That is, the frequency error variable ε_f can be calculated using the two signals qv' and ε_v. If $\omega < \omega'$, then ε_f is a positive value, if $\omega = \omega'$ then $\varepsilon_f = 0$ and if $\omega > \omega'$ then ε_f is a negative value. This means that the negative gain $-\gamma$ and the integrator expressed in Figure 10 are used to set the DC component of the frequency error variable ε_f to zero so that the center frequency ω' tracks the frequency of the input signal ω.

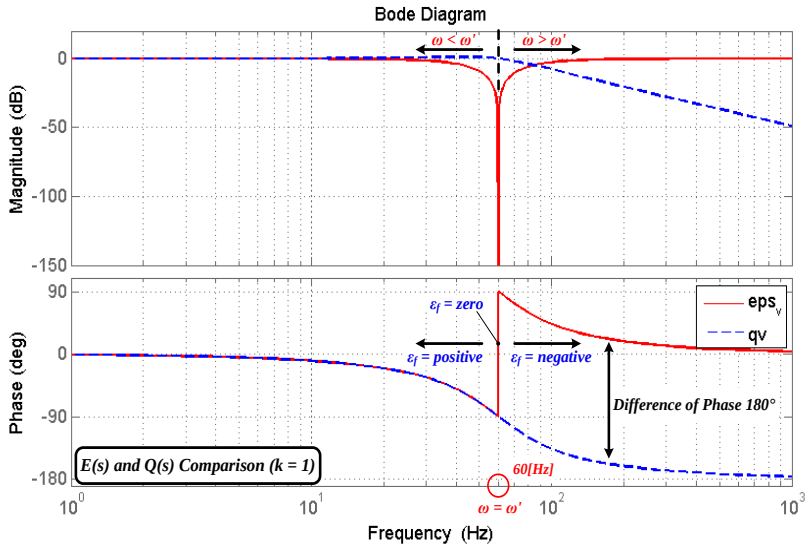


Figure 11. Comparison of transfer functions $E(s)$ and $Q(s)$.

To use this SOGI-FLL in 3-phase systems, two SOGIs are used. This is called a double second order generalized integrator (DSOGI). Figure 12 shows a control block diagram of the DSOGI-FLL that is used in the 3-phase AC system.

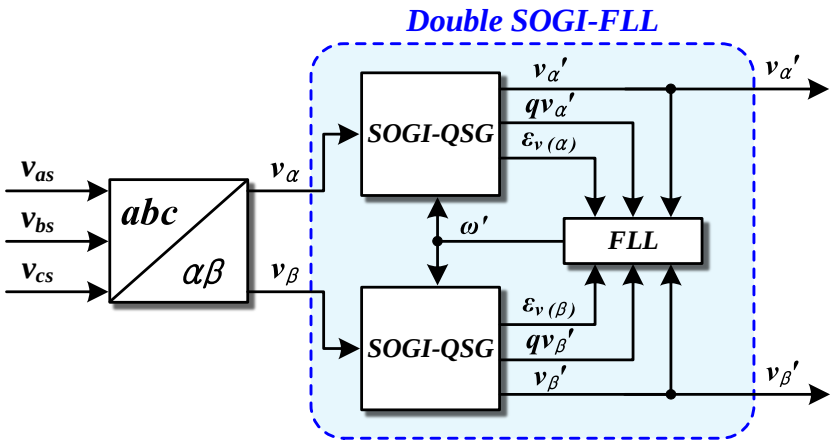


Figure 12. 3-phase SOGI-FLL (= DSOGI-FLL).

3.3. Positive Sequence Voltage Extraction and Phase Detection Using 3-Phase SOGI-FLL

In 1937, Lyon proposed a method for decomposing balanced 3-phase voltages v_a, v_b, and v_c into positive, negative, and zero sequence voltage in the time domain, respectively, while in 1918, Fortescue proposed a method in the frequency domain [23]. Using these methods, the balanced 3-phase voltage is decomposed into positive, negative, and zero sequence voltages, as shown in Equations (9)–(11), respectively.

$$\begin{bmatrix} v_a^+ \\ v_b^+ \\ v_c^+ \end{bmatrix} = \frac{1}{3}\cdot\begin{bmatrix} 1 & \alpha & \alpha^2 \\ \alpha^2 & 1 & \alpha \\ \alpha & \alpha^2 & 1 \end{bmatrix}\cdot\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \left(v_{abc}^+ = [T_+]\cdot v_{abc}\right) \tag{9}$$

$$\begin{bmatrix} v_a^- \\ v_b^- \\ v_c^- \end{bmatrix} = \frac{1}{3}\cdot\begin{bmatrix} 1 & \alpha^2 & \alpha \\ \alpha & 1 & \alpha^2 \\ \alpha^2 & \alpha & 1 \end{bmatrix}\cdot\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \left(v_{abc}^- = [T_-]\cdot v_{abc}\right) \tag{10}$$

$$\begin{bmatrix} v_a^0 \\ v_b^0 \\ v_c^0 \end{bmatrix} = \frac{1}{3}\cdot\begin{bmatrix} 1 & 1 & 1 \\ 1 & 1 & 1 \\ 1 & 1 & 1 \end{bmatrix}\cdot\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \left(v_{abc}^0 = [T_0]\cdot v_{abc}\right) \tag{11}$$

where $\alpha = e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$ and $\alpha^2 = e^{j\frac{4\pi}{3}} = -\frac{1}{2} - j\frac{\sqrt{3}}{2}$.

3×3 matrices in each equation can be expressed as $[T_+]$, $[T_-]$, and $[T_0]$. If the balanced 3-phase voltage is transformed to the voltage in the stationary reference frame, it can be defined as Equation (12). Equation (12) is then simplified to Equation (13), with the assumption that no zero sequence components exist in the balanced 3-phase voltage.

$$\begin{bmatrix} v_\alpha \\ v_\beta \\ v_0 \end{bmatrix} = \frac{2}{3}\cdot\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\cdot\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad v_{\alpha\beta 0} = \left[T_{\alpha\beta 0}\right]\cdot v_{abc} \tag{12}$$

$$\begin{bmatrix} v_\alpha \\ v_\beta \end{bmatrix} = \frac{2}{3}\cdot\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\cdot\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} \quad v_{\alpha\beta} = \left[T_{\alpha\beta}\right]\cdot v_{abc} \tag{13}$$

The transpose matrix $\left[T_{\alpha\beta}\right]$ is given by the following Equation (14).

$$\left[T_{\alpha\beta}\right]^T = \frac{3}{2}\cdot\begin{bmatrix} \frac{2}{3} & 0 \\ -\frac{1}{3} & \frac{\sqrt{3}}{3} \\ -\frac{1}{3} & -\frac{\sqrt{3}}{3} \end{bmatrix} \tag{14}$$

Using Equations (9)–(14), the positive and negative sequence voltages in the stationary reference frame can be summarized, as shown in Equations (15) and (16).

$$\begin{aligned} v_{\alpha\beta}^+ &= \left[T_{\alpha\beta}\right]\cdot v_{abc}^+ = \left[T_{\alpha\beta}\right]\cdot[T_+]\cdot v_{abc} \\ &= \left[T_{\alpha\beta}\right]\cdot[T_+]\cdot\left[T_{\alpha\beta}\right]^T\cdot v_{\alpha\beta} = \frac{1}{2}\cdot\begin{bmatrix} 1 & -q \\ q & 1 \end{bmatrix}\cdot v_{\alpha\beta} \end{aligned} \tag{15}$$

$$\begin{aligned} v_{\alpha\beta}^- &= \left[T_{\alpha\beta}\right]\cdot v_{abc}^- = \left[T_{\alpha\beta}\right]\cdot[T_-]\cdot v_{abc} \\ &= \left[T_{\alpha\beta}\right]\cdot[T_-]\cdot\left[T_{\alpha\beta}\right]^T\cdot v_{\alpha\beta} = \frac{1}{2}\cdot\begin{bmatrix} 1 & q \\ -q & 1 \end{bmatrix}\cdot v_{\alpha\beta} \end{aligned} \tag{16}$$

In Equations (15) and (16), $q = e^{-j\frac{\pi}{2}}$, which indicates that the phase is delayed by 90 degrees. In this case, the positive and negative sequence voltage extractors are added. Figure 12 is then modified, as shown in Figure 13.

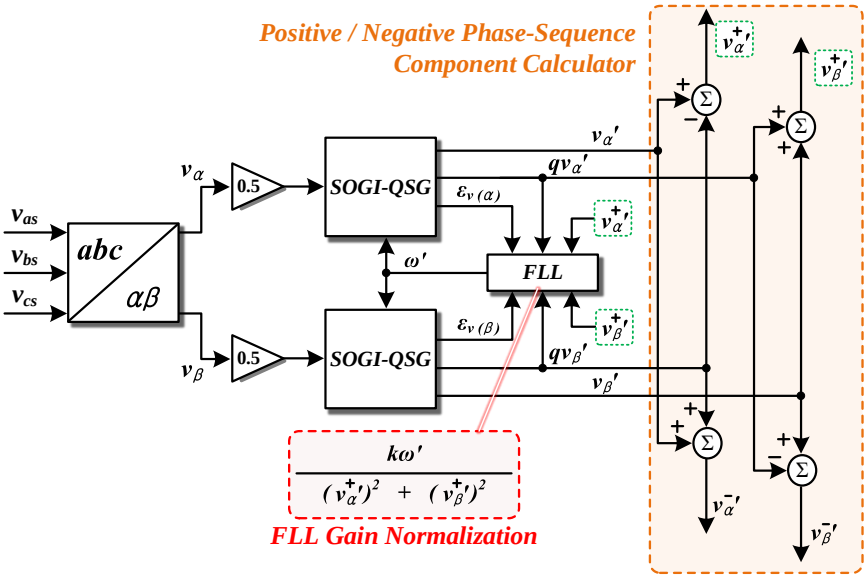


Figure 13. Positive sequence voltage extractor using 3-phase SOGI-FLL.

3.4. Control Block Diagram of Overall System with SOGI-FLL

Figure 14 shows the overall control block diagram of the proposed control scheme. Similar to the conventional control method, each line-to-line voltage of the grid is sensed and transformed to a stationary reference frame. The phase angle information is then extracted while using DSOGI-FLL. The coordinate of the input current of the 3-phase AC/DC PWM converter is transformed using the extracted phase angle derived from DSOGI-FLL. At this time, the output of the PI voltage controller that controls the dc-link voltage is applied to the input of the PI current controller that controls the active and reactive power of the grid. When the output of the current controller performs an inverse *d-q* transformation, an extracted phase angle using DSOGI-FLL is also used.

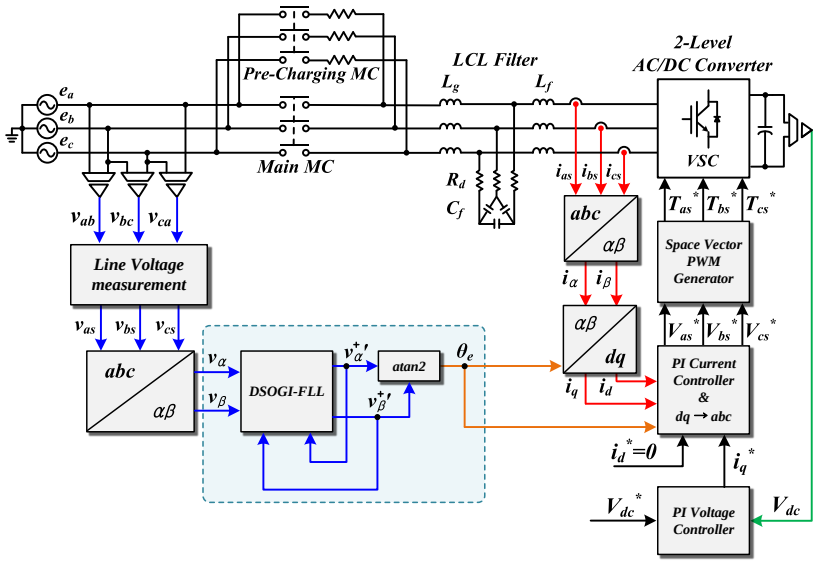


Figure 14. Control block diagram of 3-phase AC/DC PWM converter with SOGI-FLL.

As can be seen from the control block diagram, when using the proposed control scheme, the coordinate transformation is simpler than the control method while using the conventional PLL. In addition, the low pass filter that affects the bandwidth of the controller disappears in the proposed control method.

4. Simulation Results

In this paper, the simulation was performed before verifying the operation of the 3-phase AC/DC PWM converter with the SOGI-FLL method for the DC distributed system. Table 1 shows the parameters that are used in the simulation, while the configuration of the simulation circuit is shown in Figure 15. In the existing AC power grid, the power from the power plant is supplied to the consumer in single phase 220 V_{rms} and 3-phase 380 V_{rms}. Therefore, the 3-phase voltage is selected, as shown in the parameter. Also, when configuring of the DC distribution system, the DC-link voltage was selected as 700 V_{dc}, which is capable of meeting the scope of international electrotechnical commission (IEC) regulations [24]. The switching frequency is selected in consideration of the FS300R12KE3, which IGBT are used in this system, and the LCL filter are designed to satisfy the current distortion regulation of the IEEE ST 519-2014.

Table 1. Simulation parameter of DC distributed system.

Parameter	Value	Unit
Rated power of system	50	[kW]
3 phase line-to-line grid voltage	380	[V_{rms}]
Grid frequency	60	[Hz]
Switching frequency	5	[kHz]
Output DC-link voltage	700	[V_{dc}]
DC-link capacitance	10200	[μF]
LCL filter inductance at grid side	120	[μH]
LCL filter capacitance	50	[μF]
LCL filter inductance at converter side	500	[μH]

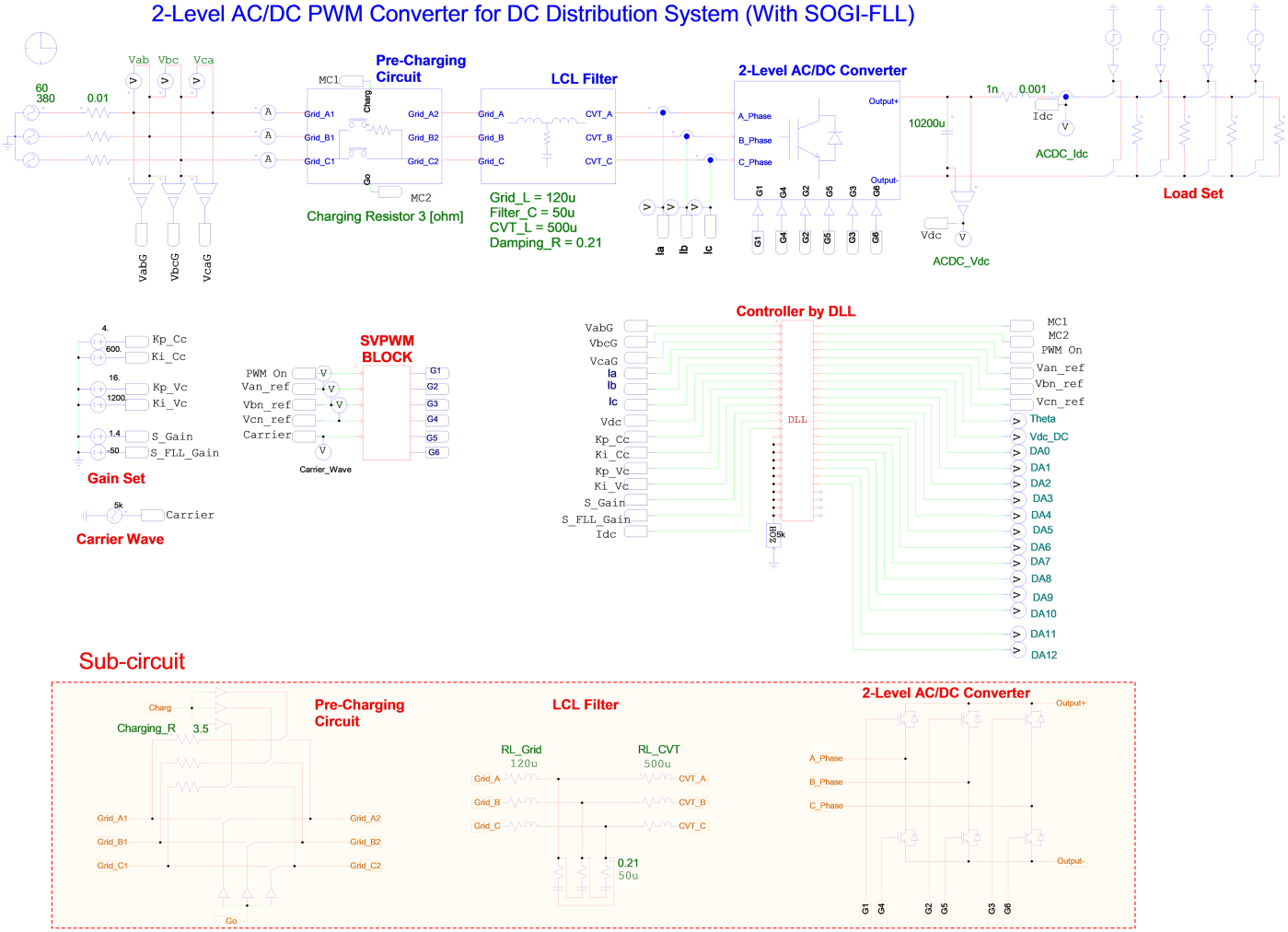


Figure 15. 3-phase AD/DC PWM converter schematic of DC distribution system used in simulation.

Figure 16a shows the output voltage waveform of a DC distribution system while using a 3-phase AC/DC PWM converter. The system uses an initial charge circuit that charges a certain amount of voltage to the output capacitor for 0.2 s to reduce the inrush current entering the output capacitor. Then, the charge of the capacitor voltage increases, while the initial charge circuit is changed from the initial charge to a standby condition. Finally, an output voltage control of 700 V_{dc} is initiated from 0.3 s. In order to prevent the high overshoot of the output voltage at the start of the control, the voltage reference is given in the form of a ramp. The voltage reference then rapidly enters the steady state due to the fast dynamic characteristics of the PI controller.

Figure 16b shows the output current waveform after connecting the DC link output to the load. The load is connected to the system from 0.8 s and the load capacity is increased by 10 kW every 0.15 s. Finally, a current is stably generated at the system rated capacity of 50 kW.

Figure 16c shows the 3-phase input current waveform from the grid to the system. It is confirmed that the reactive component rarely flows when no load is applied, and the magnitude of the input current increases step by step when the load is connected.

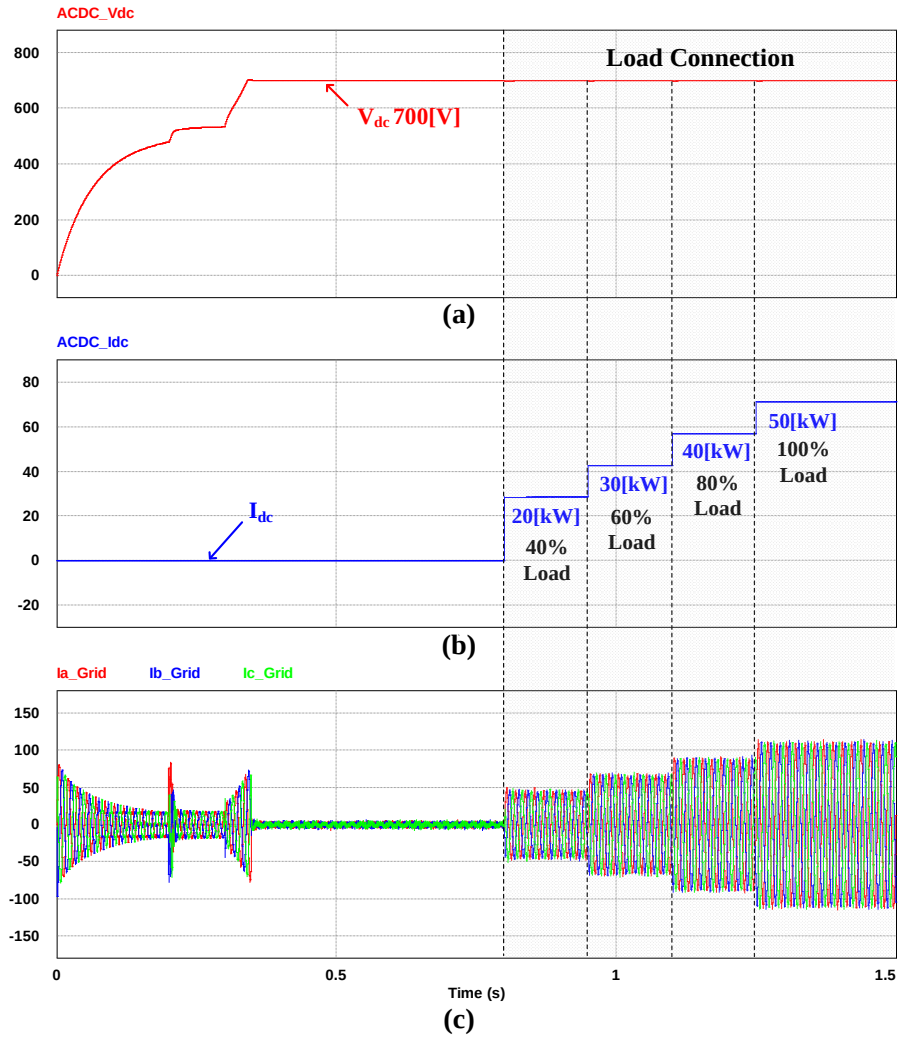


Figure 16. Input and output waveforms of DC distribution system (**a**) the dc-link voltage; (**b**) the current of the DC load; and, (**c**) the current of the grid.

Figure 17a shows the 3-phase input voltage waveforms containing the 3rd, 5th, 7th, 9th, and 11th harmonics. The input voltage is detected through the sensor and is then input to the controller. The SOGI-FLL is applied to the system controller in the middle of the $\alpha\beta - dq$ coordinate transformation,

and the output voltage of the SOGI-FLL indicates that the harmonics are reduced, as shown in Figure 17b. The THD of the detected positive sequence voltage is about 3.9%, which is appropriate for the phase angle detection.

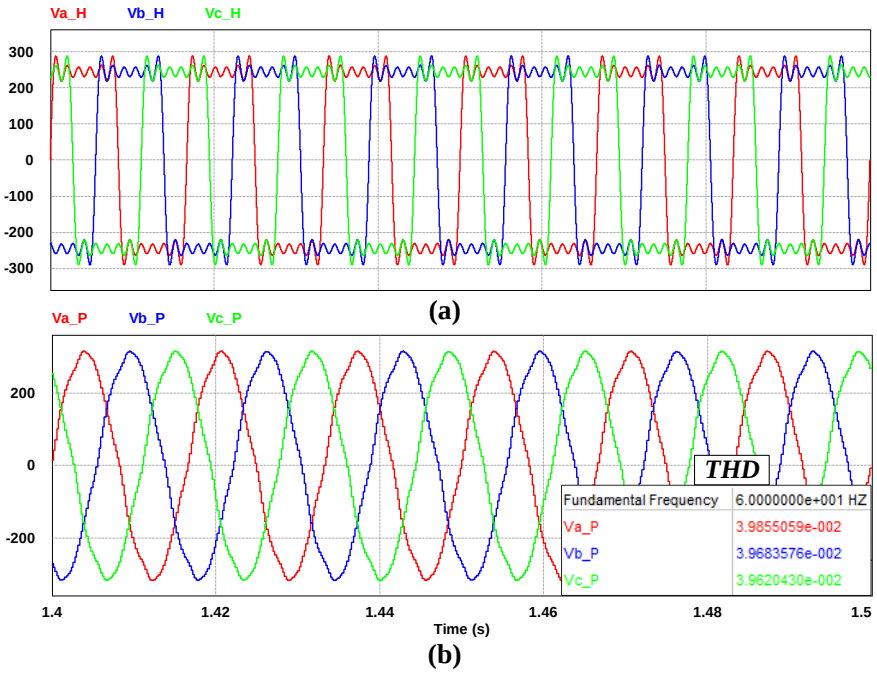


Figure 17. Waveform of voltage when harmonics is included in input side; (**a**) the 3-phase input voltage with harmonic components; and, (**b**) the 3-phase input voltage detected by the SOGI-FLL.

Figure 18 shows the waveforms when a voltage drop of about 30% occurs on the *b* phase. Figure 18a shows the dc-link output voltage waveform. A voltage ripple of about 2 [$V_{peak\text{-}to\text{-}peak}$] is generated while voltage drop occurs. Figure 18b shows the unbalanced 3-phase input voltage waveform. The balanced 3-phase condition is distorted by the voltage drop from 1 to 1.2 s. Figure 18c shows the detected positive sequence voltage waveform using SOGI-FLL. Unlike that shown in Figure 18b, the magnitude of voltage is slightly reduced and it maintains a balanced 3-phase condition. The 3-phase input current waveform is illustrated in Figure 18d. Unlike the voltage in Figure 18b, the changes in the amplitudes of the phases differ, and the shape of the waveform is severely distorted. Figure 18e shows the center frequency ω' extracted from SOGI-FLL. Only a slight ripple is generated, and it does not significantly differ from the frequency value in the steady state.

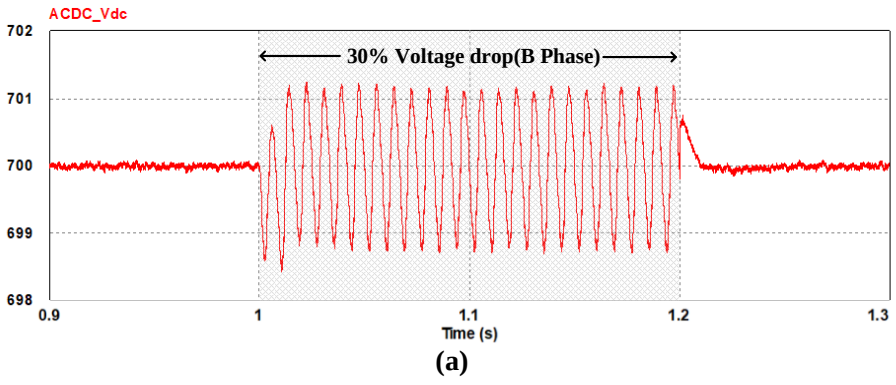
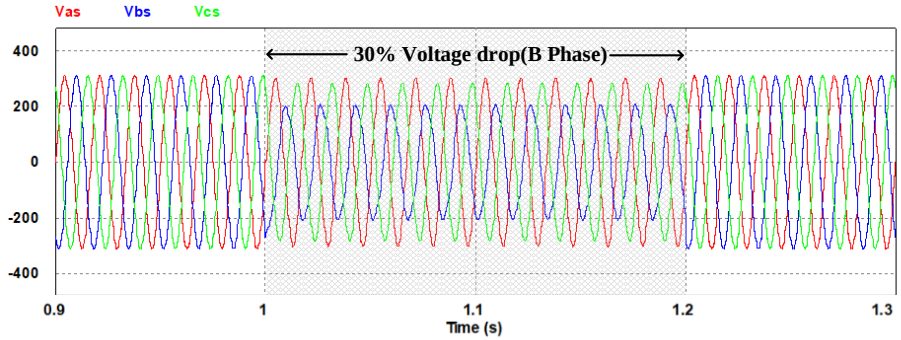
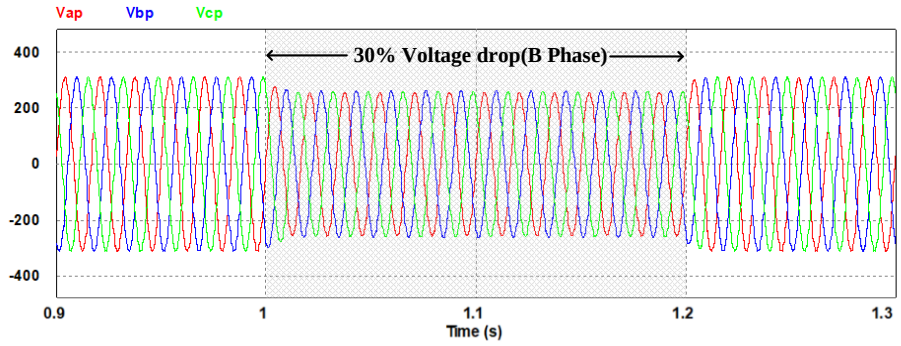


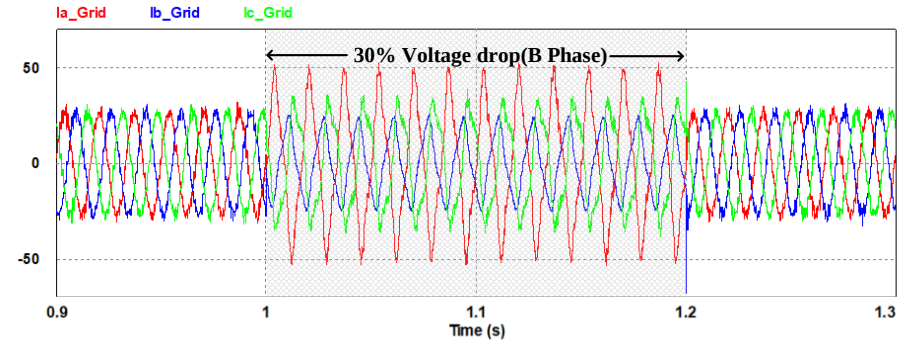
Figure 18. *Cont.*



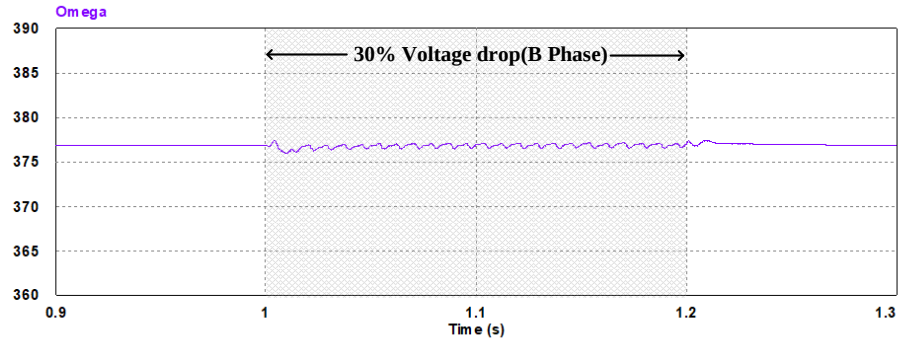
(b)



(c)



(d)



(e)

Figure 18. Waveforms of simulation results when *b* phase has a voltage drop; (**a**) the dc-link voltage; (**b**) the 3-phase input voltage with voltage unbalance; (**c**) the 3-phase input positive voltage detected by SOGI-FLL; (**d**) the 3-phase input current; and, (**e**) the center frequency extracted from SOGI-FLL.

Figure 19 shows the positive and negative sequence voltages and the phase angle generated by SOGI-FLL. While only negligible negative sequence voltage occurs before the unbalance condition, the negative sequence voltage increases immediately after the unbalance condition. In addition, while the phase angle of the positive sequence voltage is stably tracked, the phase angle of the negative sequence component is rapidly changed.

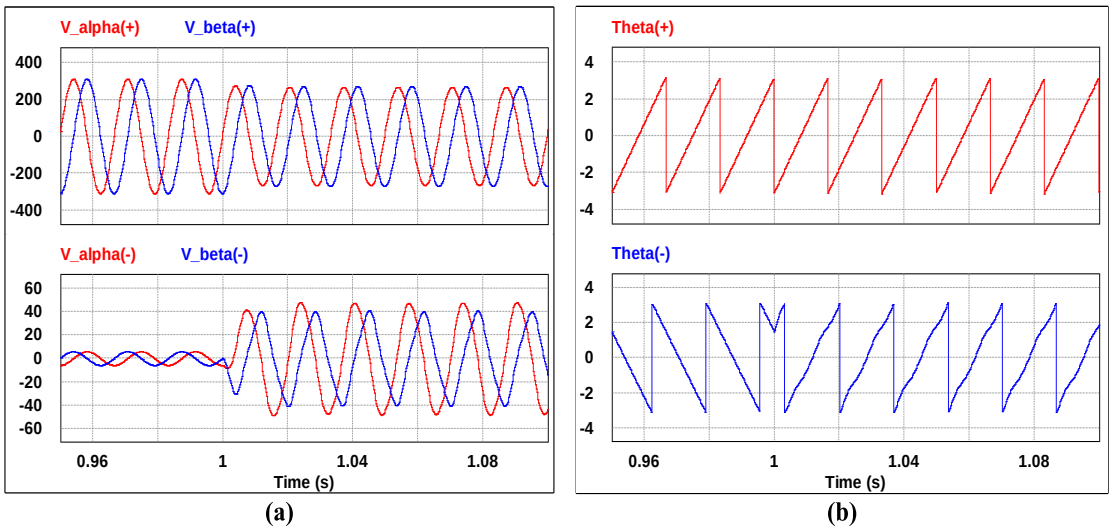


Figure 19. Waveforms of simulation results when voltage drop is occurred; (**a**) the positive and negative sequence voltage; and, (**b**) the phase angle of the positive and negative sequence voltage.

Figure 20 shows the waveforms when the grid frequency decreased from 60 Hz to 45 Hz. Grid frequency is reduced to 45 Hz from 1 to 1.2 s, while the power is supplied to the 12 kW load, and the grid frequency is then recovered to 60 Hz. Figure 20a shows that the dc-link output voltage waveform maintains an almost constant voltage, even when the frequency decreases. Figure 20b shows the 3-phase input voltage waveform. When the frequency is decreased from 1 to 1.2 s, the period increases. Figure 20c shows the positive sequence voltage waveform that was detected by SOGI-FLL. As shown in Figure 20b, since only negligible distortion occurs in the voltage, only the period changes without large amplitude change. Figure 20d shows the 3-phase input current waveform. It can be seen that, while the input current also only changes the period, it but does not cause large distortion. Figure 20e shows the center frequency ω', as extracted from SOGI-FLL. As soon as the grid frequency changes, the FLL follows the grid frequency and synchronizes the output center frequency to the grid frequency. The FLL gain value is designed considering the frequency tracking time of 0.1 s, but the steady state takes slightly more time than the designed time due to the change of the grid conditions.

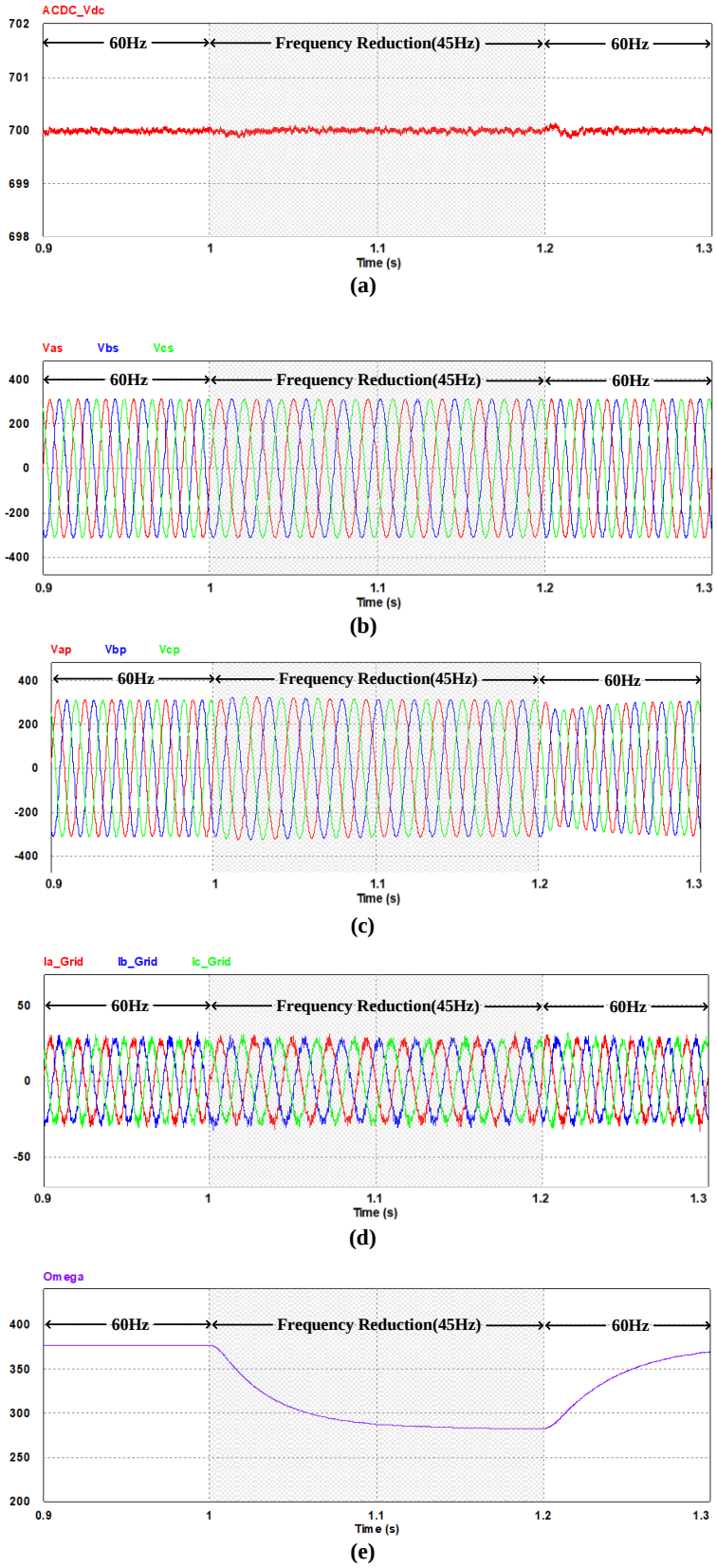


Figure 20. Waveforms of simulation results when grid frequency decreased from 60 Hz to 45 Hz drop; (**a**) the dc-link voltage; (**b**) the 3-phase input voltage; (**c**) the 3-phase input positive voltage detected by SOGI-FLL; (**d**) the 3-phase input current; and, (**e**) the center frequency that was extracted from SOGI-FLL.

In Figure 21, the conventional synchronous reference frame-phase locked loop (SRF-PLL) method [25] and SOGI-FLL method are compared to each other when the 3-phase grid voltage frequency is decreased from 60 Hz to 45 Hz. During power supply to 50 kW load, the grid frequency decreases to 45 Hz from 1 to 1.2 s, and then recovers to 60 Hz.

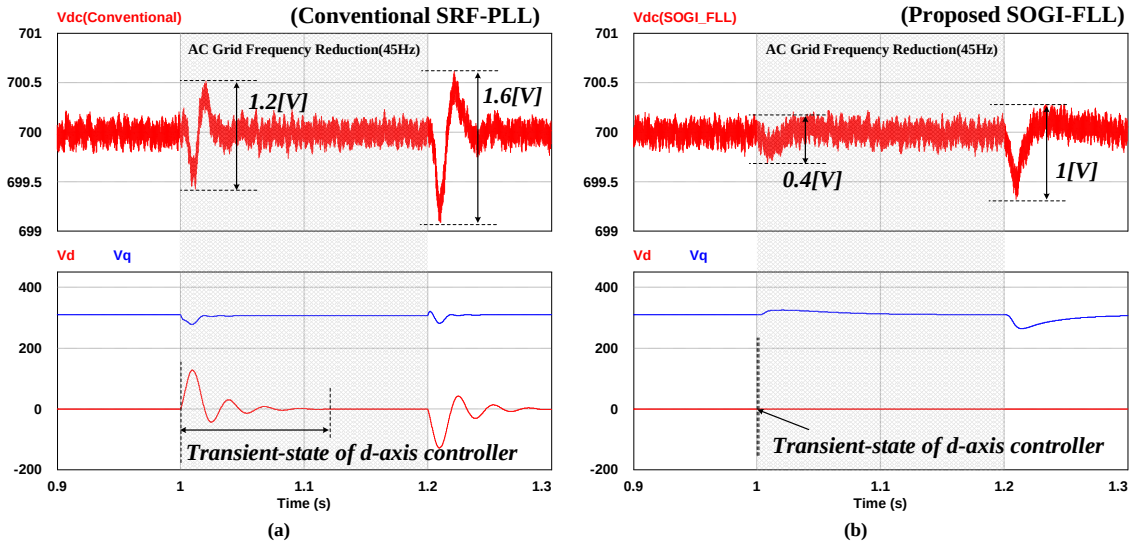


Figure 21. Waveforms of simulation results when frequency suddenly change (**a**) the DC-link voltage, *d* and *q*-axis voltage in synchronous reference frame with conventional synchronous reference frame-phase locked loop (SRF-PLL) (**b**) the DC-link voltage, *d* and *q*-axis voltage in synchronous reference frame with proposed control method.

Figure 21a shows that the *d*-axis voltage in a synchronous reference frame oscillates significantly when the grid frequency changes, and the dc-link voltage oscillation ranges from ± 0.5 to 0.9 V_{dc}. This oscillation of dc-link output voltage has the potential to adversely affect both the load and the dc-link capacitor. The oscillation occurs because the bandwidth of the controller is low due to the low cut-off frequency of the low pass filter. While this problem can be solved by increasing the cut-off frequency, the low frequency harmonics cannot be blocked.

On the other hand, in the voltages in the synchronous reference frame using SOGI-FLL, as shown in Figure 20b, no oscillation occurs in the *d*-axis voltage during the frequency change, and the transient state of the dc-link voltage is improved by about 50%.

As a result, the conventional SRF-PLL method takes a long time to stabilize the overshoot of the *d*-axis current controller in case of a frequency change because of the bandwidth problems in the controller due to digital filters, however, the proposed control method that is based on SOGI-FLL does not use these digital filters, so it is possible to stable and fast transient control.

5. Experiment Results

An experiment was performed to verify the feasibility of the proposed control method that is applied in a 3-phase AC/DC PWM converter for a DC distribution system. The configurations of the experimental system and power stacks are shown in Figures 22–24, and the experimental parameters are shown in Table 1.

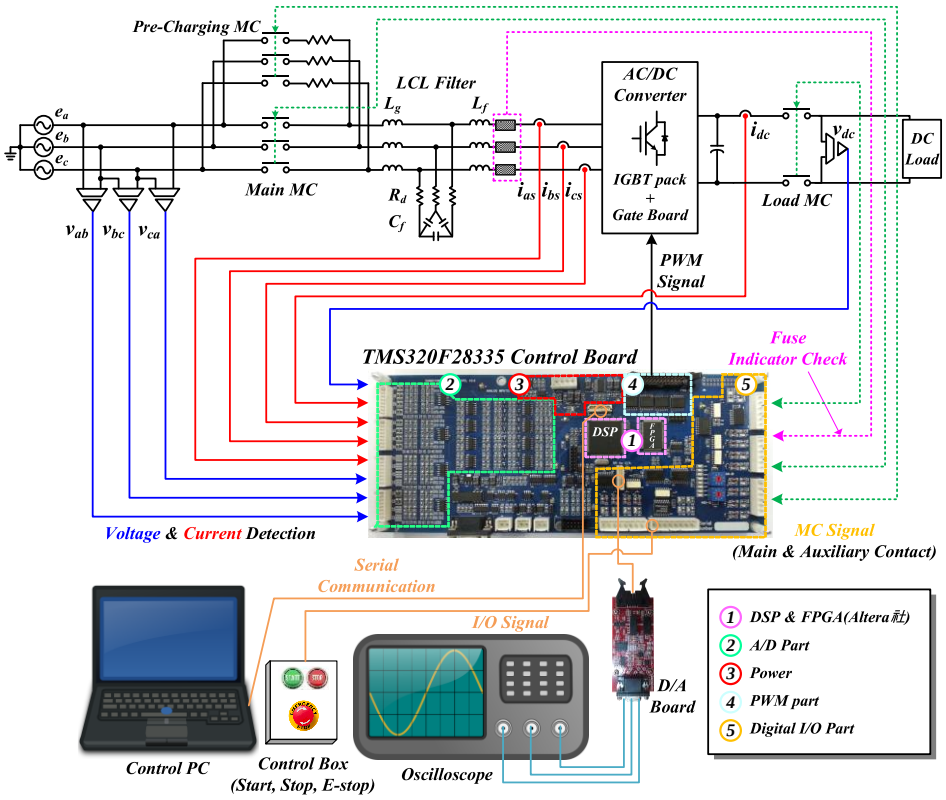


Figure 22. Configuration of the experiment system. MC: Magnetic Contactor.

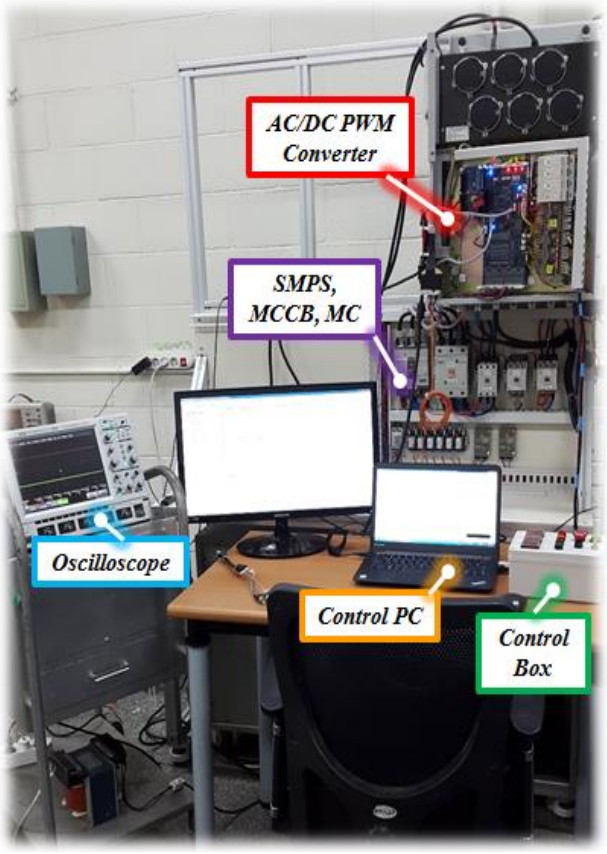


Figure 23. Experiment setup 1 of the 3-phase AC/DC PWM converter.

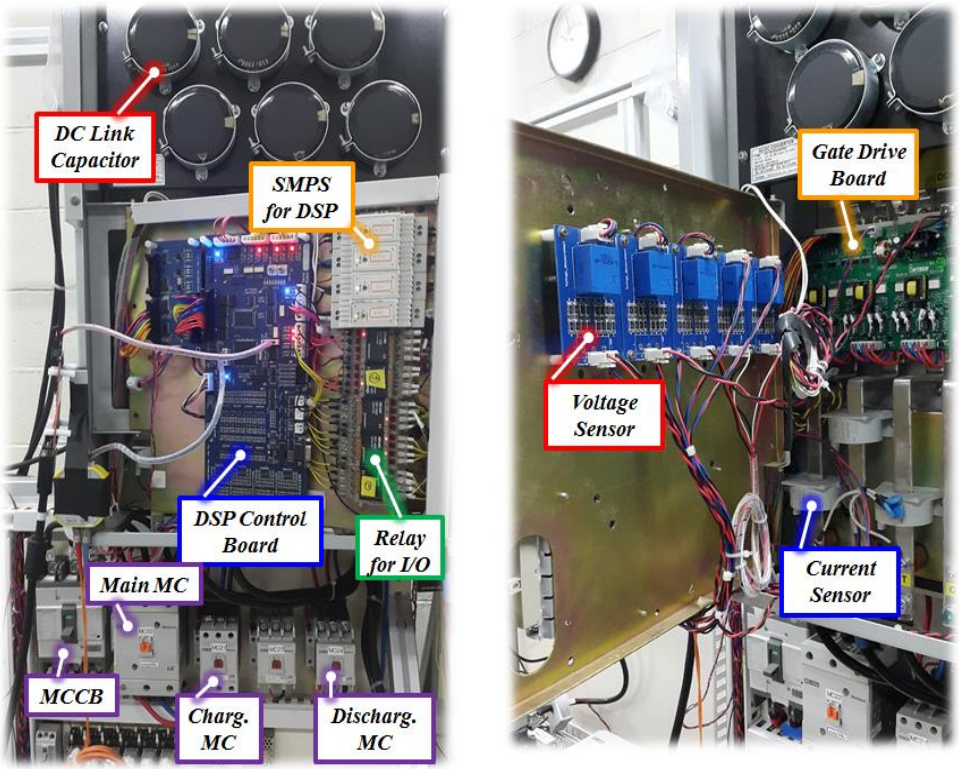


Figure 24. Experiment setup 2 of the 3-phase AC/DC PWM converter. SMPS: switched-mode power supply; DSP: digital signal processor; MCCB: molded case circuit breaker.

Figure 25 shows the waveforms for the operating sequence of a 3-phase AC/DC PWM converter for DC distribution. To prevent an excessive inrush current to the capacitor, the dc-link capacitor is charged while using an initial charging circuit consisting of magnetic switch and a resistor. After the initial charging is completed, the main magnetic switch is activated and the voltage is charged to the capacitor up to the input phase voltage peak value of 311 V_{dc}. The controller then starts to operate and the voltage increases up to 700 V_{dc}, which is the voltage reference, and the operation maintains steady state. As the load capacity increases, the output current gradually increases and the voltage remains constant, despite the increasing load.

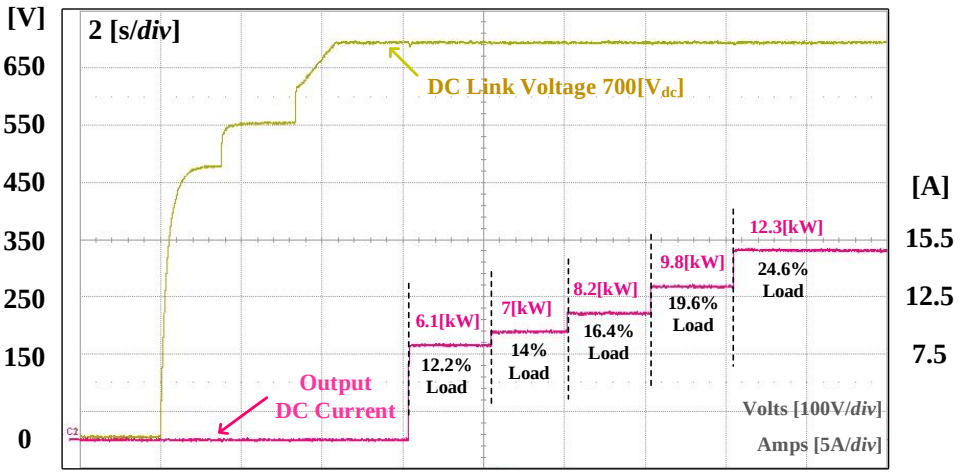


Figure 25. Waveform of 3-phase AC/DC PWM converter operation.

Figure 26 shows the input phase current waveform at the grid side when a load of 12.3 kW is applied, which is the largest capacity used of those shown in Figure 25. Since the load capacity is lower than that of the designed capacity of 50 kW, the current waveform includes the harmonics.

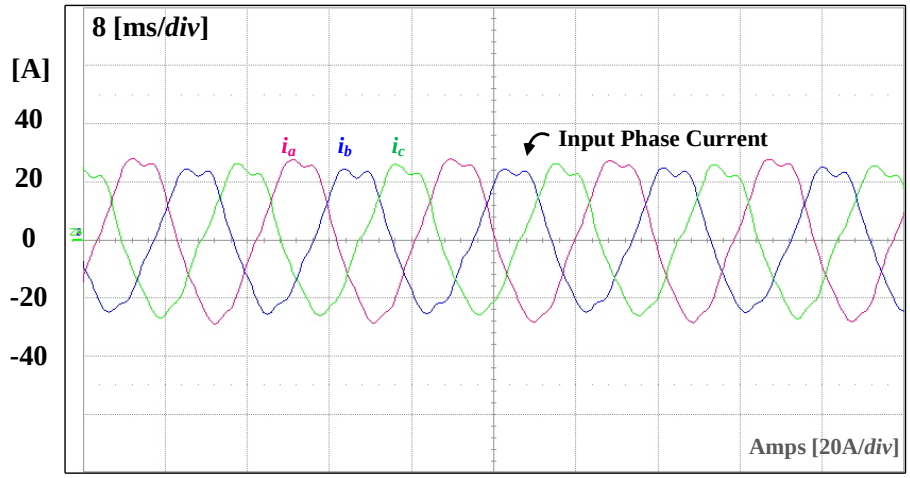


Figure 26. Waveform of input phase current of 3-phase AC/DC PWM converter.

Figure 27 shows the grid side input *a* voltage and current waveforms. The phase angle of the input phase voltage was extracted while using the positive sequence voltage and phase detector using SOGI-FLL without the need to use the PLL of the conventional control or the PLL used for the coordinate transformation of the phase current. In addition, the power factor is controlled to be 1 by adjusting the *d*-axis current command in the synchronous reference frame, which is a reactive power component. The phase detection performance of SOGI-FLL is then verified by experiment waveform.

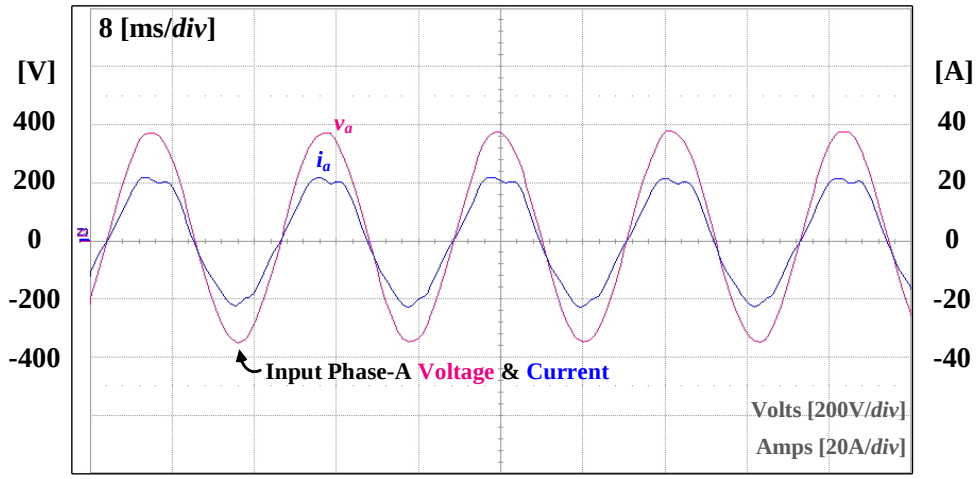


Figure 27. Waveform of input phase *a* voltage and current.

Figure 28 shows the 3-phase voltage waveform when a voltage drop (about 10%) occurs on the *b* phase. Figure 28b shows the expanded waveform of Figure 28a when the voltage drop occurs, and Figure 28c shows the waveform of the 3-phase positive sequence input voltage extracted while using SOGI-FLL. The amplitude of the 3-phase positive sequence voltage decreases due to the voltage drop. Even though the input 3-phase voltage is unbalanced, the extracted positive sequence voltage using SOGI-FLL maintains the balanced condition.

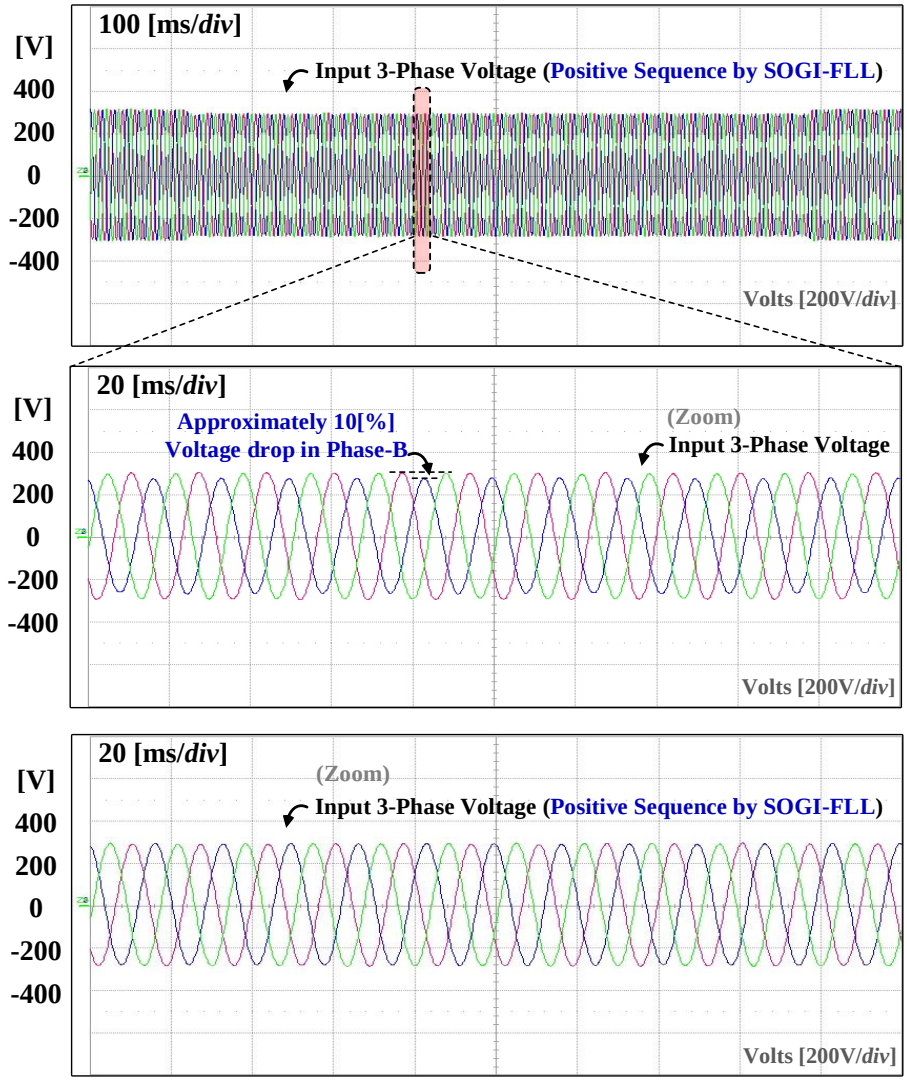


Figure 28. Waveforms of extracted 3-phase positive sequence input voltage using SOGI-FLL when the *b* phase has voltage drop.

Figure 29 shows the positive and negative sequence $\alpha\beta$ voltage and phase angle θ, before and after the *b* phase voltage drop. In the case of the $\alpha\beta$ voltage in the stationary reference frame, the amplitude and phase angle of the positive sequence component are always the same as these of the grid side. While the appearance of the negative sequence component is negligible at the steady state, the amplitude varies depending on the distortion in the unbalance condition. The phase angle θ of the positive sequence is always rotated in the same direction. In the case of a negative sequence, the magnitude, direction, and shape of the phase angle change depending on the balance, unbalance, and distortion.

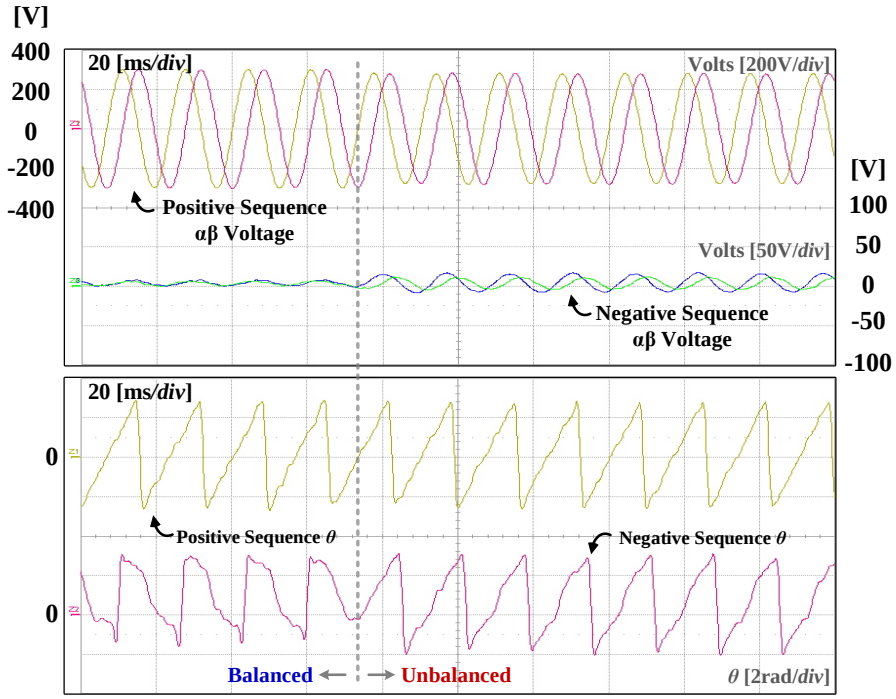


Figure 29. Waveform of detected positive/negative sequence $\alpha\beta$ voltage and phase angle θ (before and after b phase voltage drop).

6. Conclusions

In this paper, we studied a control method using SOGI-FLL for a 3-phase AC/DC PWM converter that is used in a DC distribution system. The proposed control method comprises a SOGI-FLL, which performs positive sequence voltage extraction, phase angle extraction, and harmonic filtering without an additional filter.

In DC distribution system, the power delivered to the load will depend on the 3-phase AC/DC PWM converter that is connected to the grid. However, the conventional control method with PLL used in 3-phase AC/DC PWM converter can not flexibly cope with the various conditions occurred in the grid. Unlike the conventional method, the proposed control method using SOGI-FLL can allow for the stable power to supply to the load in DC distribution even when various conditions occurred in the grid because it have stable and fast transient characteristics.

Experiment and simulation applied to 50 kW 3-phase 2-level AC/DC PWM converter was performed to verify the feasibility and effectiveness of the proposed control method. As a result, stable and fast transient control was verified while using the proposed method, even if the input voltage includes various harmonics, the frequency changes and a voltage drop occurs. Given those results, it is expected that the proposed method based on SOGI-FLL is one of good candidates for DC distribution system.

Author Contributions: J.-W.K., and K.-W.S. conceived and designed the experiment; J.-W.K. and K.-W.S. performed the experiment; J.-W.K., K.-M.K., H.L. and K.-W.S. analyzed the theory. J.-W.K. and H.L. wrote the manuscript. J.K. and C.-Y.W. participated in research plan development and revised the manuscript. All authors have contributed to the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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