



Article Double Adaptive PI-Structure for Regulating a Microgrid DC Bus Using a Flyback-Based Battery Charger/Discharger Converter

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Abstract: DC microgrids are composed of loads, renewable sources, and storage devices that require control and protection to operate safely. The flyback converter is an alternative to connect paralleled batteries with nominal voltage DC buses; however, until now, complex controllers have been proposed, making difficult their implementation. On the other hand, when the voltage of a DC microgrid is not properly controlled, the loads may be damaged due to the voltage outside of the safe range. Therefore, proposed in this paper are two adaptive PI-structures to control a battery charger based on a flyback converter to be used in DC microgrids. The first adaptive current controller regulates the magnetizing current for stabilizing the system, and the second adaptive voltage controller regulates the voltage of the DC bus to protect the elements of the microgrid. The methodology to design the adaptive parameters of the PI-structures is developed as follows: first, the power stage of the flyback converter is introduced to derive a control-oriented model. The battery and the DC bus of the microgrid, which are interfaced by the flyback converter, are represented with widely accepted approaches. The second step is focused on modeling the system. The flyback converter, which includes a capacitance to model the DC microgrid, is represented by a dynamic model. The differential equations are averaged, and several transfer functions of the main variables are obtained. In the third step, the transfer functions are used to design the PI adaptive current controller and the PI adaptive voltage controller. In the last step, several recommendations are made to implement the power and control stages in low-cost hardware. An application example with realistic parameters is carried out in PSIM to validate the controller loops design. A battery of 12 V is connected to a DC microgrid of 48 V through a flyback converter with a switching frequency of 50 kHz. The settling time and deviation of the DC microgrid voltage, after a perturbation, are 0.845 ms and 2.04 V respectively, while the maximum values are adjusted to be 1 ms and 2.4 V. The simulation results validate the proposed procedure and the effectiveness of the PI-structures in regulating the magnetizing current and the DC bus voltage.

Keywords: adaptive control structures; battery charger; DC microgrid; device protection; flyback converter; performance criteria; safe operation

1. Introduction

Energy storage systems (ESSs) are essential elements in AC and DC microgrids (MGs) since they compensate for the unbalances between generation and load produced by unpredictable renewable energy sources, like photovoltaic and wind turbine generators [1–3]. Although there are different ESSs technologies, like batteries, supercapacitors, flywheels, superconducting magnetic energy storage, pumped hydro, among others [4], batteries have established as the most widely used ESS technology. Lithium-ion batteries are particularly important since they correspond to 93% of the 5 GW energy storage capacity installed in 2020, according to the International Energy Agency [5].



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Copyright: © 2022 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https:// creativecommons.org/licenses/by/ 4.0/). In DC MGs, the battery, or array of batteries, are connected to the DC bus through a charging/discharging system, which is formed by two main elements: a bidirectional DC/DC converter and a control system. On the one hand, the DC/DC converter couples the battery voltage (v_b) to the DC bus voltage (v_{bus}) levels, where the common relation between v_b and v_{bus} is given by $v_b > v_{bus}$ [1,6]; hence, step-up DC/DC converters are typically used to implement a charging/discharging system [1,6]. On the other hand, the control system is aimed at regulating the DC voltage charging or discharging the battery when the power produced by the sources is higher or lower than the load, respectively. Therefore, the battery and the charging/discharging system compensate for the unbalances between generation and load by regulating the DC bus voltage [1,2]. Such regulation is important for the correct operation of the MG, since the loads may be disconnected or damaged if v_{bus} is out of the expected operating range.

In the literature it is possible to find charging/discharging systems implemented with different bidirectional converters like Boost [6,7], Buck-Boost [8,9], Cuk [10,11], Zeta/Sepic [12], Sepic/Zeta [13,14], or flyback [15]. The Boost converter has some advantages like its simplicity, reduced number of components, and simple control system, regarding Buck-Boost, Cuk, Zeta/Sepic, and Sepic/Zeta. Meanwhile, these last three converters stand out due to their capacity of operating as step-up or step-down converters and lower input (Cuk and Sepic/Zeta) or output (Zeta/Sepic) current and voltage oscillations regarding the Boost converter [16]. Nevertheless, these four converters (Boost, Buck-Boost, Cuk, Zeta/Sepic, Sepic/Zeta) have limited voltage gains; consequently, v_b must be close to v_{bus} , which is achieved by connecting batteries in series. The connection of batteries in series may result in imbalances in their state-of-charge due to differences in the active material and internal resistance resulting from the manufacturing process, as well as differences in the charging/discharging currents and operating temperature [17,18]. These differences may produce the overcharge or undercharge of the individual batteries, which reduces the batteries' lifetime [18,19].

The flyback converter has the advantage of providing high voltage gains by modifying the turn ratio of its transformer, which allows the connection of a battery, or array of parallel batteries, directly to the DC bus—thus avoiding the connection of the batteries in series and reducing the unbalances among the state-of-charge of the batteries. Moreover, the flyback converter has a simple structure and provides galvanic isolation between the battery and the load. That is why this converter is used in the charging/discharging system proposed in [15] and the converter considered in this paper.

The controller for the flyback-based charging/discharging proposed in [15] is an adaptive Sliding-Mode Controller (SMC), whose main objective is to regulate the DC bus voltage. The SMC switching function is defined as $\Psi = K_v \cdot (v_{bus} - v_r) + K_i \cdot i_m - i_{bus}$, where v_r is the reference value of v_{bus} , i_m is an estimation of the magnetizing current, i_{bus} is the DC bus current, and K_v and K_i are two controller's constants. The constant K_i is dynamically calculated from v_b , v_{bus} , the transformer turn ratio, and the transformer inductances (i.e., magnetizing and leakage) to ensure the system stability; while K_v is a fixed value calculated to obtain the desired dynamic behavior of v_{bus} . Nevertheless, the controller proposed in [15] results in a variable switching frequency of the MOSFETs, which makes difficult the converter design as well as the design and implementation of filters for the measured signals. Moreover, the implementation of the hysteresis band usually requires analog circuitry, which increases the number of components required to implement the controller.

Although there is no other flyback-based charging/discharging system proposed in the literature, to the best knowledge of the authors, it is possible to find flyback-based battery charging or discharging systems with controllers simpler than SMC that provide fixed-frequency operation. For example, the authors of [20–22] use PI controllers for different applications that use a flyback converter to charge [20,21] or discharge a battery [22]. Particularly, in [20–22] the authors use a single PI to regulate the flyback output voltage for three different applications: charging an auxiliary battery for a MG, charging the battery of

a phone [20], and feeding a LED light system [22]. However, these papers do not provide general design procedures that can be applied for other applications, since in [20] the authors determine the PI's proportional gain (k_p) and the integral time (t_i) by testing three different arbitrary values for each parameter, while in [21,22] the authors do not provide any design procedure of k_p and t_i .

The solutions proposed in [23,24] have the same structure as the ones introduced in the previous paragraph, but they use a two-poles/two-zeros compensator instead of a PI, and the flyback output voltage is regulated to feed a DC motor. In both papers, the compensator's parameters are designed to obtain the desired frequency response in a particular operating point of the system.

Other papers report cascade PIs to regulate the flyback output voltage to implement an electric vehicle battery charger [25,26], where the flyback input voltage is regulated by another converter with an independent controller. The cascade controller proposed in these papers has an inner loop with a PI that tracks a reference of the current injected to the battery, while the outer loop is a PI that regulates the flyback output voltage by manipulating the reference of the inner loop. In [26] the authors use frequency response to determine k_p and t_i of both PIs to obtain a stable system for a particular operating point. Nevertheless, in [25] the authors do not provide any design procedure for the proposed controllers.

The linear controllers for flyback-based charging or discharging (i.e., one direction of power flow) systems described before are designed for a single operating point with fixed controller parameters. Therefore, those controllers cannot guarantee the same dynamic performance of the system for any operating condition. Moreover, the papers that use linear controllers do not provide a detailed design procedure to determine the controllers' parameters, which makes difficult their application for a charging/discharging system power flows in both directions of the converter. Additionally, the SMC controller proposed in [15] provides a variable switching frequency of the converter, which makes it difficult to design the converter and filters, and requires analog circuitry for its implementation.

This paper proposed a cascade linear controller with adaptive parameters for a flybackbased charging/discharging system along with a detailed design procedure of the controller's parameters. In the cascade controller, the outer loop regulates the DC bus voltage by manipulating the magnetizing current reference, whereas the inner loop tracks such reference by modifying the duty cycle. The inner loop is implemented with a proportional controller with an adaptive gain (k_i) to guarantee that the closed-loop crossover frequency is 1/5 of the switching frequency (*F*); while the outer loop is realized with a PI with two adaptive parameters (x_p and x_i), where x_p assures a damping ratio equal to 1 whilst x_i is designed to fulfill the desired settling time, a maximum deviation, and a closed-loop crossover frequency less than F/25. The paper includes a detailed design procedure for the three controller parameters and guarantees the same dynamic performance of the DC bus voltage for any operating condition. Therefore, the main contributions of the paper are: (1) a cascade controller implemented with two adaptive linear compensators that guarantee the system stability and the desired dynamic performance for any operating point and mode (i.e., charging, discharging, or null); (2) a detailed design procedure of the cascade controller parameters (k_i , x_p , and x_i) considering the system stability and the bandwidth restrictions of the inner and outer loops; (3) a flyback-based charging/discharging system that operates at a constant switching frequency with an adaptive linear controller, which facilitates the design of the converter as well as the controller implementation.

The rest of the paper is organized as follows: Section 2 introduces a control-oriented model of the system, the description of the proposed cascade controller, and the design procedure. Section 3 shows an application example of the proposed design procedure, which illustrates that the system is stable and show the same dynamic performance for different operating conditions. Section 4 closes the paper with the conclusions.

2. Proposed Cascade Controller and Design Procedure

This section begins with the description of the charging/discharging system considered in this paper along with its main elements. Such description is used afterward to explain the control-oriented model used for the analysis and design procedure of magnetizing current controller. With the inner controller designed, the section continues with the system model assuming a controlled magnetizing current, which is used to analyze the DC bus voltage adaptive PI regulator and its design procedure. This section closes with a summary of the proposed controller design procedure to help the reader with its implementation.

2.1. Circuital Interface

The power electronics interface proposed for this application is based on a bidirectional implementation of a flyback converter. The main advantages of this converter are the galvanic isolation, which protects the battery from failures occurring on the DC bus due to problems on the devices of the MG; and the variable voltage conversion ratio, which enables to develop a single solution suitable for multiple MGs with different bus voltage requirements.

A simplified model of the battery interface application is presented in Figure 1, which shows the flyback converter modeled with an ideal transformer with a turn ratio 1:*n* interacting with both the magnetizing (L_m) and the leakage (L_k) inductances. Such a power converter is designed with two complementary MOSFETs (MOS₁ and MOS₂) to enable the bidirectional power flow between the battery and the bus; moreover, those MOSFETs are activated using a complementary dual driver, such as the UC1715 Complementary Switch FET Driver [27], which produces the complementary activation signals *u* for MOS₁ and $\bar{u} = 1 - u$ for MOS₂. The control signal of this power circuit is the duty cycle *d* of the converter, thus a PWM circuit is included in the circuital interface of Figure 1. The MOSFETs are selected to have built-in current sensing capabilities, which are needed to implement the control structure of the battery interface. Some examples of those MOSFETs are the BUK7908-40AIE [28], BUK7107-55AIE [29], and IMZ120R045M1 [30], which have TrenchPLUS current sensing circuits; and the IRCZ24 [31] that has HEXSence internal current sensors. Finally, the capacitance of the bus is labeled as C_{bus} , which must be designed depending on the MG requirements as will be discussed in Section 2.4.



Figure 1. Flyback-based circuital interface for bidirectional power flow.

The circuital interface of Figure 1 models the battery with the voltage source v_b , and the MG bus is modeled with the C_{bus} capacitance and the current source i_{bus} , which combines the currents provided by the sources and consumed by the MG loads. Finally, the circuital interface has the following sensors for control purposes: the MOSFETs currents i_{M1} and i_{M2} , the battery voltage v_b , the bus voltage v_{bus} , and the current exchanged with the bus i_{bus} , which could be positive (discharge mode), negative (charge mode), or zero (null mode).

This circuital interface must be controlled, by imposing an appropriate duty cycle, to provide a regulated bus voltage, which ensures a safe operation of the devices forming the MG. The following sections deal with the design of such a controller.

2.2. Control-Oriented Model

The correct design of the bus voltage controller requires a control-oriented model of the circuital interface, which is developed in this subsection.

The first state of the circuital interface occurs when u = 0 (thus $\bar{u} = 1$), which produces the following equations for the bus voltage v_{bus} , magnetizing current i_m , leakage current i_k , MOSFETs currents i_{M1} and i_{M2} :

$$\frac{dv_{bus}}{dt} = \frac{1}{C_{bus}} \cdot \left(\frac{i_m}{n} - i_{bus}\right) \tag{1}$$

$$\frac{di_m}{dt} = -\frac{1}{n} \cdot \left(\frac{v_{bus}}{L_m + \frac{L_k}{n^2}}\right) \tag{2}$$

$$i_{M1} = 0 \tag{3}$$

$$i_{M2} = -i_k = -\frac{i_m}{n} \tag{4}$$

Similarly, the second state of the circuital interface occurs when u = 1 (thus $\bar{u} = 0$), which produces the following equations:

$$\frac{dv_{bus}}{dt} = -\frac{i_{bus}}{C_{bus}} \tag{5}$$

$$\frac{di_m}{dt} = \frac{v_b}{L_m} \tag{6}$$

$$i_{M1} = i_m \tag{7}$$

$$i_{M2} = -i_k = 0 \tag{8}$$

Those equations are averaged within the switching period *T* of the PWM using the duty cycle definition $d = \frac{1}{T} \cdot \int_0^T u \, dt$, where F = 1/T is the switching frequency:

$$\frac{dv_{bus}}{dt} = \frac{\left(\frac{i_m}{n}\right) \cdot (1-d) - i_{bus}}{C_{bus}} \tag{9}$$

$$\frac{di_m}{dt} = \frac{v_b \cdot d}{L_m} - \frac{1}{n} \cdot \left[\frac{v_{bus} \cdot (1-d)}{L_m + \frac{L_k}{n^2}} \right]$$
(10)

$$i_{M1} = i_m \cdot d \tag{11}$$

$$i_{M2} = -i_k = -\frac{i_m}{n}(1-d) \tag{12}$$

In stable conditions the previous derivatives are equal to (or near) zero, which leads to the following stable values for the duty cycle and magnetizing current:

$$d = \frac{1}{1 + n \cdot \left(\frac{v_b}{v_{bus}}\right) \cdot \left(1 + \frac{L_k}{n^2 \cdot L_m}\right)} \tag{13}$$

$$i_m = \frac{n \cdot i_{bus}}{1 - d} \tag{14}$$

The next step to obtain a control-oriented model is to summarize the averaged differential Equations (9) and (10) into the following matrix format:

$$\frac{dX_m}{dt} = A_m \cdot X_m + B_m \cdot U_m \tag{15}$$

$$Y_m = C_m \cdot X_m + D_m \cdot U_m \tag{16}$$

For this circuital interface, the states vector X_m and the inputs vector U_m are defined as given in (17), which produces the A_m and B_m matrices reported in (18) and (19), respectively.

$$X_m = \begin{bmatrix} i_m \\ v_{bus} \end{bmatrix} \land U_m = \begin{bmatrix} d \\ v_b \\ i_{bus} \end{bmatrix}$$
(17)

$$A_m = \begin{bmatrix} 0 & -\frac{1-d}{n \cdot \left(L_m + \frac{L_k}{n^2}\right)} \\ \frac{1-d}{n \cdot C_{bus}} & 0 \end{bmatrix}$$
(18)

$$B_m = \begin{bmatrix} \frac{v_b}{L_m} + \frac{v_{bus}}{n \cdot \left(L_m + \frac{L_k}{n^2}\right)} & \frac{d}{L_m} & 0\\ -\frac{i_m}{n \cdot C_{bus}} & 0 & -\frac{1}{C_{bus}} \end{bmatrix}$$
(19)

Matrices C_m and D_m depend on the outputs Y_m defined for the system. Since the main objective is to regulate the bus voltage to ensure a safe operation of the MG, thus, the first option is to define $Y_{m,v} = [v_{bus}]$, which produces the matrices $C_{m,v} = [0 \ 1]$ and $D_{m,v} = [0 \ 0 \ 0]$. Then, applying the matrix-to-transfer function transformation $\frac{V_{bus}(s)}{d(s)} = C_{m,v} \cdot (s \cdot I - A_m)^{-1} \cdot B_m + D_{m,v}$, where *s* is the Laplace variable and *I* is the identity matrix, leads to the following transfer function:

$$\frac{V_{bus}(s)}{d(s)} = \frac{\left(\frac{1-d}{n\cdot C_{bus}}\right) \cdot \left[\frac{v_b}{L_m} + \frac{v_{bus}}{n\cdot \left(L_m + \frac{L_k}{n^2}\right)}\right] - \left(\frac{i_m}{n\cdot C_{bus}}\right) \cdot s}{s^2 + \frac{(1-d)^2}{n^2 \cdot C_{bus} \cdot \left(L_m + \frac{L_k}{n^2}\right)}}$$
(20)

The previous transfer function has a right-hand zero (RHZ), i.e., a positive zero; hence, a feedback linear-loop for a power converter designed with such a transfer function will be unstable as discussed in [32]. Therefore, the voltage in this type of system is commonly regulated using cascade structures with an inner current controller as it is discussed in [25,26], which avoids the problem of the RHZ if it is not present in the current-to-duty cycle transfer function.

To design an inner current controller, it is necessary to obtain the $\frac{I_m(s)}{d(s)}$ transfer function. Thus, the output vector is defined as $Y_{m,i} = [i_m]$, which produces the matrices $C_{m,i} = [1 \ 0]$ and $D_{m,i} = [0 \ 0 \ 0]$. Then, applying the matrix-to-transfer function transformation $\frac{I_m(s)}{d(s)} = C_{m,i} \cdot (s \cdot I - A_m)^{-1} \cdot B_m + D_{m,i}$ leads to the following transfer function:

$$G_{i_m,d}(s) = \frac{I_m(s)}{d(s)} = \frac{s \cdot \left\lfloor \frac{v_b}{L_m} + \frac{v_{bus}}{n \cdot \left(L_m + \frac{L_k}{n^2}\right)} \right\rfloor + \left(\frac{(1-d) \cdot i_m}{n^2 \cdot C_{bus} \cdot \left(L_m + \frac{L_k}{n^2}\right)}\right)}{s^2 + \frac{(1-d)^2}{n^2 \cdot C_{bus} \cdot \left(L_m + \frac{L_k}{n^2}\right)}}$$
(21)

Such a transfer function (21) does not have RHZ because all the terms in the numerator are positive (including 1 - d > 0); thus, it is possible to design a stable current loop for the flyback converter using a linear controller. The $G_{i_m,d}(s)$ transfer function is rewritten as given in (22) to reduce the mathematical expressions, where z_1 and z_2 given in (23) describe the zero, and σ given in (24) describes the poles. It must be noted that z_2 expression uses the steady i_m value previously obtained in (14).

$$G_{i_m,d}(s) = \frac{z_1 \cdot s + z_2}{s^2 + \sigma^2}$$
(22)

$$z_1 = \frac{v_b}{L_m} + \frac{v_{bus}}{n \cdot \left(L_m + \frac{L_k}{n^2}\right)} \quad \wedge \quad z_2 = \frac{i_{bus}}{n \cdot C_{bus} \cdot \left(L_m + \frac{L_k}{n^2}\right)} \tag{23}$$

$$\sigma = \frac{1-d}{n \cdot \sqrt{C_{bus} \cdot \left(L_m + \frac{L_k}{n^2}\right)}}$$
(24)

Finally, the previous z_1 , z_2 , and σ values must be evaluated at the operating point in which the MG is operating. Therefore, the following sections propose adaptive controllers, which are automatically modified to compensate for the changes on z_1 , z_2 , and σ .

2.3. Adaptive Current Controller

The design of the current controller is performed using the $G_{i_m,d}(s)$ transfer function given in (22); thus, the duty cycle *d* is generated to regulate the magnetizing current i_m . This process is carried out adopting the feedback structure presented in Figure 2, where the proportional controller k_i is located in the feedback loop.



Figure 2. Current loop based on a proportional controller.

The design of the k_i value requires the calculation of the closed-loop transfer function T_i , which describes the behavior of $I_m(s)$ for changes on the reference value $I_r(s)$. Applying block diagram algebra to Figure 2 leads to the following transfer function for the current loop:

$$T_i(s) = \frac{I_m(s)}{I_r(s)} = \frac{z_1 \cdot s + z_2}{s^2 + (k_i \cdot z_1) \cdot s + (k_i \cdot z_2 + \sigma^2)}$$
(25)

Taking into account that the magnetizing current is not the main variable intended to be controlled, the only restriction applied to T_i is to constrain the transfer function gain at the maximum frequency in which the averaged model (21) accurately represents the circuit behavior. The gain of the $T_i(s)$ transfer function, given as a function of the angular frequency, is reported in (26).

$$|T_{i}(\omega)| = \frac{\sqrt{z_{1}^{2} \cdot \omega^{2} + z_{2}^{2}}}{\sqrt{(k_{i} \cdot z_{2} + \sigma^{2} - \omega^{2})^{2} + (k_{i} \cdot z_{1} \cdot \omega)^{2}}}$$
(26)

The bandwidth of the closed loop transfer function $T_i(s)$ must be restricted to the bandwidth of the model $G_{i_m,d}(s)$ used for the control design, otherwise the closed-loop system will operate in a frequency range in which the converter has not been modeled. In [33] it was confirmed the validity of the averaged model of a switching converter at 1/5 of the switching frequency (*F*), thus that is the bandwidth adopted for the design of k_i . Therefore, Equation (26) must be solved for a gain of $-3 \text{ dB} = \frac{1}{\sqrt{2}}$, which is assumed as a cut-gain of transfer functions, thus solving $\left|T_{i(\omega_x)}\right| = \frac{1}{\sqrt{2}}$ for an angular frequency $\omega_x = 2 \cdot \pi \cdot F/5$ results in the following k_i expression:

$$k_{i} = \frac{-z_{2} \cdot (\sigma^{2} - \omega_{x}^{2}) + \sqrt{z_{2}^{2} \cdot (\sigma^{2} - \omega_{x}^{2})^{2} - (z_{1}^{2} \cdot \omega_{x}^{2} + z_{2}^{2}) \cdot \Phi}}{z_{1}^{2} \cdot \omega_{x}^{2} + z_{2}^{2}}$$

$$\text{where} \quad \Phi = -2 \cdot (z_{1}^{2} \cdot \omega_{x}^{2} + z_{2}^{2}) + (\sigma^{2} - \omega_{x}^{2})^{2}$$

$$(27)$$

Therefore, the k_i value must be dynamically calculated, using (27), to ensure the desired behavior of the current controller for any operating condition. Taking into account that z_1 , z_2 , and σ depend on v_b , v_{bus} , and i_{bus} , such variables must be measured to update periodically the k_i value, thus adapting the current controller to the operating conditions imposed by both the battery and MG.

Finally, the steady-state gain M_i of the current loop transfer function (25) must be calculated, since such gain affects the stable value of the magnetizing current as $I_m = M_i \cdot I_r$. Therefore, such an M_i gain must be included in the model designed to develop the bus voltage controller, which is analyzed in the following section. The M_i value is calculated by evaluating (26) for $\omega = 0$ rad/s as follows:

$$M_{i} = \lim_{\omega \to 0} \left| T_{i(\omega)} \right| = \frac{z_{2}}{k_{i} \cdot z_{2} + \sigma^{2}} = \frac{1}{k_{i} + \frac{(1-d)^{2}}{n \cdot i_{pus}}}$$
(28)

It must be noted that the final M_i value was calculated by replacing the z_2 and σ values given in (23) and (24), respectively, and using the k_i value updated with Equation (27). Therefore, the M_i value is also an adaptive quantity.

2.4. Adaptive Voltage Controller

The next step needed to design the bus voltage controller is to obtain a closed-loop model of the circuital interface including the current control loop. The electrical equivalent of the flyback converter considering the current loop is presented in Figure 3a, where the average current of the second MOSFET i_{M2} is regulated by the current loop, which imposes the value reported in Equation (12) with $i_m = M_i \cdot i_r$.



(a) Electrical equivalent considering the current loop

Figure 3. Voltage loop based on a cascade controller.

Applying the Kirchhoff current law and capacitor differential equation to the circuit of Figure 3a, in the Laplace domain, leads to the bus voltage equation given in (29). Such an

expression depends on both the reference current i_r and bus current i_{bus} , where the latter one corresponds to the main perturbation of the system. From such an expression, two transfer functions are defined: G_{v,i_r} given in (30), which describes the behavior of v_{bus} to changes on the current reference i_r ; and $G_{v,i_{bus}}$ given in (31), which describes the behavior on v_{bus} to perturbations on the bus current i_{bus} .

$$v_{bus} = \frac{1}{s \cdot C_{bus}} \cdot \left[\frac{M_i \cdot (1-d)}{n} \cdot i_r - i_{bus} \right]$$
(29)

$$G_{v,i_r} = \frac{v_{bus}}{i_r} = \frac{M_i \cdot (1-d)}{s \cdot n \cdot C_{bus}}$$
(30)

$$G_{v,i_{bus}} = \frac{v_{bus}}{i_{bus}} = \frac{-1}{s \cdot C_{bus}} \tag{31}$$

Figure 3b shows the block diagram of the cascade voltage loop, which considers a voltage controller named H_v . Such a voltage controller processes the error between the voltage reference v_r and the bus voltage v_{bus} to produce the reference i_r of the current loop. Thus, the output of the voltage controller i_r is the input of the transfer function G_{v,i_r} , while bus current i_{bus} is the input of the transfer function $G_{v,i_{bus}}$. Finally, the bus voltage is the result of the contribution of both G_{v,i_r} and $G_{v,i_{bus}}$.

This work proposes the design of a classical PI controller for H_v as given in (32), where x_p is the proportional parameter and x_i is the integral parameter.

$$H_v = x_p + \frac{x_i}{s} \tag{32}$$

Applying block diagram algebra to Figure 3b leads to the transfer function for the voltage loop given in (33), which describes the effect of i_{bus} perturbations on the bus voltage v_{bus} . Thus, the design of H_v parameters must be performed using such a transfer function. However, it is noted that the transfer function coefficients depend on both M_i and d, which change with the operating point. Therefore, H_v parameters x_p and x_i must be adapted to ensure consistent behavior of the bus voltage.

$$T_{v} = \frac{v_{bus}}{i_{bus}} = \frac{-s}{C_{bus} \cdot s^{2} + \left[\frac{x_{p} \cdot M_{i} \cdot (1-d)}{n}\right] \cdot s + \left[\frac{x_{i} \cdot M_{i} \cdot (1-d)}{n}\right]}$$
(33)

The adaptation of x_p and x_i is performed by normalizing those values concerning both M_i and d, obtaining the normalized parameters α_p and α_i as given below:

$$\alpha_p = x_p \cdot M_i \cdot (1-d) \quad \land \quad \alpha_i = x_i \cdot M_i \cdot (1-d) \tag{34}$$

Then, replacing the normalized parameters (34) into the bus voltage transfer function (33) leads to the normalized closed-loop transfer function given in (35), which exhibits constant coefficients, thus a consistent behavior of the bus voltage could be ensured.

$$T_{v,N} = \frac{v_{bus}}{i_{bus}} = \frac{-s}{C_{bus} \cdot s^2 + \frac{\alpha_p}{n} \cdot s + \frac{\alpha_i}{n}}$$
(35)

The controller design must be performed for the worst perturbation possible on the bus current, which corresponds to a step current with an arbitrary amplitude ΔI_{bus} ; thus, in the Laplace domain, it is $i_{bus} = \frac{\Delta I_{bus}}{s}$. Then, evaluating the bus voltage from the normalized transfer function (35) considering the previous step current on the bus results in the following Laplace expression:

$$v_{bus} = \frac{-\frac{\Delta I_{bus}}{C_{bus}}}{s^2 + \frac{\alpha_p}{n \cdot C_{bus}} \cdot s + \frac{\alpha_i}{n \cdot C_{bus}}}$$
(36)

Considering the canonical second-order denominator $s^2 + 2 \cdot \rho \cdot \omega_n \cdot s + \omega_n^2$ enables to obtain the expressions for the natural frequency ω_n and damping ratio ρ of the previous transfer function, as follows:

$$\omega_n = \sqrt{\frac{\alpha_i}{n \cdot C_{bus}}} \quad \wedge \quad \rho = \frac{\alpha_p}{2 \cdot \omega_n \cdot n \cdot C_{bus}} \tag{37}$$

To provide a bus voltage without oscillations, the damping ratio is defined as $\rho = 1$. Then, replacing such ρ value in (37) results in the following relation between α_p and α_i :

$$\alpha_p = 2 \cdot \sqrt{C_{bus} \cdot n \cdot \alpha_i} \tag{38}$$

Replacing the previous relation into expression (36), and applying the inverse Laplace transformation, leads to the time-domain waveform of the bus voltage given in (39), which is the response of the voltage loop to the worst-case perturbation $i_{bus} = \frac{\Delta I_{bus}}{s}$.

$$v_{bus} = -\frac{\Delta I_{bus}}{C_{bus}} \cdot t \cdot e^{-\sqrt{\frac{\alpha_i}{C_{bus} \cdot n}} \cdot t}$$
(39)

The design of the voltage controller is performed to impose the following performance criteria:

- 1. Maximum settling time t_s needed to restore the bus voltage into an acceptable band $[-\epsilon, \epsilon]$. In engineering, the most commonly used band for the settling time is $\epsilon = 2\%$, but any other value can be used depending on the MG requirements.
- 2. Maximum bus voltage deviation *MD* after the bus current perturbation occurs.
- 3. Finally, in [33] was confirmed that the validity of the current loop model on a cascade voltage control structure, like the one modeled in Figure 3, is limited to 1/5 of the current loop bandwidth. Therefore, since the current loop bandwidth was limited to $\omega_x = 2 \cdot \pi \cdot F/5$, the cut-gain frequency ω_c of the transfer function (36) must be limited to 1/25 of the switching frequency; thus, a maximum angular frequency $\omega_c = 2 \cdot \pi \cdot F/25$ must be ensured.

For the first performance criterion, i.e., the settling time, Expression (39) is solved for $v_{bus} = \epsilon \cdot v_r$ and $t = t_s$ by using the LambertW function (W), which provides the expression of t_s as a function of the controller parameter α_i and bus capacitance C_{bus} :

$$t_{s} = \frac{-W\left(\frac{-\epsilon \cdot v_{bus} \cdot \sqrt{\frac{C_{bus} \cdot \alpha_{i}}{n}}}{\Delta I_{bus}}\right)}{\sqrt{\frac{\alpha_{i}}{C_{bus} \cdot n}}}$$
(40)

For the second performance criterion, i.e., the maximum deviation, Expression (39) is derived as given in (41), which enables to find the time t_{MD} needed to reach the maximum voltage deviation that occurs when $\frac{dv_{bus}}{dt} = 0$; Equation (42) provides the expression for t_{MD} .

$$\frac{dv_{bus}}{dt} = \frac{\Delta I_{bus}}{C_{bus}} \cdot \left(e^{-\sqrt{\frac{\alpha_i}{C_{bus} \cdot n}} \cdot t}\right) \cdot \left(1 - t \cdot \sqrt{\frac{\alpha_i}{C_{bus} \cdot n}}\right)$$
(41)

$$t_{MD} = \sqrt{\frac{C_{bus} \cdot n}{\alpha_i}} \tag{42}$$

Finally, replacing the previous t_{MD} value on the bus voltage Equation (39) provides the expression of *MD* as a function of the controller parameter α_i and bus capacitance C_{bus} :

$$MD = -\frac{\Delta I_{bus}}{e} \cdot \sqrt{\frac{n}{C_{bus} \cdot \alpha_i}}$$
(43)

The third performance criterion is calculated by first obtaining the magnitude of (35) depending on the angular frequency as given in (44). Then, solving that equation for the -3 dB magnitude, thus $|T_{v,N(\omega)}| = \frac{1}{\sqrt{2}}$, provides the expression of the cut-gain frequency ω_c as a function of the controller parameter α_i and bus capacitance C_{bus} , which must be lower or equal than F/25 as given in (45).

$$\left|T_{v,N(\omega)}\right| = \frac{\omega}{\frac{\alpha_i}{n} + C_{bus} \cdot \omega^2} \tag{44}$$

$$\omega_c = \frac{1}{2} \cdot \left(\frac{\sqrt{2}}{C_{bus}} + \sqrt{\frac{2}{C_{bus}^2} - \frac{4 \cdot \alpha_i}{C_{bus} \cdot n}} \right) \le \frac{F}{25}$$
(45)

Finally, the maximum acceptable setting time t_s^* and bus voltage deviation MD^* are defined depending on the operational requirements of the sources and loads connected to the MG. Therefore, the non-linear equation system given in (46) must be solved to calculate both the controller parameter α_i and bus capacitance C_{bus} needed to ensure the correct operation of the MG.

$$\begin{array}{c}
t_s \leq t_s^* \\
MD \leq MD^* \\
\omega_c \leq \frac{F}{25}
\end{array}$$
(46)

2.5. Summary of the Design Procedure

Figure 4 summarizes the offline process needed to design both the voltage controller parameters (α_i and α_p) and the bus capacitance (C_{bus}). Such a design process must be performed a single time since the adaptability of the control system will compensate for the changes in the operating point. The figure also summarizes the online process needed to adapt both the current and voltage loops to the changes on the operating point; this process must be performed in real-time, using analog or digital circuitry, to ensure that the controller parameters always have the correct values.



Figure 4. Flowchart of both design and adaptive processes.

3. Results and Discussion

This section introduces the validation of the proposed controller and its dynamic performance by using an application example for a battery charging/discharging system. The section begins with a description of the implementation of the proposed controller, including the estimation procedure of the magnetizing current and the online calculation of

the adaptive controller's parameters (k_i , x_p , and x_i). Then, the section shows the dynamic performance of the proposed controller beginning with the magnetizing current for charging, discharging, and null operating modes. Finally, the section introduces an example of the design procedure of the DC voltage regulator and shows that the dynamic behavior meets the desired criteria (t_s , MD, and w_c) for the different operating conditions.

3.1. Implementation of the Adaptive Control System

The implementation of the proposed control system is performed using Equations (27) and (28) for real-time calculation of k_i and M_i , respectively; Equation (34) is used for the real-time calculation of the adapted PI parameters x_p and x_i ; the feedback structure described in the block diagram of Figure 2 is used to implement the adaptive current loop, and the feedback structure described in the block diagram of Figure 3b is used to implement the adaptive voltage loop. Such an implementation scheme is depicted in Figure 5.



Figure 5. Implementation of the double-adaptive control system.

Moreover, the calculation of x_p and x_i requires the value d' = 1 - d; thus, such a calculation must be also performed in real-time. Finally, the current loop requires the value of the magnetizing current i_m , which cannot be directly measured; instead, the magnetizing current must be reconstructed from the MOSFETs built-in current sensors, which were discussed in Section 2.1 and Figure 1. Such a reconstruction of the magnetizing current i_m^* is based on Equations (4) and (7), as given in (47), which is also considered in the implementation scheme of Figure 5.

$$i_m^* = i_{M1} - n \cdot i_{M2} \tag{47}$$

Considering that Equations (27) and (28) require a lot of non-linear calculations, those expressions are most suitable to be processed with a digital microprocessor. Instead, the PI calculations (integration and addition) could be done using analog circuitry like operational amplifiers. On the other hand, the calculation of x_p and x_i requires divisions and multiplications, which can be done using digital or analog circuits; however, taking into account that Equations (27) and (28) must certainly be calculated using a microprocessor,

 x_p and x_i can be calculated inside the same microprocessor. The same approach can be applied to the calculation of d'. By contrast, the reconstructed magnetizing current i_m^* must be calculated using analog circuitry (operational amplifiers), since the current loop must be calculated as fast as possible. Finally, the duty cycle calculated by the current loop is delivered to the PWM, which interacts with a complementary dual-driver to act on both MOSFETs as discussed in Section 2.1.

3.2. Application Example and Validation

This subsection presents an application of the proposed solution using realistic parameters, which enables the validation of the proposed control strategy and design process. The main parameters of the application example are given in Table 1, which defines the switching frequency, battery and bus voltages, bus current range, and maximum bus current perturbation. In addition, the example considers a maximum safe deviation of the bus voltage equal to 5% (2.4 V), and a maximum 2% settling time equal to 1 ms. Finally, the transformer adopted for this application is the Vitec 58PR6962 [34], which is widely adopted in high-frequency converters [35].

Parameter	Value
<i>v</i> _r	48 V
v_b	12 V
F	50 kHz
i _{bus}	[-1,1] A
ΔI_{bus}	2 A
$t_{s}^{*}(2\%)$	1 ms
MD*	5%
n	5.4
L_m	20 μH
L_k	4 μΗ

Table 1. Parameters of the application example.

The validation of the proposed control system is performed using the professional power electronics simulator PSIM [36], which is widely used in the industry. Figure 6 shows the circuital implementation in PSIM of both power and control systems, which includes the real (non-linear) behavior of the MOSFETs, and both the magnetizing and leakage effects of the high-frequency transformer. Therefore, such a simulation tests the proposed control system under realistic conditions.

In such a circuital implementation, the calculation of k_i , M_i , d', x_p , and x_i is performed in real-time using a C-block. That a block is useful to simulate digital microprocessors programmed in C language, such as the TMS320F28335 from Texas Instruments [37], where the C code used to program the C-block can be used, without any major change, to program the digital microprocessor. This is possible due to the C-block uses ANSI C; hence, it is highly portable to other platforms.

Figure 6 also highlights the circuital implementation of both adaptive loops, including the reconstruction of the magnetizing current and the PWM circuit. Moreover, the power circuit includes two current sensors simulating the MOSFETs current sensing capabilities; and the bus current is simulated using a current source, which can be modified to simulate the MG current flow generated by the interaction of the devices (sources and loads) connected to the bus. Such a circuital implementation is used to perform two tests: the first one only evaluates the current loop—thus, the voltage loop is disconnected; the second one evaluates the complete control system—thus, both current and voltage loops are active.



Figure 6. Circuital implementation in PSIM of both power and control systems.

The first simulation considers the adaptive current loop designed in Section 2.3 following a pre-defined reference, which enables the validation of the correct adaptation of k_i even without the action of a voltage controller, i.e., with a non-regulated bus voltage. Figure 6 shows, in the red box, the PSIM implementation of the adaptive current loop; however, in this first simulation i_r is generated by a programmable source followed by a 10 kHz low-pass filter, which restricts the i_r bandwidth up to 1/5 of the switching frequency to fulfill the k_i design given in (27). Figure 7 reports the PSIM circuital simulation of the adaptive current loop for three reference values (i_r), where i_r is multiplied by the loop gain M_i (28) to validate the accurate regulation of the magnetizing current $i_m = M_i \cdot i_r$.



Figure 7. Circuital simulation of the adaptive current loop in PSIM for arbitrary values of i_r .

The simulation of Figure 7 confirms the correct regulation of the magnetizing current, which is achieved by adapting k_i to changes in the bus current, bus voltage, and magnetizing current. Moreover, the simulation also verifies the correct operation of the current loop for charge mode, discharge mode, and null mode, therefore confirming the correct behavior under any operating condition. The next step is to design the parameters of the adaptive voltage loop.

The normalized parameters α_p and α_i and the bus capacitance C_{bus} are calculated following the flowchart previously presented in Figure 4: solving the system of nonlinear equations reported in that flowchart, using the t_s^* and MD^* values given in Table 1, producing the solution spaces reported in Figure 8. In particular, Figure 8a shows the values of both C_{bus} and α_i needed to ensure a maximum deviation lower than MD^* , while Figure 8b shows the values of those parameters needed to ensure a settling time lower than t_s^* . Those figures provide the solution of (46) including the limitation of the voltage loop bandwidth to F/25 defined in (45), thus ensuring the stability of the voltage loop. From Figure 8a,b can be selected particular C_{bus} and α_i values to define precise $MD < MD^*$ and $t_s < t_s^*$ conditions; in this example, a commercially available $C_{bus} = 110 \ \mu\text{F}$ capacitance is selected, thus providing a 17% safe margin for the maximum deviation. Similarly, $\alpha_i = 6400 \ \text{A}/(\text{V} \cdot \text{s})$ is selected to provide a 15% safe margin for the settling time.



Figure 8. Plots used to design of C_{bus} and α_i . (a) Design of C_{bus} in terms of *MD*. (b) Design of α_i in terms of t_s .

Figure 9 shows the theoretical simulation of the bus voltage using the normalized waveform given in (36), where $\alpha_p = 3.8995 \text{ A/V}$ is calculated from (38). The figure confirms the accurate definition of both the settling time $t_s = 0.845$ ms and maximum deviation MD = 2.04 V, thus verifying the correctness of the design procedure summarized in the flowchart of Figure 4.



Figure 9. Theoretical simulation of the normalized voltage controller.

Finally, Figure 10 reports the complete PSIM simulation of the double adaptive PIstructure, which corresponds to the circuital implementation of Figure 6 including the adaptive voltage loop. This simulation considers a bus current profile with charge, discharge, and null conditions to evaluate the control system for all the possible conditions. The first step perturbation in the bus current has $\Delta i_{bus} = 2$ A as reported in Table 1, and the simulation shows a settling time $t_s = 0.845$ ms and a maximum voltage deviation MD = 2.04 V, which is in agreement with the design parameters selected from Figure 8 and with the theoretical results reported in the normalized simulation of Figure 9. Therefore, this circuital simulation confirms the validity of both the design process and the practical implementation reported in Figure 6. Moreover, the bus current also exhibits step changes for both charge and discharge conditions, where the bus voltage is always lower than MD; therefore, t_s and MD are always below the maximum limits defined in Table 1, i.e., $MD^* = 5\%$ and $t_s^* = 1$ ms, which ensures a safe operation of all the devices connected to the MG.



Figure 10. Circuital simulation of the double adaptive PI structure in PSIM.

The simulation of Figure 10 also shows the correct operation of the adaptive current loop, since the magnetizing current i_m is always equal to the theoretical value $i_r \cdot M_i$. Finally, the figure also shows the dynamic adaptation of the voltage loop parameters x_p and x_i , which both are modified when the bus voltage and current change. Therefore, the proposed control system always ensures the same desired performance for any operating condition, which is the main objective of the proposed control system.

4. Conclusions

DC MGs are a suitable approach to connect loads, renewable sources, and storage devices to produce electric energy. Loads, sources, and storages devices can be interconnected through power converters that can be used to guarantee a safe operation of the elements and consequently for the entire MG. A formal design of a battery charging/discharging solution based on a flyback converter and two adaptive control loops were proposed in this paper to protect the devices of a DC MG. The design was dominated by a formal procedure that modeled the system and establish three performance criteria to be guaranteed by the controllers: a maximum settling time, a maximum voltage deviation, and a maximum angular frequency. The PI structures are adaptive to changes in the operating point, even for changes in the converter parameters. To encourage the interested community to implement the battery charging solution, a detailed design flowchart was presented. In addition, several recommendations were made to select the hardware that can be used in the implementation of the battery charger and its controllers. Hence, this paper provides three main contributions: (1) an adaptive linear controller that guarantees the system stability and the desired dynamic behavior for any operating condition; (2) a step-by-step design procedure to determine the controller parameters considering the system stability; and (3) a

charging/discharging based on a flyback converter with an adaptive linear controller that operates at a fixed switching frequency.

Finally, a practical example simulated in PSIM software confirmed the correct operation of the adaptive current loop and the adaptive voltage loop. The simulation results showed that bus voltage fulfilled the performance criteria defined in the case ($t_s = 1 \text{ ms}$, MD = 5%, and $w_c \leq F/25$). However, additional verifications, using real hardware, will be performed in the future to test the proposed control system under commercial conditions.

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