computation

MDPI

Article

Co-Design of the Control and Power Stages of a Boost-Based Rectifier with Power Factor Correction Depending on Performance Criteria

Carlos Andres Ramos-Paja [1,*,†], Andres Julian Saavedra-Montes [1,†] and Juan David Bastidas-Rodriguez [2,†]

[1] Facultad de Minas, Universidad Nacional de Colombia, Medellin 050013, Colombia; ajsaaved@unal.edu.co
[2] Facultad de Ingeniería y Arquitectura, Universidad Nacional de Colombia, Manizales 170003, Colombia; jubastidasr@unal.edu.co
* Correspondence: caramosp@unal.edu.co
† These authors contributed equally to this work.

Abstract: Rectifiers with power factor correction are key devices to supply DC loads from AC sources, guaranteeing a power factor close to one and low total harmonic distortion. Boost-based power factor correction rectifiers are the most widely used topology and they are formed by a power stage (diode bridge and Boost converter) and a control system. However, there is a relevant control problem, because controllers are designed with linearized models of the converters for a specific operating point; consequently, the required dynamic performance and stability of the whole system for different operating points are not guaranteed. Another weak and common practice is to design the power and control stages independently. This paper proposes a co-design procedure for both the power stage and the control system of a Boost-based PFC rectifier, which is focused on guaranteeing the system's stability in any operating conditions. Moreover, the design procedure assures a maximum switching frequency and the fulfillment of different design requirements for the output voltage: maximum overshoot and settling time before load disturbances, maximum ripple, and the desired damping ratio. The proposed control has a cascade structure, where the inner loop is a sliding-mode controller (SMC) to track the inductor current reference, and the outer loop is an adaptive PI regulator of the output voltage, which manipulates the amplitude of the inductor current reference. The paper includes the stability analysis of the SMC, the design procedure of the inductor to guarantee the system stability, and the design of the adaptive PI controller parameters and the capacitor to achieve the desired dynamic performance of the output voltage. The proposed rectifier is simulated in PSIM and the results validate the co-design procedures and show that the proposed system is stable for any operating conditions and satisfies the design requirements.

Keywords: sliding-mode control; active rectifier; harmonic distortion; power factor; adaptive control

Citation: Ramos-Paja, C.A.; Saavedra-Montes, A.J.; Bastidas-Rodriguez, J.D. Co-Design of the Control and Power Stages of a Boost-Based Rectifier with Power Factor Correction Depending on Performance Criteria. *Computation* **2022**, *10*, 61. https://doi.org/10.3390/computation10040061

Academic Editor: Demos T. Tsahalis

Received: 23 February 2022
Accepted: 1 April 2022
Published: 11 April 2022

1. Introduction

Rectifiers, or AC/DC converters, are essential electronic devices to feed DC loads from AC sources. In fact, most of the DC loads used in residential or industrial applications include rectifiers to generate the required DC voltage from the grid. Typical rectifiers are constructed with a diode or thyristor bridge and a capacitor to generate an approximately constant voltage to supply the power required by the load. Although those rectifiers are simple and low cost, they produce large distortions in the current provided by the AC source, since a typical rectifier, even with an ideal resistor as load, is a highly nonlinear load from the AC source point of view [1,2]. Those nonlinear loads are translated into a significant increment of the Total Harmonic Distortion (THD) of the AC sources, they negatively affect the load power factor (PF), produce imbalances in the three-phase systems, and, as consequence, it is not possible to utilize the full energy potential from the grid nor meet power quality standards such as IEC 61000-2-3 [3] and IEEE 519 [4].

One option to supply a DC load from an AC source with low-input current distortions (i.e., low THD) and PF close to one are the rectifiers with active power factor correction (PFC), which are usually formed by a diode bridge, a DC/DC power converter, and a control system [1,2]. Even if those devices introduce higher system complexity and higher costs, regarding traditional rectifiers, the joint operation of the DC/DC converter and the control system can cause the rectifier to behave as a resistive load from the AC source perspective. Hence, the PF is close to one, the THD is significantly improved, and there is a reduction in the three-phase system imbalances; all of this allows the increment of the power drawn from the grid. Additionally, these devices can be used for different power levels and allow the compliance of power quality standards [1,2].

PFC rectifiers can be implemented with different DC/DC converter topologies such as Boost, Buck [5], Buck-Boost [6], Cuk [7], Sepic [8], and Flyback [9], among others. However, Boost-based PFC rectifiers are the most widely adopted topology in the literature, since the Boost converter provides continuous input current, requires few elements (i.e., low cost), has a simple model, and has a simpler analysis and control design than Cuk- and SEPIC-based rectifiers [1,2]. Additionally, Boost converters are also extensively used in a high variety of applications, from motor drives [10] to microgrids [11]. Therefore, this paper considers a Boost-based PFC rectifier to propose a co-design procedure for both converter and control strategy.

In Boost-based PFC, the control problem is to regulate the DC output voltage (v_{dc}) to a constant reference (v_r) with zero steady-state error considering a time-varying input voltage ($v_{in} = v_{pk} \cdot |\sin(w \cdot t)|$) as well as perturbations in the DC load current (i_{dc}) and the peak input voltage (v_{pk}): where v_{in} is the input voltage, w is the angular frequency, and t is the time. Table 1 summarizes the main perturbations and their main causes and effects on v_{dc}. Although the typical control structure for widely used power converters, such as Buck and Boost, is aimed at regulating their output voltage with a single loop [12,13], the most common structure to tackle this control problem is a cascade controller, where the outer loop regulates the DC output voltage (v_{dc}) to a constant reference (v_r) by modifying the amplitude of the inductor current reference (i_r), while the inner loop tracks i_r acting on the Boost switch [1]. Moreover, i_r must be in phase with the converter input voltage (v_{in}), which corresponds to the output of the diode bridge, i.e., $v_{in} = v_{pk} \cdot |\sin(w \cdot t)|$; hence, i_r is defined as $i_r = i_{pk} \cdot |\sin(w \cdot t)|$, where w is the angular frequency of the AC source.

Table 1. PFC main perturbations, causes and effects.

Perturbation	Main Cause	Main Effect
Change in i_{dc}	Connection/disconnection of loads	Reduction/increment in v_{dc}
Change in v_{pk}	Sag/swell in grid voltage	Reduction/increment in v_{dc}

The outer loop is typically implemented with a PI controller, either with analog [1,14–17] or digital circuitry [18–20], since it rejects load perturbations, it provides zero steady-state error, and its parameters can be tuned by frequency response [16,19]. Moreover, the PFC system regulated by a PI controller is relatively simple because the inner loop deals with the system nonlinearities and the time-varying reference. Nevertheless, in many cases the design procedure of the PI controller of the outer loop is not provided [14,15,18,20] or it is not clearly explained [16,17,19].

The inner loop can be implemented with linear or nonlinear controllers to track i_r. Linear controllers such as P [19] and PI [17] are commonly used to track i_r in PFC rectifiers. These controllers are simple, can be implemented with analog circuits or microcontrollers, and can be tuned with different methods, such as frequency response [17,19]. However, in many works, the authors do not provide a clear design method for the linear controllers [16,17,19], and those controllers are designed and tuned with linearized models of the DC/DC converter in a particular operating point; therefore, they cannot guarantee the desired dynamic performance for different loads, and the system stability may be compromised under particular operating conditions. Moreover, other works, such as the

one reported in [21], use feedforward compensators to improve the dynamic response of the system. That work is based on two control loops (inner current loop and outer voltage loop), which have two adaptive gains calculated to compensate changes on the grid voltage and load current. However, that paper only considers resistive loads in its analysis and the adaptive gains have a calculation delay imposed by a peak detector, which needs half of the grid cycle to update their values. That is why sliding-mode controllers (SMC) are an interesting option for controlling Boost converters [13], since they take advantage of the converter variable structure imposed by the switch, and those controllers provide fast dynamic responses.

The authors of [18,20] propose a cascade controller for a Boost-based PFC where the outer loop is a digital PI to regulate v_{dc} and the inner loop is an SMC to track i_r. Although in both papers the switching function is defined as $\Psi = i_L - i_r$ (where i_L is the inductor current), the authors of [18] propose a method to implement the hysteresis band on a microcontroller, while [20] uses the equivalent control analysis to calculate the converter duty cycle to generate a PWM that acts on the switch. Moreover, [20] proposes an additional loop to regulate the converter switching frequency to a desired value by modifying the hysteresis band. However, these papers do not provide a design procedure of the PI parameters and [18] do not include the stability analysis. Furthermore, the SMC proposed in [18] generates a duty cycle and not the converter switching signal, which reduces the speed of the system dynamic response.

In [15,22], the authors propose an SMC to track i_r where the switching function has the following form: $\Psi = k_1 \cdot (i_L - i_r) + k_2 \cdot (v_{dc} - v_r)$. The authors of [15] do not perform the stability analysis nor provide a design procedure for k_1 and k_2; but they use a PI as outer loop to regulate v_{dc} (by modifying i_r) and to guarantee zero steady-state error. While in [22] the authors perform the stability analysis of the controlled system, they propose an expression to determine the hysteresis band to assure a maximum switching frequency, and they determine the SMC parameters (k_1 and k_2) by using a genetic algorithm. Unfortunately, the control structure proposed in [22] does not include an outer loop to regulate v_{dc}, which results in steady-state error in v_{dc}; in addition, the optimization problem to determine k_1 and k_2 is not clearly explained.

Other works use SMC theory to propose complex controllers to track i_r by generating the duty cycle of the Boost converter [14,23–25]. In [23], the authors propose an SMC observer for i_L and v_{dc}, and combine this observer with a triangular signal to generate a PWM with a fixed frequency. The proposed control system has four parameters: two for the SMC observer and two to define the triangular signal. Although the work [23] includes a Lyapunov-based stability analysis and defines conditions to guarantee the stability, it does not provide a methodology to design the four controller parameters and it does not regulate v_{dc}, since no outer loop is implemented.

Moreover, the works presented in [14,24,25] use complex switching functions to implement the SMCs. In [14,24], the proposed switching functions include the inductor current error as well as its first [14] and the second integrals [24]; while in [25], the switching function considers the inductor current and output voltage errors along with their integrals. On the one hand, the advantages of the work introduced in [14] are: it combines two switching functions to provide robustness to uncertainties in the inductor resistance and inductance; it performs a Lyapunov-based stability analysis; and the controller includes a PI to regulate v_{dc} and to provide zero steady-state error. However, one of the switching functions is not clearly defined and there is no design procedure for the PI parameters. On the other hand, the advantages of the work presented in [24] are: it provides a design procedure for the SMC parameters (based on frequency response); it performs the stability analysis using sliding-mode theory; and the SMC is implemented with a commercial PFC controller (integrated circuit). However, the controller does not include an outer loop to regulate v_{dc} (i.e., v_{dc} has a steady-state error), the SMC implementation with the commercial PFC integrated circuit is not clearly justified, and the experimental results show high ripples in i_L.

Additionally, one of the advantages of the controller proposed in [25] is that inductor-current SMC includes the output voltage error in the switching function to improve the dynamic response and robustness of v_{dc}, which is regulated by a PI. The other advantage is that the paper includes the stability analysis of the system and the inequalities to be considered for the design of the three switching function constants. Nevertheless, there is not a detailed design procedure for the SMC parameters to facilitate its implementation in other converters, it requires an additional sensor to measure the output capacitor current, and considers a resistive load. Further, similar to the SMC-based controllers introduced in [14,23–25], the SMC generates a PWM signal and not the converter-switching signal, which reduces the speed of the converter dynamic response.

Finally, the controller proposed in [26] combines the SMC and fuzzy logic control (FLC) to track the inductor current reference generated by a PI regulator of the output voltage. The SMC is used to generate one component of the duty cycle (or the equivalent control signal u_{eq}) considering a simple sliding surface ($\Psi = i_L - i_r$), while the FLC uses the signal $S = (i_L - i_r) - d(i_L - i_r)/dt$ to generate a second component of the duty cycle (u_s). Then, u_{eq} and u_s are combined to generate the converter duty cycle. Even though the authors validate the proposed approach with experimental results, they do not perform any stability analysis of the system nor a design procedure of the proposed controllers. Moreover, they do not provide information on the PI regulator of v_{dc} and the SMC is not used to generate the converter switching signal.

From the papers discussed before, it is possible to identify two main points: the first one is the lack of a joint design procedure (or co-design) of the converter's and controller's parameters considering the system stability, and the second one is the lack of a solution for the open-loop condition when $i_L = 0\,[A]$. Regarding the first point, only [16] provides expressions to determine the converter's inductor and capacitor, while [27] merely introduces an expression to define the capacitor; nevertheless, those expressions are independent of the control structure and they do not consider the system stability. Regarding the second point, in [23,24], the authors determine the region (in radians) where the system is "out-of-control" [23] or the time interval where the system is in open-loop [24]; however, these works do not propose any solution to guarantee the system stability when i_L is close to zero.

Therefore, this paper proposes a co-design procedure of the control system (inner and outer loops) and the converter for a Boost-based PFC to guarantee global stability of the system even close to $i_L = 0\,[A]$. The proposed controller assures a PF close to one as well as v_{dc} regulation with the desired ripple and settling time before nonlinear load perturbations. The inner loop tracks i_r and it is implemented with an SMC using a simple switching function $\Psi = i_L - i_r$, while the outer loop regulates v_{dc} with an adaptive PI controller. Hence, this paper has three main contributions: (1) a cascade controller that guarantees the global stability of the system for any operating condition and considering nonlinear loads, (2) a detailed co-design procedure of the converter (L and C) and controller parameters (k_p and k_i) to ensure the system stability and the desired dynamic response (settling time, maximum overshoot, and v_{dc} ripple), (3) a solution for the open-loop condition when $i_L = 0\,[A]$ as well as a detailed analysis of the ripples in v_{dc} produced by the time-varying input voltage.

The rest of the paper begins with Section 2, which includes all the details of the proposed approach including the mathematical model of the system, the design of the proposed cascade controller, the design of the inductor, and the design of the capacitor. Then, Section 3 shows the validation of the proposed approach with detailed simulation results, and Section 4 closes the paper with the discussion.

2. Materials and Methods

This section describes the proposed co-design procedure of the converter and the control system for a Boost-based rectifier with PFC. This section is divided into six subsections, where the first one (Section 2.1) introduces a control-oriented model of the system including

the Boost converter and a generic load. Then, Section 2.2 presents the SMC controller of the i_L along with the validation of the stability conditions (transversality, reachability, and equivalent control) and its practical implementation. Later, Section 2.3 shows the inductor design procedure to guarantee global stability in the SMC. Next, Section 2.4 introduces the design of the v_{dc} controller and the capacitor to meet the desired dynamic response and guarantee the system stability; while Section 2.5 presents an analysis of the ripples in v_{dc} introduced by v_{in}. Finally, Section 2.6 summarizes the complete co-design procedure to facilitate its implementation.

2.1. Circuital and Mathematical Models

The simplified scheme of the Boost-based rectifier with power factor correction is reported in Figure 1, where the inductor current i_L of the boost converter must be regulated to be in-phase with the input voltage v_{in} of the converter, i.e., the output voltage of the diode–bridge rectifier. Moreover, the electrical scheme also shows the nonlinear load modeled using a current source i_o; such a model provides higher generality to the system design in comparison with resistive models usually adopted in literature to represents loads, since the current source is a suitable model to represent the power converters commonly present at the input of commercial DC loads [28,29].

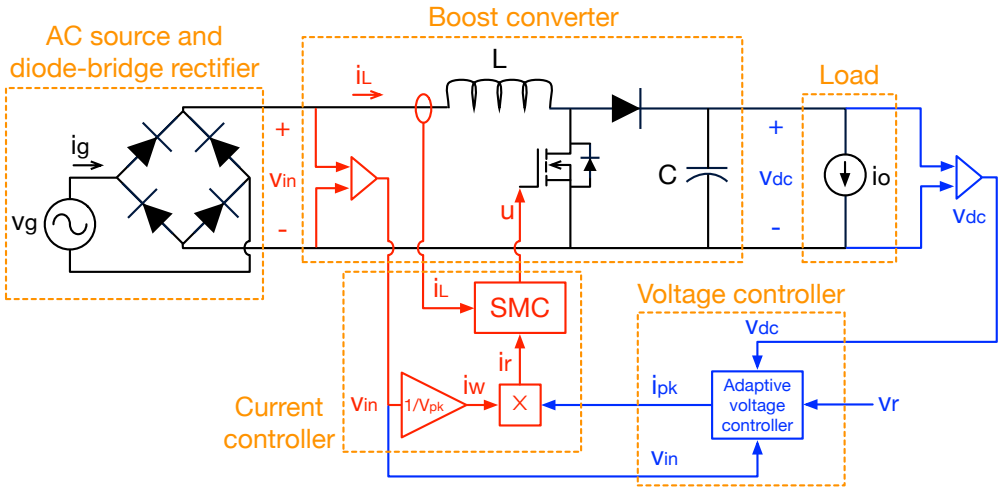

Figure 1. Electrical scheme of the Boost-based rectifier with power factor correction.

The scheme of Figure 1 reports the current controller in red color, which is based on a sliding-mode controller (SMC) and a multiplier. Such a control system measures the v_{in} waveform, which is applied to the current reference i_r of the SMC, using i_w, to ensure the inductor current i_L is in-phase with the input voltage v_{in}, thus ensuring a high power factor (PF) [1]. The peak value i_{pk} of the current reference is defined by the voltage controller, which is depicted in blue. Such a voltage controller must be designed using an adaptive strategy to provide the same performance for any operating condition imposed by the load, i.e., for different power and current requested by the load.

The switched differential equations describing the boost converter operation are given in (1) and (2), where u represents the activation signal of the MOSFET.

$$\frac{di_L}{dt} = \frac{v_{in} - v_{dc} \cdot (1-u)}{L} \tag{1}$$

$$\frac{dv_{dc}}{dt} = \frac{i_L \cdot (1-u) - i_o}{C} \tag{2}$$

The averaged value of u within the switching period T_{sw} corresponds to the duty cycle of the converter, i.e., $d = (1/T_{sw}) \cdot \int_0^{T_{sw}} u \, dt$, hence, the averaged model of the converter is the following one:

$$\frac{di_L}{dt} = \frac{v_{in} - v_{dc} \cdot (1-d)}{L} \tag{3}$$

$$\frac{dv_{dc}}{dt} = \frac{i_L \cdot (1-d) - i_o}{C} \tag{4}$$

Finally, the steady-state relations of the converter are obtained from (3) and (4) by considering the differential equations equal to 0, which lead to:

$$1 - d = \frac{v_{in}}{v_{dc}} = \frac{i_o}{i_L} \tag{5}$$

2.2. Current Controller

The current controller is designed using the sliding-mode theory, hence it corresponds to an SMC. The sliding-mode theory is adopted since it provides robustness to parametric changes [30,31], which is useful to overcome aging or tolerance effects. Moreover, the SMC provides a binary output, which matches the binary nature of the control signal u needed to activate or deactivate the MOSFETs of the DC/DC converter.

The proposed SMC is based on the sliding-surface Φ reported in (6), where Ψ (7) is the switching function defining the surface. The operation of the system into that surface Φ forces the inductor current i_L to follow the reference i_r. In that way, it is possible to impose a sinusoidal waveform into i_L to ensure the desired power factor for the rectifier.

$$\Phi = \{\Psi = 0\} \tag{6}$$

$$\Psi = i_L - i_r \tag{7}$$

The analysis of the SMC stability is based on three tests: the transversality condition, the reachability conditions, and the equivalent control [32,33].

2.2.1. Transversality Condition

The transversality condition evaluates the ability of the controller to modify the system trajectory. Therefore, the control signal u must be present into the trajectory derivative. This is formalized as follows:

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) \neq 0 \tag{8}$$

The previous condition is fulfilled when the control signal u is present into the derivative of the switching function Ψ. Therefore, the first step of this analysis is to obtain the switching function derivative as follows:

$$\frac{d\Psi}{dt} = \frac{di_L}{dt} - \frac{di_r}{dt} \tag{9}$$

Replacing the switching expression of $\frac{di_L}{dt}$ given in (1) into (9) leads to:

$$\frac{d\Psi}{dt} = \frac{v_{in} - v_{dc} \cdot (1-u)}{L} - \frac{di_r}{dt} \tag{10}$$

Finally, replacing expression (10) into (8) provides the final transversality proof given in (11), which is always different from zero since v_{dc} and L are positive values. Therefore, it is confirmed that the SMC based on (7) and (6) is feasible.

$$\frac{d}{du}\left(\frac{d\Psi}{dt}\right) = \frac{v_{dc}}{L} > 0 \tag{11}$$

2.2.2. Reachability Conditions

The reachability conditions test the ability of the SMC to drive the system to the surface and keep operating inside that desired surface. The reachability conditions are the following ones [32,33]:

- When the system (Ψ) is operating under the surface ($\Psi < 0$), the derivative of the switching function must be **positive** to reach the surface:

$$\lim_{\Psi \to 0^-} \frac{d\Psi}{dt} > 0 \tag{12}$$

- When the system (Ψ) is operating above the surface ($\Psi > 0$), the derivative of the switching function must be **negative** to reach the surface:

$$\lim_{\Psi \to 0^+} \frac{d\Psi}{dt} < 0 \tag{13}$$

However, the transversality sign also impacts the test of the reachability conditions: a positive transversality sign implies that positive changes on the control signal u produce **positive** switching function derivatives ($\frac{d\Psi}{dt} > 0$); on the contrary, a negative transversality sign implies that positive changes on the control signal u produce **negative** switching function derivatives ($\frac{d\Psi}{dt} < 0$). Taking into account that the transversality sign is always positive (11), the reachability conditions that must be tested for this case are:

$$\lim_{\Psi \to 0^-} \left.\frac{d\Psi}{dt}\right|_{u=1} > 0 \tag{14}$$

$$\lim_{\Psi \to 0^+} \left.\frac{d\Psi}{dt}\right|_{u=0} < 0 \tag{15}$$

Replacing the explicit equation for the switching function derivative (10) into both reachability conditions gives:

$$\frac{v_{in} - v_{dc}}{L} < \frac{di_r}{dt} < \frac{v_{in}}{L} \tag{16}$$

The previous expressions provide the conditions on $\frac{di_r}{dt}$ and L that must be fulfilled to ensure the reachability conditions, which also guarantee the controller stability. In Section 2.3, the expression for $\frac{di_r}{dt}$ will be analyzed to calculate a design equation for L, which guarantees that the reachability conditions are always fulfilled.

2.2.3. Equivalent Control Condition

In DC/DC converter applications, the equivalent control condition evaluates the saturation of the duty cycle d [32]. In general, the equivalent control condition is the following one: the averaged value of the control signal u must be always constrained by the possible values of that signal. In DC/DC converters, the possible values of u are 1 (MOSFET closed) and 0 (MOSFET open); moreover, the averaged value of u corresponds to the converter' duty cycle d. Therefore, when the equivalent control condition is fulfilled, the DC/DC converter operates with a duty cycle inside the physical limits ($0 < d < 1$) to avoid instability caused by duty cycle saturation.

Since the reachability conditions ensures that the SMC drives the system to the sliding-surface, the equivalent control condition is evaluated inside the surface:

$$\Psi = 0 \quad \wedge \quad \frac{d\Psi}{dt} = 0 \tag{17}$$

The first step of this test is to obtain the expression for the control signal u when the system is operating inside the sliding surface:

$$u = 1 - \frac{v_{in} - L \cdot \frac{di_{ir}}{dt}}{v_{dc}} \tag{18}$$

Then, such an expression is averaged as $d = (1/T_{sw}) \cdot \int_0^{T_{sw}} u \, dt$, and the result is constrained into $0 < d < 1$, which results in the same expression previously reported in (16). Therefore, this test confirms that fulfilling the condition given in (16) also ensures the equivalent control condition, i.e., the duty cycle is not saturated.

Finally, the three tests confirm that the proposed SMC is stable when condition (16) is fulfilled; hence, the inductor current i_L follows the reference value i_r.

2.2.4. Practical Implementation

The proposed SMC requires a control law to be implemented. Such a control law is extracted from the reachability conditions: from (14) it is observed that the control signal must be set to $u = 1$ when $\Psi < 0$, while (15) indicates that $u = 0$ when $\Psi > 0$. However, theoretical sliding-mode controllers require infinite switching frequency F_{sw}, which is impossible to implement [32]. Therefore, SMCs are traditionally implemented using an hysteresis band $\pm\Delta\Psi$ around the sliding surface to limit the switching frequency:

$$\{\Psi = 0\} \quad \rightarrow \quad \{|\Psi| \leq \Delta\Psi\} \tag{19}$$

The previous hysteresis band requires the following practical control law, which is an extension of the theoretical control law extracted from the reachability conditions:

$$u = \begin{cases} 1 & \text{if} \quad \Psi < -\Delta\Psi \\ 0 & \text{if} \quad \Psi > +\Delta\Psi \end{cases} \tag{20}$$

The current reference i_r changes at the grid frequency, which is much smaller than the switching frequency (60 Hz vs. 250–300 kHz). Therefore, with a switching period T_{sw} (less than 5 µs) the changes on i_r are almost negligible; hence, the hysteresis limit $\Delta\Psi$ is equal to the inductor current ripple Δi_L. Such a relation is obtained from (7) as follows:

$$\Delta\Psi = \Delta i_L \text{ because } \Delta i_r \approx 0 \text{ within } T_{sw} \tag{21}$$

From Equation (1), the inductor current ripple is calculated as given in (22), which leads to the switching frequency expression given in (23).

$$\Delta i_L = \frac{v_{in} \cdot d \cdot T_{sw}}{2 \cdot L} = \Delta\Psi \tag{22}$$

$$F_{sw} = \frac{v_{in} \cdot d}{2 \cdot L \cdot \Delta\Psi} \tag{23}$$

Figure 2 illustrates the effect of the hysteresis band on the switching frequency, where the Ψ waveform is constrained within $[-\Delta\Psi, +\Delta\Psi]$. The figure at the top shows that reducing $\Delta\Psi$ increases F_{sw}, this because the Ψ waveform requires a shorter time to complete a period (higher F_{sw}), which is in agreement with Equation (23).

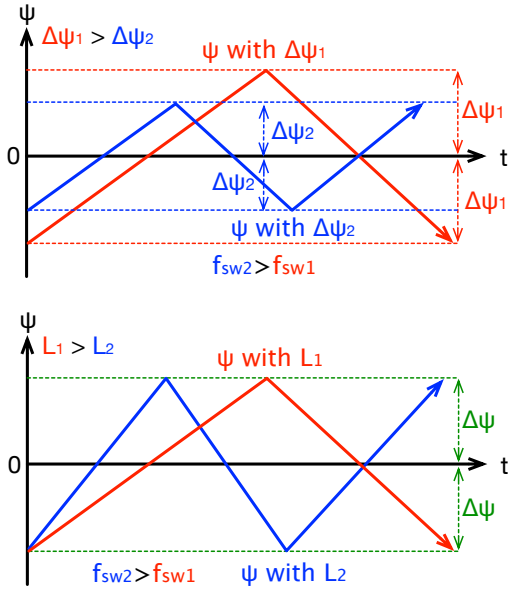

Figure 2. Ψ waveform for different values of $\Delta\Psi$ and L.

Similarly, the bottom traces of Figure 2 shows the effect of the inductance L in the switching frequency: reducing L increases the derivative of the inductor current, as given in (1); hence, the Ψ waveform takes a shorter time to reach the hysteresis band (higher F_{sw}), which is also in agreement with Equation (23).

Finally, the switching function Ψ must be always inside the hysteresis band $[-\Delta\Psi, +\Delta\Psi]$ to ensure that the inductor current i_L follows the reference value i_r. Otherwise, when Ψ is outside $[-\Delta\Psi, +\Delta\Psi]$ the inductor current is not regulated; consequently, the power factor correction is not ensured. Therefore, both L and $\Delta\Psi$ values must be carefully designed.

2.2.5. SMC Circuit

The circuital implementation of the SMC is performed using the control law previously defined in (20). Such an implementation uses two traditional comparators to test the inequalities of the control law, and a flip-flop S-R is used to set the control signal u according to (20): SET (S) = 1 imposes the output Q (u) = 1; while RESET (R) = 1 imposes Q (u) = 0. Finally, the switching function Ψ is calculated using a subtractor as given in (7). Figure 3 summarizes the circuital implementation of the SMC, which is commonly constructed using operational amplifiers and a TS555-integrated circuit [34,35].

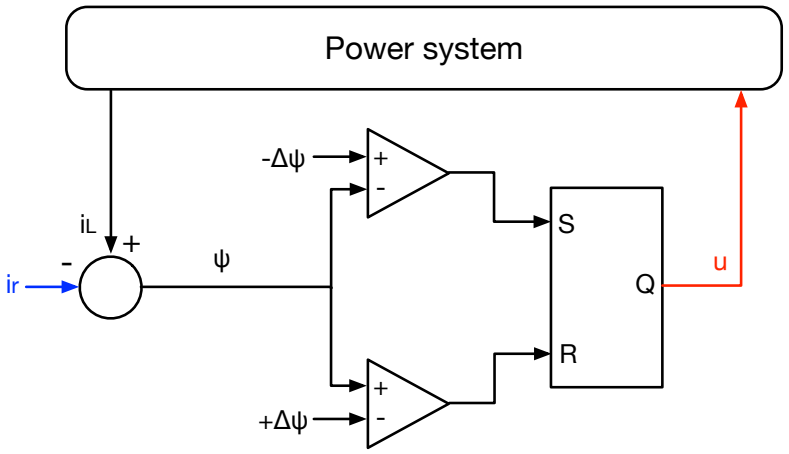

Figure 3. Circuital implementation of the SMC.

2.3. Design of the Inductor to Guarantee Global Stability

The inductor L must be designed to ensure that the reachability conditions (16) are fulfilled, otherwise the global stability of the SMC will not be guaranteed. From Figure 1, it is observed that i_r must have the same waveform (frequency and phase) that the input voltage v_{in} to ensure a unitary power factor, but the peak value i_{pk} of the current reference is defined by the voltage controller to regulate the DC voltage as $v_{dc} = v_r$.

The input voltage of the converter, i.e., the output voltage of the diode rectifier, has a waveform defined in (24), where v_{pk} is the peak value of the voltage and f_g is the grid frequency ($T_g = 1/f_g$) is the period of the grid). Therefore, in general, the current reference has the form given in (25), where i_{pk} is the peak current.

$$v_{in} = v_{pk} \cdot \sin\left(2 \cdot \pi \cdot f_g \cdot t\right) \text{ for } 0 \leq t \leq T_g/2 \tag{24}$$

$$i_r = i_{pk} \cdot \sin\left(2 \cdot \pi \cdot f_g \cdot t\right) \text{ for } 0 \leq t \leq T_g/2 \tag{25}$$

To evaluate the conditions in (16) it is necessary to calculate the expression for the derivative of i_r:

$$\frac{di_r}{dt} = 2 \cdot i_{pk} \cdot \pi \cdot f_g \cdot \cos\left(2 \cdot \pi \cdot f_g \cdot t\right) \tag{26}$$

The previous expressions will be analyzed in the interval $0 \leq t \leq T_g/2$, since those signals have the same values in the interval $T_g/2 \leq t \leq T_g$ due to the action of the diode bridge rectifier. Replacing expressions (24) and (26) into (16) leads to:

$$\frac{v_{pk} \cdot \sin\left(2 \cdot \pi \cdot f_g \cdot t\right) - v_{dc}}{L} < 2 \cdot i_{pk} \cdot \pi \cdot f_g \cdot \cos\left(2 \cdot \pi \cdot f_g \cdot t\right) \tag{27}$$

$$2 \cdot i_{pk} \cdot \pi \cdot f_g \cdot \cos\left(2 \cdot \pi \cdot f_g \cdot t\right) < \frac{v_{pk} \cdot \sin\left(2 \cdot \pi \cdot f_g \cdot t\right)}{L} \tag{28}$$

Taking into account that the boost converter requires an input voltage smaller than the output voltage, i.e., $v_{in} < v_{dc}$, condition (27) is fulfilled since the left term is always negative and the right term is positive in the analysis interval. In contrast, condition (28) could not be fulfilled when the right side of the expression becomes very small, which occurs when the input voltage v_{in} and grid voltage v_g are near to zero. Therefore, such a condition must be analyzed in detail: it is observed that expression (28) corresponds to the reachability condition given in (14), where the switching function derivative has the following form:

$$\left.\frac{d\Psi}{dt}\right|_{u=1} = \frac{v_{pk} \cdot \sin\left(2 \cdot \pi \cdot f_g \cdot t\right)}{L} - 2 \cdot i_{pk} \cdot \pi \cdot f_g \cdot \cos\left(2 \cdot \pi \cdot f_g \cdot t\right) \tag{29}$$

Then, the explicit expression for the changes of Ψ is obtained by integrating Equation (29), as follows:

$$\Psi = -\left[\frac{v_{pk}}{2 \cdot \pi \cdot f_g \cdot L} \cos\left(2 \cdot \pi \cdot f_g \cdot t\right) + i_{pk} \cdot \sin\left(2 \cdot \pi \cdot f_g \cdot t\right)\right] \tag{30}$$

The maximum amplitude of Ψ when expression (28) is not fulfilled (v_{in} near to zero) occurs at $\left.\frac{d\Psi}{dt}\right|_{u=1} = 0$; then, the time $t = T_x$ when such a condition occurs is evaluated from expression (29):

$$T_x = \frac{T_g}{2 \cdot \pi} \cdot \arctan\left(\frac{2 \cdot \pi \cdot f_g \cdot L \cdot i_{pk}}{v_{pk}}\right) \tag{31}$$

Such a maximum amplitude of Ψ is calculated by evaluating Equation (30) for $t = T_x$:

$$\max(|\Psi|) = \left(\frac{v_{pk}}{2 \cdot \pi \cdot f_g \cdot L}\right)\left[-1 + \sqrt{1 + \left(\frac{2 \cdot \pi \cdot f_g \cdot L \cdot i_{pk}}{v_{pk}}\right)^2}\right] \text{ for } u = 1 \tag{32}$$

The previous section described that global stability is ensured when the maximum deviation of the switching function is always trapped inside the hysteresis band; therefore, the inductance L must be designed to ensure the following stability condition:

$$\max(|\Psi|) \leq \Delta\Psi \tag{33}$$

Figure 4 illustrates the waveform of Ψ when the system approaches $v_{in} \approx 0$, i.e., not fulfilling (28), for two values of L: with L_1 the stability condition (33) is not fulfilled, hence i_L does not follow closely the reference i_r during a section of the grid period, thus degrading the power factor; instead, with L_2 the stability condition (33) is always fulfilled, hence i_L follows closely i_r for all the grid period, thus providing a high power factor.

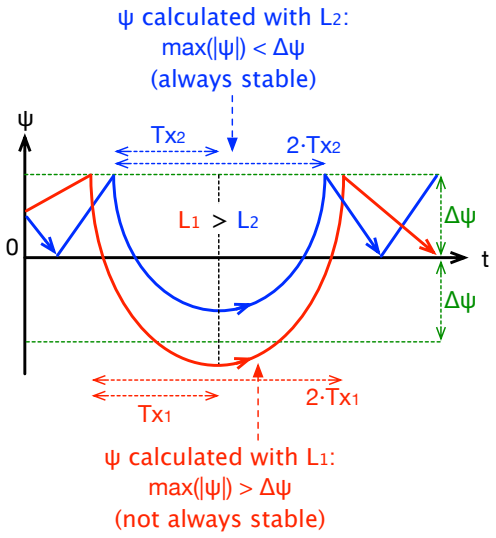

Figure 4. Detailed waveform of Ψ when $v_{in} \approx 0$ for different L values.

Figure 4 indicates that $L_1 > L_2$, which is confirmed by calculating the partial derivative of $\max(|\Psi|)$ with respect to L, as given in (34), which is always positive. Therefore, increasing L also increases $\max(|\Psi|)$.

$$\frac{\partial \max(|\Psi|)}{\partial L} = \left(\frac{v_{pk}}{2 \cdot \pi \cdot f_g \cdot L^2}\right)\left[1 - \frac{1}{\sqrt{1 + \left(\frac{2 \cdot \pi \cdot f_g \cdot L \cdot i_{pk}}{v_{pk}}\right)^2}}\right] > 0 \text{ for } u = 1 \tag{34}$$

Finally, operating (32) and (33), the inductance values that fulfill the reachability conditions are calculated using (16), ensuring global stability of the SMC even when v_{in} is near zero.

$$L \leq \frac{v_{pk} \cdot \Delta\Psi}{\pi \cdot f_g \left[i_{pk}^2 - (\Delta\Psi)^2\right]} \tag{35}$$

Figure 1 shows that i_{pk} is provided by the voltage controller; hence, the worst-case condition for i_{pk} is calculated in the following sections.

2.4. Voltage Controller and Capacitor Design

The voltage controller and bus capacitor must be designed to impose the average DC voltage v_{dc} required by the load. This process requires the converter behavior to be modeled under the action of the current controller. Therefore, the following section presents the equivalent dynamics of the current loop and the proposed voltage loop.

2.4.1. Equivalent Model of the Current and Voltage Loops

Taking into account that the current SMC is globally stable, the sliding surface (6) ensures that $i_L = i_r$. Therefore, the voltage differential Equation (4) of the averaged model is modified as given in (36), where $\langle v_{dc} \rangle$ is the averaged DC voltage at the converter output, and $\langle i_r \rangle$ represents the averaged value of the current reference. Finally, Equation (37) reports the Laplace representation of the averaged DC voltage $\langle v_{dc} \rangle(s)$ for changes on the average value of reference $\langle i_r \rangle(s)$ and the load current $i_o(s)$.

$$\frac{d\langle v_{dc} \rangle}{dt} = \frac{\langle i_r \rangle \cdot (1-d) - i_o}{C} \tag{36}$$

$$\langle v_{dc} \rangle(s) = \frac{\langle i_r \rangle(s) \cdot (1-d) - i_o(s)}{s \cdot C} \tag{37}$$

Figure 5 presents the voltage loop proposed to regulate the DC voltage. In such a figure the block G_V represents the voltage controller, which will be designed in the Laplace domain.

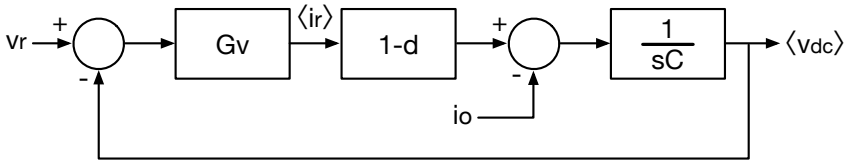

Figure 5. Voltage control loop.

The previous diagram enables to calculate the following closed-loop expression for the average DC voltage:

$$\langle v_{dc} \rangle(s) = \frac{G_V \cdot (1-d)}{s \cdot C + G_V \cdot (1-d)} \cdot v_r - \frac{1}{s \cdot C + G_V \cdot (1-d)} \cdot i_o(s) \tag{38}$$

2.4.2. Adaptive Controller Design

The proposed voltage controller is given in (39), which corresponds to a proportional-integral (PI) structure.

$$G_V = k_p + \frac{k_i}{s} \tag{39}$$

In these kinds of applications, the reference value is usually constant; hence, the changes on $\langle v_{dc} \rangle(s)$ are caused by perturbation on the load current $i_o(s)$. Therefore, the transfer function $G_{dc/o}(s)$ between $i_o(s)$ and $\langle v_{dc} \rangle(s)$ is calculated from (38) and (39) as given in (40).

$$G_{dc/o}(s) = \frac{\langle v_{dc} \rangle(s)}{i_o(s)} = \frac{-1}{s \cdot C + G_V \cdot (1-d)} = \frac{-\frac{s}{C}}{s^2 + \frac{(1-d)k_p}{C} s + \frac{(1-d)k_i}{C}} \tag{40}$$

The main problem of such a model concerns the dependency on the duty cycle d, which changes depending on the operating point as reported in (5); hence, the values of k_p and k_i will produce a different performance for different i_o. Therefore, this paper

proposes to adapt the k_p and k_i values depending on the operating point defined by d; this is performed by using the following normalized parameters x_p and x_i:

$$x_p = (1-d)k_p \quad \wedge \quad x_i = (1-d)k_i \tag{41}$$

Then, expression (40) is rewritten using x_p and x_i as follows:

$$G_{dc/o}(s) = \frac{-\frac{s}{C}}{s^2 + \frac{x_p}{C}s + \frac{x_i}{C}} \tag{42}$$

The objective is to calculate those x_p and x_i values to impose the desired performance in any operating conditions. The performance is defined by the following criteria:

- The reference v_r for the averaged DC voltage is constant.
- The load current i_o is the main perturbation for the average DC voltage. This design is performed for the worst-case scenario, which corresponds to a step change in the load current as given in (43), where I_o is the step size.

$$i_{o(s)} = \frac{I_o}{s} \tag{43}$$

- The maximum deviation allowed for the average DC voltage is MO_{dc}.
- The maximum settling time (2% criterion) for recovering the average DC voltage is t_s.
- The waveform of the average DC voltage must have a damping ratio ρ.

Considering the step function of the load current given in (43), the average DC voltage has the following Laplace representation, in which I_o is a scalar.

$$\langle v_{dc} \rangle(s) = \frac{-\frac{I_o}{C}}{s^2 + \frac{x_p}{C}s + \frac{x_i}{C}} \tag{44}$$

Taking into account that the canonical form of a second order system $\frac{\omega_n^2}{s^2+2\cdot\rho\cdot\omega_n\cdot s+\omega_n^2}$ has a settling time $t_{s,c} = -\frac{\ln(\epsilon)}{\rho\cdot\omega_n}$; then, the values of x_p and x_i to ensure a damping ratio ρ and a 2% settling time t_s to the average DC voltage are:

$$x_p = \frac{-2\cdot\ln(\epsilon)\cdot C}{t_s} \quad , \quad \epsilon = 0.02 \tag{45}$$

$$x_i = \left(\frac{-\ln(\epsilon)}{\rho\cdot t_s}\right)^2 \cdot C \tag{46}$$

From Figure 1, it is observed that the adaptive voltage controller must define only the peak current i_{pk} of the SMC reference i_r, since the current waveform i_w is a normalization of the input voltage (over the peak voltage v_{pk}) to ensure a high power factor. Therefore, such a peak current i_{pk} must ensure the average reference current $\langle i_r \rangle$ corresponds to the value defined by the G_V adaptive controller. This process requires the calculation of the average value of i_r from (25) as $\langle i_r \rangle = \frac{2\cdot i_{pk}}{\pi}$, which leads to the following peak value:

$$i_{pk} = \frac{\pi}{2}\cdot\langle i_r \rangle \tag{47}$$

Hence, the output of the G_V adaptive controller must be multiplied by $\frac{\pi}{2}$ to ensure the desired average current extracted from the diode bridge rectifier. Moreover, the x_p and x_i values must be denormalized in real-time, dividing them by $(1-d)$, which provides k_p and k_i parameters adapted to the operation condition. The structure of the adaptive voltage controller is summarized in Figure 6: the controller measures v_{dc} and v_i to calculate $(1-d)$, which is used to calculate the k_p and k_i parameters; moreover, the averaged value of the DC voltage ($\langle v_{dc} \rangle$) is calculated using a low-pass filter. Finally, the structure also

shows the construction of the SMC reference i_r from the normalized waveform i_w and the peak current i_{pk}.

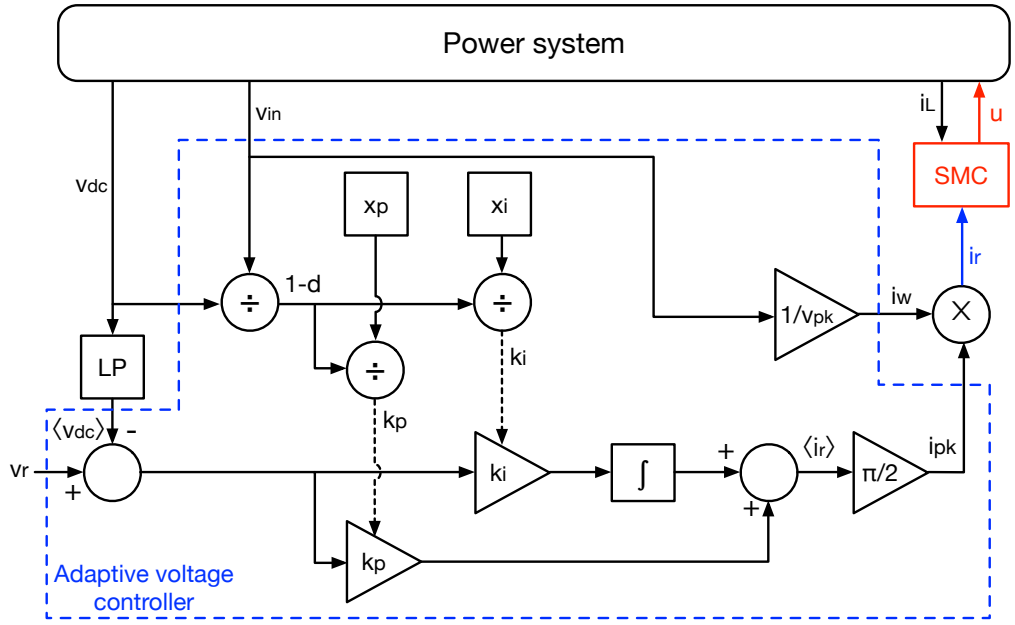

Figure 6. Structure of the adaptive voltage controller.

2.4.3. Capacitor Design to Ensure the Average Voltage Deviation MO_{dc}

Another important parameter to ensure the maximum deviation MO_{dc} of the averaged DC voltage is the capacitance C. The design of such a parameter is performed using the time-domain waveform $\langle v_{dc} \rangle(t)$ of the averaged DC voltage, given in (48), which is obtained from the inverse Laplace transformation of (44).

$$\langle v_{dc} \rangle(t) = \frac{-\frac{I_o}{C}}{\frac{x_p}{2 \cdot C}\sqrt{\frac{1}{\rho^2}-1}} \cdot \exp\left(-\frac{x_p}{2 \cdot C} \cdot t\right) \cdot \sin\left(\frac{x_p}{2 \cdot C}\sqrt{\frac{1}{\rho^2}-1} \cdot t\right) \tag{48}$$

The maximum deviation MO_{dc} occurs when the derivative of (48) is equal to zero, which is named time t_m and it is calculated in (49). Then, evaluating $\langle v_{dc} \rangle(t)$ in (48) for $t = t_m$ leads to the MO_{dc} expression reported in (50).

$$\frac{d\langle v_{dc} \rangle(t)}{dt} = 0 \quad \Rightarrow \quad t_m = \frac{\arctan\left(\sqrt{\frac{1}{\rho^2}-1}\right)}{\frac{x_p}{2 \cdot C}\sqrt{\frac{1}{\rho^2}-1}} \tag{49}$$

$$MO_{dc} = -\frac{2 \cdot I_o \cdot \rho}{x_p} \cdot \exp\left(-\frac{\arctan\left(\sqrt{\frac{1}{\rho^2}-1}\right)}{\sqrt{\frac{1}{\rho^2}-1}}\right) \tag{50}$$

Finally, replacing the x_p value given in (45) into (50) enables to calculate the capacitance values that ensures the limit value MO_{dc} is not violated:

$$C \geq \frac{I_o \cdot \rho \cdot t_s}{\ln(\epsilon) \cdot MO_{dc}} \cdot \exp\left(-\frac{\arctan\left(\sqrt{\frac{1}{\rho^2}-1}\right)}{\sqrt{\frac{1}{\rho^2}-1}}\right) \tag{51}$$

In conclusion, values of C higher than the limit defined in (51) will produce maximum deviations of the average DC voltage lower than the limit MO_{dc}.

2.5. Low-Frequency Ripple in the DC Voltage

The operation of any single-phase rectifier produces a low-frequency ripple at the DC output. This is caused by the capacitor current generated by the interaction between the ac current extracted from the grid and the DC current requested by the load. Figure 7 shows a simplified model of the converter output port, where the diode is modeled using a current source imposing an average rectified current.

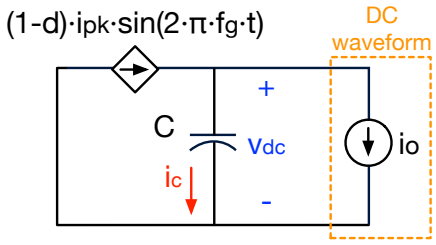

Figure 7. Output port model for analyzing the low-frequency voltage ripple at the DC side.

From the previous circuital scheme it is observed that the capacitor current is $i_C = (1-d)\cdot i_{pk}\cdot \sin(2\cdot\pi\cdot f_g\cdot t) - i_o$, and replacing the values of d and v_{in} given in (5) and (24) leads to the following expression:

$$i_C = \frac{v_{pk}\cdot i_{pk}}{v_{dc}}\cdot \sin^2(2\cdot\pi\cdot f_g\cdot t) - i_o \tag{52}$$

Stable DC voltage implies the capacitor fulfills the charge balance principle, i.e., the average capacitor current is zero in the complete grid period $[0, T_g]$; therefore, the steady-state relation between the load current i_o and the peak values is obtained as follows:

$$\frac{1}{T_g}\cdot\int_0^{T_g}\left\{\frac{v_{pk}\cdot i_{pk}}{v_{dc}}\cdot \sin^2(2\cdot\pi\cdot f_g\cdot t) - i_o\right\}dt = 0 \quad\rightarrow\quad i_o = \frac{v_{pk}\cdot i_{pk}}{2\cdot v_{dc}} \tag{53}$$

Then, replacing that i_o expression into (53) leads to the explicit expression of i_C given in (54). Figure 8 shows the waveform of i_C described by Equation (54). In addition, the capacitor voltage waveform v_{dc}, imposed by i_C, is given by $v_{dc} = \frac{1}{C}\cdot\int i_C\, dt$; moreover, the instants in which $i_C = \frac{dv_{dc}}{dt} = 0$ correspond to the maximum and minimum values of v_{dc}. Those instants are calculated by solving $i_C = 0$ as $t = \frac{T_g}{8}$ and $t = \frac{3\cdot T_g}{8}$, and those instants are depicted in Figure 8. Since i_C is a sinusoidal waveform centered in 0, i_C is only positive (or only negative) between the $i_C = 0$ points; in the example of Figure 8 i_C is positive; hence, v_{dc} is monotonically increased from the minimum value to the maximum value of the ripple.

$$i_C = \frac{v_{pk}\cdot i_{pk}}{v_{dc}}\cdot\left[\sin^2(2\cdot\pi\cdot f_g\cdot t) - \frac{1}{2}\right] \tag{54}$$

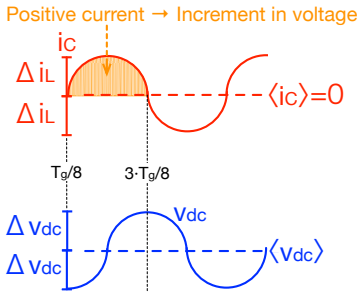

Figure 8. Low-frequency ripple waveforms at the DC side.

Taking into account that the average value $\langle v_{dc} \rangle$ of v_{dc} is at the center of the waveform, the voltage ripple is defined as $\pm\Delta v_{dc}$ around $\langle v_{dc} \rangle$. Therefore, $2 \cdot \Delta v_{dc} = \frac{1}{C} \cdot \int_{T_g/8}^{3 \cdot T_g/8} i_C \, dt$, which leads to the following ripple magnitude at the DC voltage:

$$\Delta v_{dc} = \frac{v_{pk} \cdot i_{pk}}{8 \cdot \pi \cdot f_g \cdot C \cdot v_{dc}} \tag{55}$$

Finally, expression (56) can be used to calculate the capacitor C to ensure a maximum ripple magnitude Δv_{dc}, where i_{pk} is replaced by the expression obtained in (53), where $I_{o,max}$ is the maximum steady-state value at the load current i_o.

$$C \geq \frac{I_{o,max}}{4 \cdot \pi \cdot f_g \cdot \Delta v_{dc}} \tag{56}$$

2.6. Design Procedure and Application Example

This section is focused on providing a synthesis of the design procedure, which is illustrated using an application example. Figure 9 shows a scheme of the application example, which considers an isolation transformer between the ac grid and the power system for protection purposes [36]. In this example the turn-ratio of the transformer is 2:1, but such a relation can be modified depending on the application requirements. The orange block (controlled boost converter) in Figure 9 corresponds to the device to be designed, which encloses the power stage and control loops detailed in Figure 1.

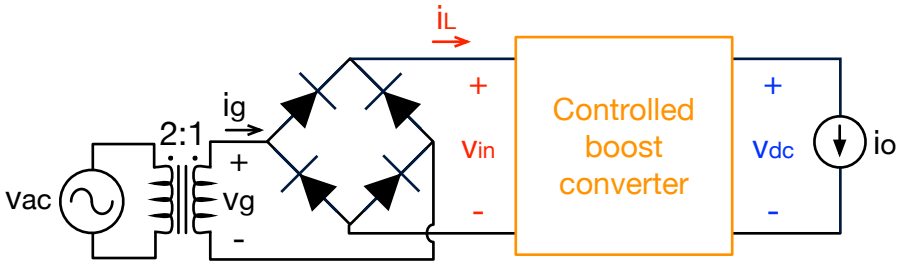

Figure 9. Scheme of the application example.

The grid voltage in this application is 120 VAC, hence, the peak voltage at the transformer secondary side is $v_{pk} = 84.85\ V$ and the grid frequency is f_g = 60 Hz. The required DC voltage for the load is v_{dc} = 220 V; such a load request has a maximum current $I_{o,max}$ = 2 A, including dynamic step-like changes with amplitudes I_o = 1 A. The maximum acceptable voltage ripple at the DC side, to ensure a correct load operation, is Δv_{dc} = 4 V. Similarly, the correct operation of the load requires a maximum deviation of the average voltage lower than $MO_{dc} = -10$ V with a 2% settling time shorter than $t_{s,2\%}$ = 100 ms. This application considers a damping ratio $\rho = 0.707$ to provide a trade-off between response time and oscillations, and the maximum switching frequency ($F_{sw,max}$) is set to F_{sw} = 300 kHz due to the limitations of average semiconductors. Table 2 summarizes the application parameters.

Table 2. Parameters for the application example.

Parameter	Value	Parameter	Value
v_{pk}	84.85 V	v_{dc}	220 V
f_g	60 Hz	$F_{sw,max}$	300 kHz
I_o	1 A	$I_{o,max}$	2 A
MO_{dc}	−10 V	Δv_{dc}	4 V
ρ	0.707	$t_{s,2\%}$	100 ms

2.6.1. Design of the Inductor and Hysteresis Band

The first step is to design the indictor L and hysteresis band $\Delta\Psi$ to ensure both global stability and maximum switching frequency. Those parameters are governed by Equations (23) and (35). The maximum F_{sw} value is obtained at the maximum value of v_{in}, which corresponds to v_{pk} and $d = v_{pk}/v_{dc} - 1$. Similarly, the i_{pk} value on the stability Equation (35) is calculated as given in (53) using $I_{o,max}$. Then, the system of equations formed by the parameterized versions of (23) and (35) is solved to establish the values fulfilling both maximum switching frequency and global stability, which can be done using any numerical method. Figure 10 shows the solution of such an equation system, where four zones are observed:

- **Left zone:** a zone where Equation (35) is fulfilled, thus the system is stable, but the switching frequency is higher than 300 kHz.
- **Right zone:** a zone where Equation (23) ensures $F_{sw} \leq 300$ kHz, but the system is unstable.
- **Bottom zone:** a zone where the system is unstable and $F_{sw} > 300$ kHz.
- **Top zone:** a zone where both global stability and and $F_{sw} \leq 300$ kHz are ensured.

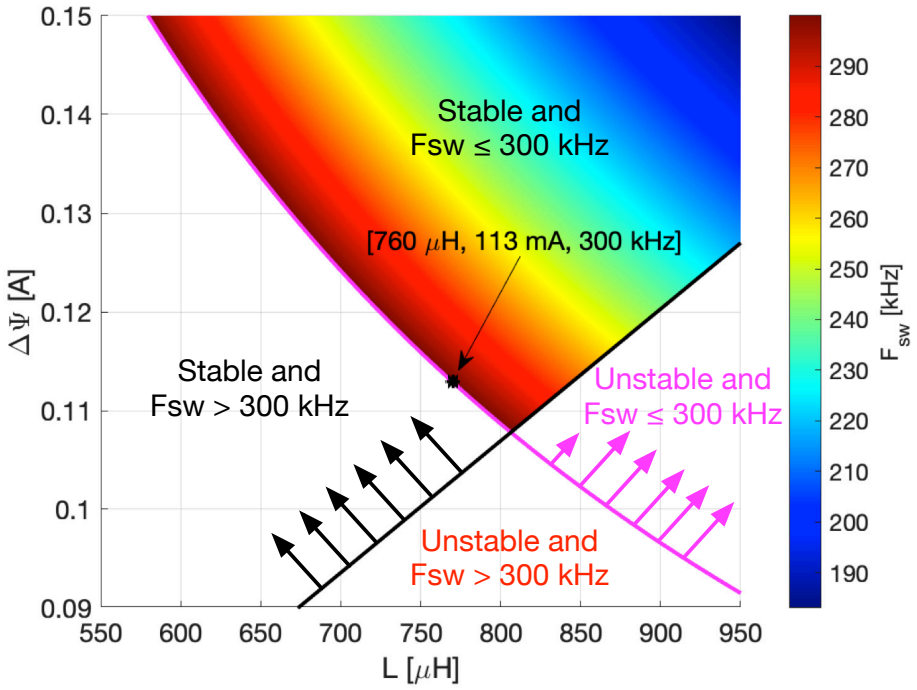

Figure 10. Design of the inductor L and hysteresis band $\Delta\Psi$.

Therefore, any point inside the Top zone is acceptable (global stability and $F_{sw} \leq 300$ kHz). For this application example, Figure 10 was constructed by defining two vectors (L_v and $\Delta\Psi_v$) of possible values of inductance (from 550 µH to 950 µH with steps of 1 µH) and $\Delta\Psi$ (from 0.09 A to 0.15 A with steps of 100 µA). The next step is to generate the matrix $F_{sw,m}$ by evaluating (23) for the possible combinations of L_v and $\Delta\Psi_v$, which is used to identify the region where the switching frequency is lower or equal than $F_{sw,max}$ (300 kHz). Moreover, the stability condition (35) is evaluated for each possible combination of L_v and $\Delta\Psi_v$ elements, which serves to determine the regions where the system is stable or unstable. Finally, Figure 10 is the result of plotting $F_{sw,m}$ in the region where the system is stable and the switching frequency is lower than or equal to 300 kHz. For this example, a point at the frontier of that zone is selected to define a maximum switching frequency equal to 300 kHz, but any other one can be used; the particular point is $\{L = 770\ \mu\text{H}, \Delta\Psi = 113\ \text{mA}\}$.

2.6.2. Design of the Capacitor and Controller Parameters

The next step is to design the capacitor of the power stage. This process is performed using Equation (51) to ensure an average voltage deviation smaller than MO_{dc}, and using Equation (56) to ensure a voltage ripple lower than Δv_{dc} at the DC side. Both expressions provide the minimum C value needed to fulfill MO_{dc} and Δv_{dc} conditions; thus, a capacitor higher than the result of both equations must be selected.

Figure 11 shows the equations for calculating both MO_{dc} and Δv_{dc} (solid lines), and the zones in which the average voltage deviation and voltage ripple are below the design parameters defined in Table 2. In this application example, $C \geq 663.15$ µF is needed to fulfill the desired maximum Δv_{dc}, according to (56); while $C \geq 823.62$ µF is required to meet the MO_{dc} restriction given by (51); therefore, in this particular case, the limit imposed by (51) is the most restrictive condition. For this example, the value $C = 827$ µF is selected inside both zones, which provides $MO_{dc} = -9.96$ V and $\Delta v_{dc} = 3.2$ V, thus fulfilling the restrictions given in Table 2.

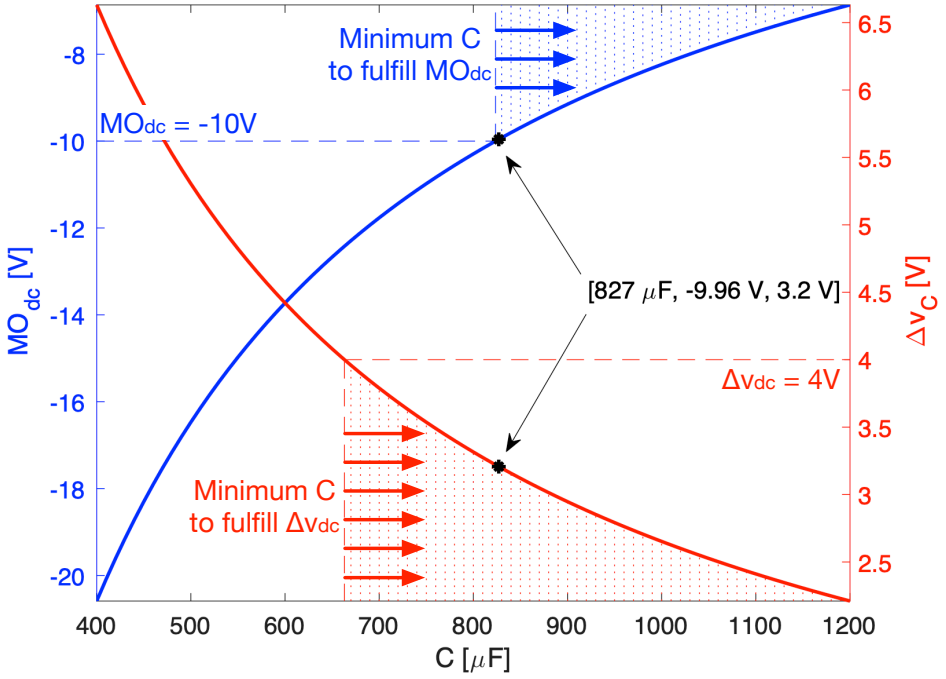

Figure 11. Design of the capacitor C.

With the previous capacitance value, and the parameters of Table 2, expressions (45) and (46) are used to calculate the normalized parameters of the adaptive voltage controller $x_p = 0.0645$ and $x_i = 2.5165$.

2.6.3. Summary of the Design Process

The design process is summarized in the flowchart depicted in Figure 12, where the processes to design the power and control stages are clearly described. The flowchart also shows that both processes can be performed in parallel due to the separability of the equations involved in those calculations.

The previous flowchart put into evidence the simplicity of the design process needed to parameterize the proposed rectifier with power factor correction; hence, providing a simple-to-use solution for real-world applications.

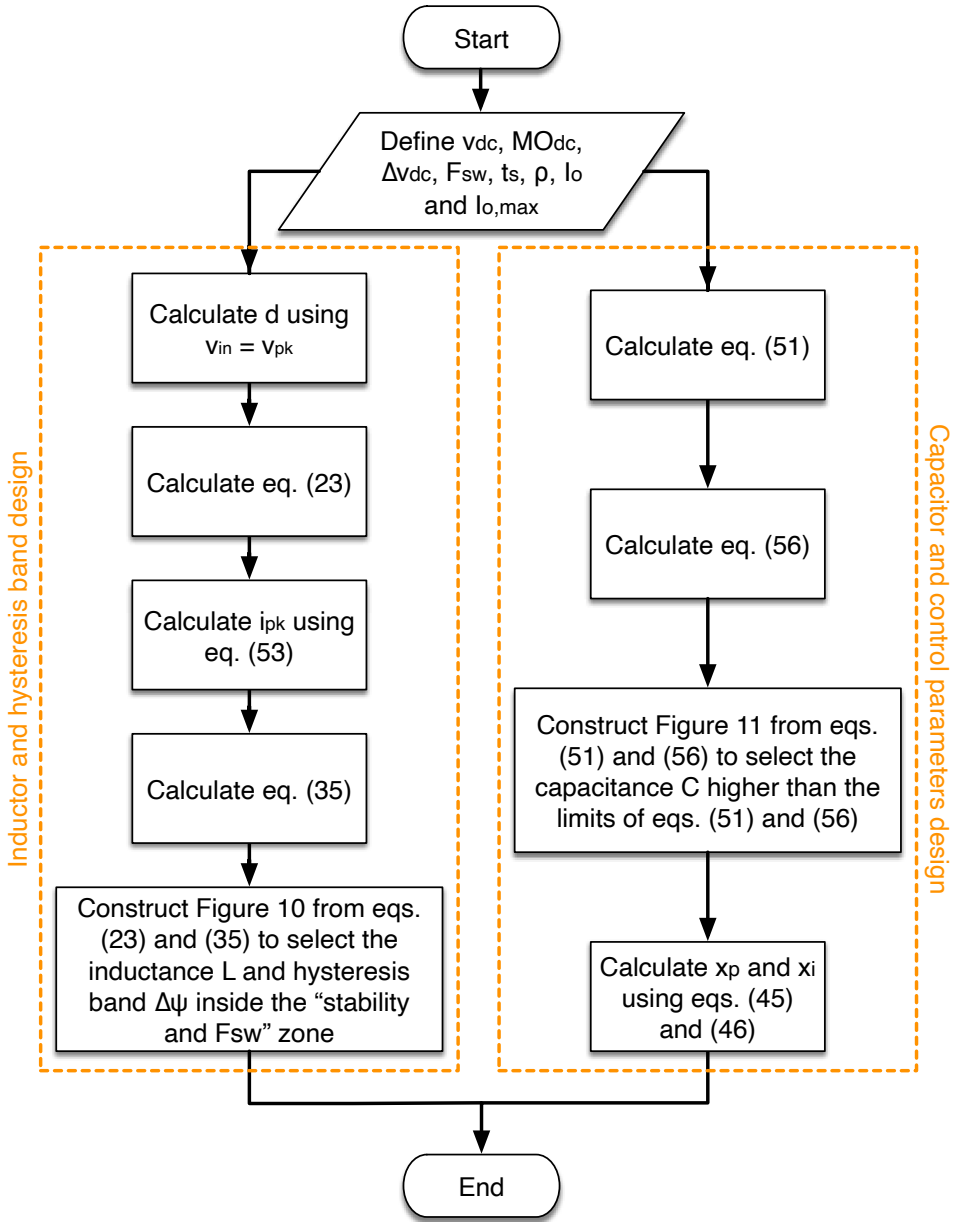

Figure 12. Flowchart of the design process.

At this point, it is important to remark on the main contributions of the proposed control system and the co-design procedure described in this section. The first one is that the control-oriented mathematical model considers a generic model for the load, which allows the representation of nonlinear loads in the rectifier. The second contribution is the design procedure of the SMC hysteresis band ($\Delta\Psi$) and the converter inductance (L) to guarantee the global stability of the SMC. The third contribution is the design procedure of the converter capacitance (C) that meets the desired maximum overshoot and maximum ripple of v_{dc}. The last contribution is the adaptive PI to regulate v_{dc}, where the time-varying gains k_p and k_i ensure the desired damping ratio and settling time.

3. Results

The proposed solution was implemented in the power electronics simulator PSIM, which is an industry standard. Figure 13 depicts the electrical implementation of both the power and control stages, where the control stage is divided into the current SMC and the adaptive voltage controller. Such an scheme is based on power elements (inductor, capacitor, MOSFET, diode, bridge rectifier, transformer), current and voltage sensors, gains, analog

comparators, a flip-flop, adders, and analog multipliers and dividers, which are available as integrated circuits. In this way, the SMC can be implemented using a TS555-integrated circuit, where the hysteresis band is defined with a constant gain, as reported in [37]. The adders, subtractors, constant gains, and integrator can be implemented using operational amplifiers, and the constant values can be defined with zener diodes and variable resistors. The multiplications and divisions are commonly implemented using analog circuits such as the HA-2557 [38], RC4200 [39], and AD533 [40]; while the current sensor is usually a small shunt resistor. It is also important to avoid the chattering phenomenon [41], which is caused by a high-frequency switching of the sliding mode controller exiting nonmodeled dynamics of the system. In [41], it was demonstrated that the first step for avoiding this phenomenon is to limit the switching frequency, which was already discussed in Section 2.2.4. Therefore, the final step is to select analog circuitry fast enough to avoid sensible chattering effects on the SMC. For the example designed in the previous section, the switching frequency is limited up to 300 kHz; thus, the analog circuitry for the implementation must have a bandwidth larger than 1.0 MHz, which are not difficult to find.

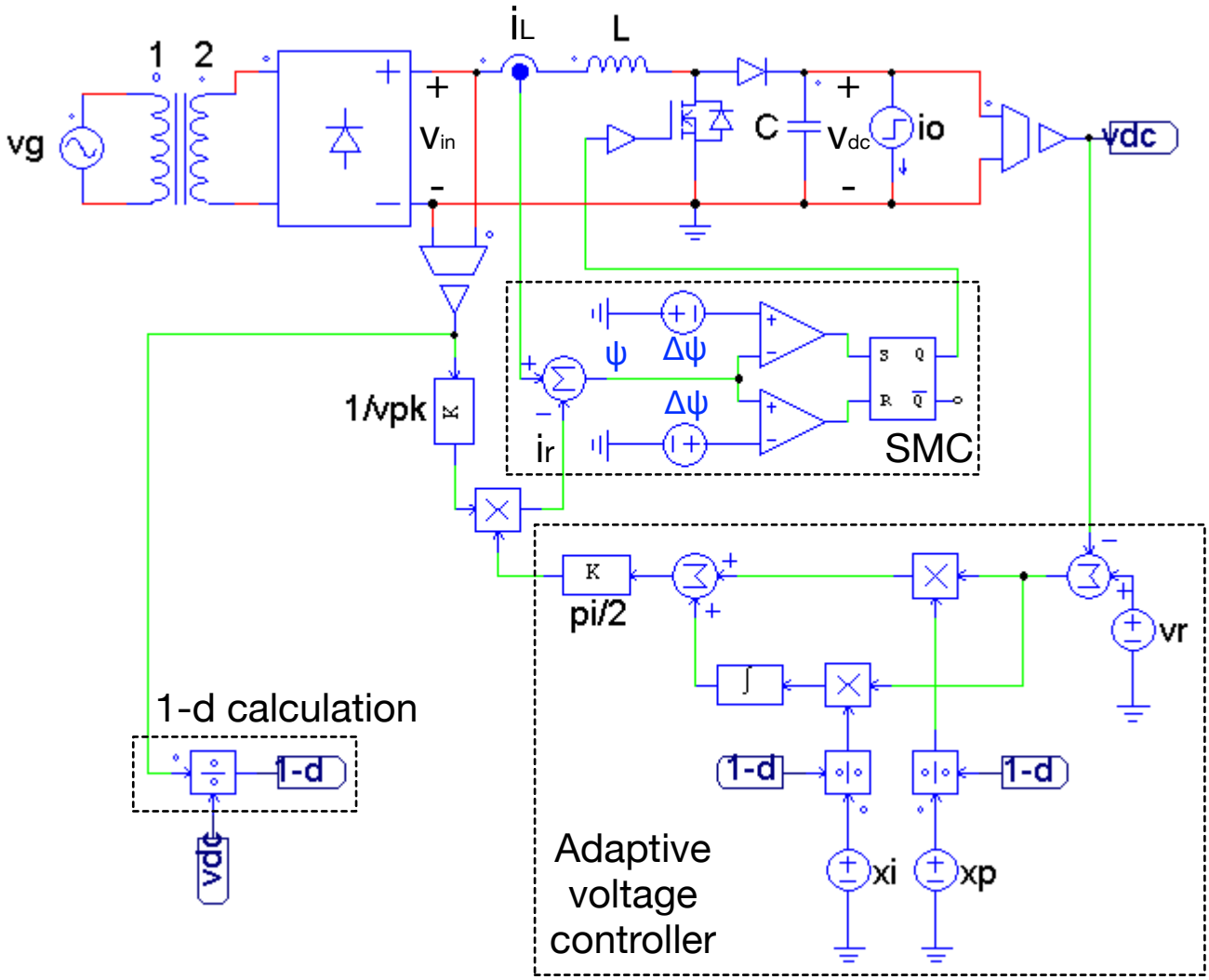

Figure 13. Application example implemented in the power electronics simulator PSIM.

The simulation of the previous PSIM circuit are presented in Figure 14, where the current requested to the bridge rectifier (i_L) is equal to the reference (i_r), which confirms the accuracy of the current SMC. Moreover, the simulation validates the accuracy of the reference generation, since the voltage (v_{in}) and current (i_L) at the bridge rectifier output are in phase. This is further confirmed by the current (i_g) and voltage (v_g) waveforms of

the grid, which are in phase. In fact, the simulation data reports a grid-side power factor $PF = 0.9997$ and a $THD = 1.84 \times 10^{-2}\%$, which is close to an ideal condition ($PF = 1$, $THD = 0\%$). Finally, Figure 14 also reports the switching frequency of the MOSFET and diode, which is limited to 300 kHz as expected.

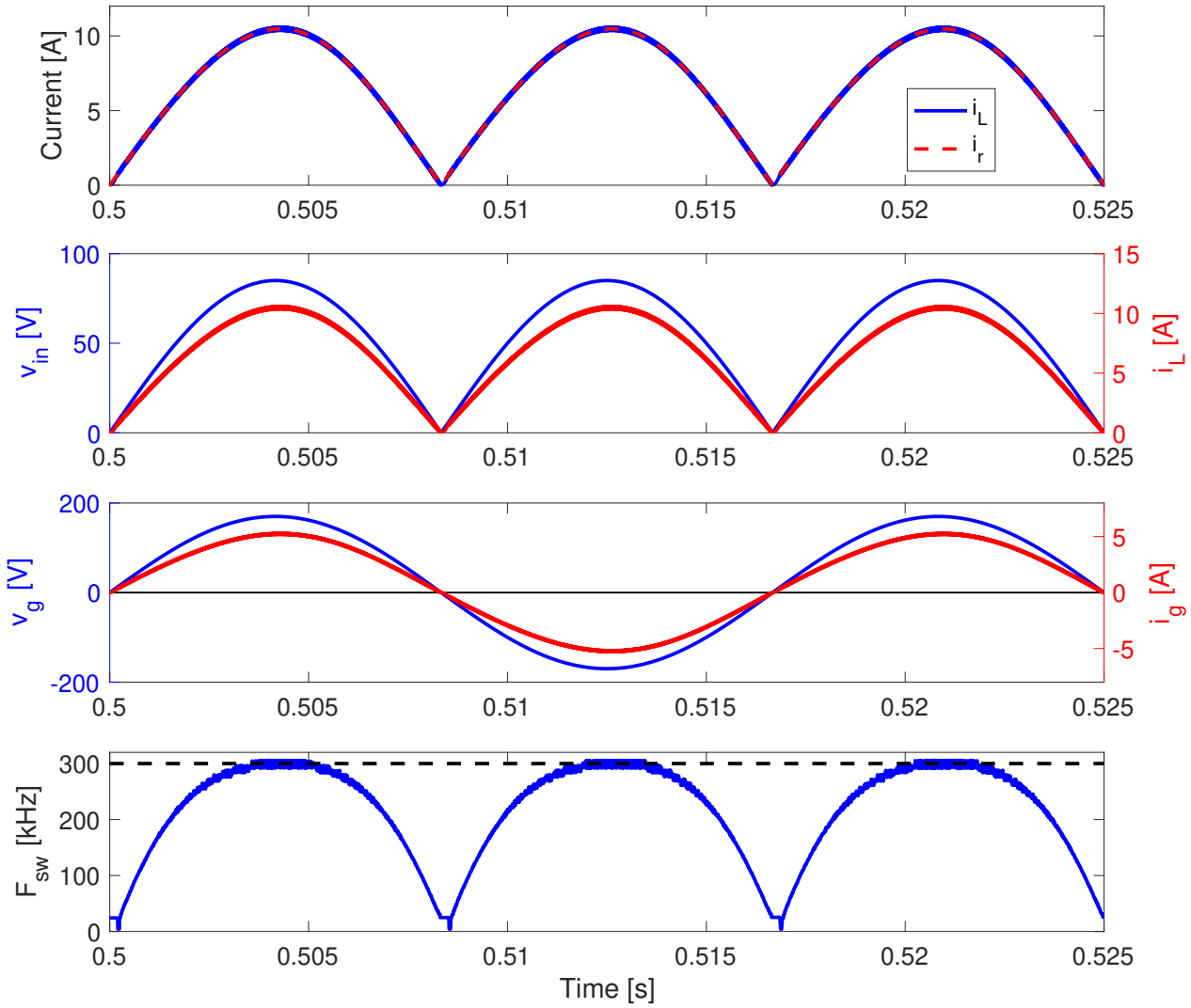

Figure 14. Validation of the SMC, inductor current and hysteresis band.

Section 2.3 discussed the possible instability of the rectifier when v_{in} is near to zero, which is confirmed in the zoom presented in Figure 15. Such a figure confirms that the designed value for L ensures that the switching function Ψ is always inside the hysteresis band, thus the inductor current closely follows the reference. The figure also shows the same waveform around $v_{in} = v_{pk}$, where the switching function is always triangular and inside the hysteresis band. Therefore, this simulation confirms the correct operation of the SMC, and the correct design of L and $\Delta\Psi$.

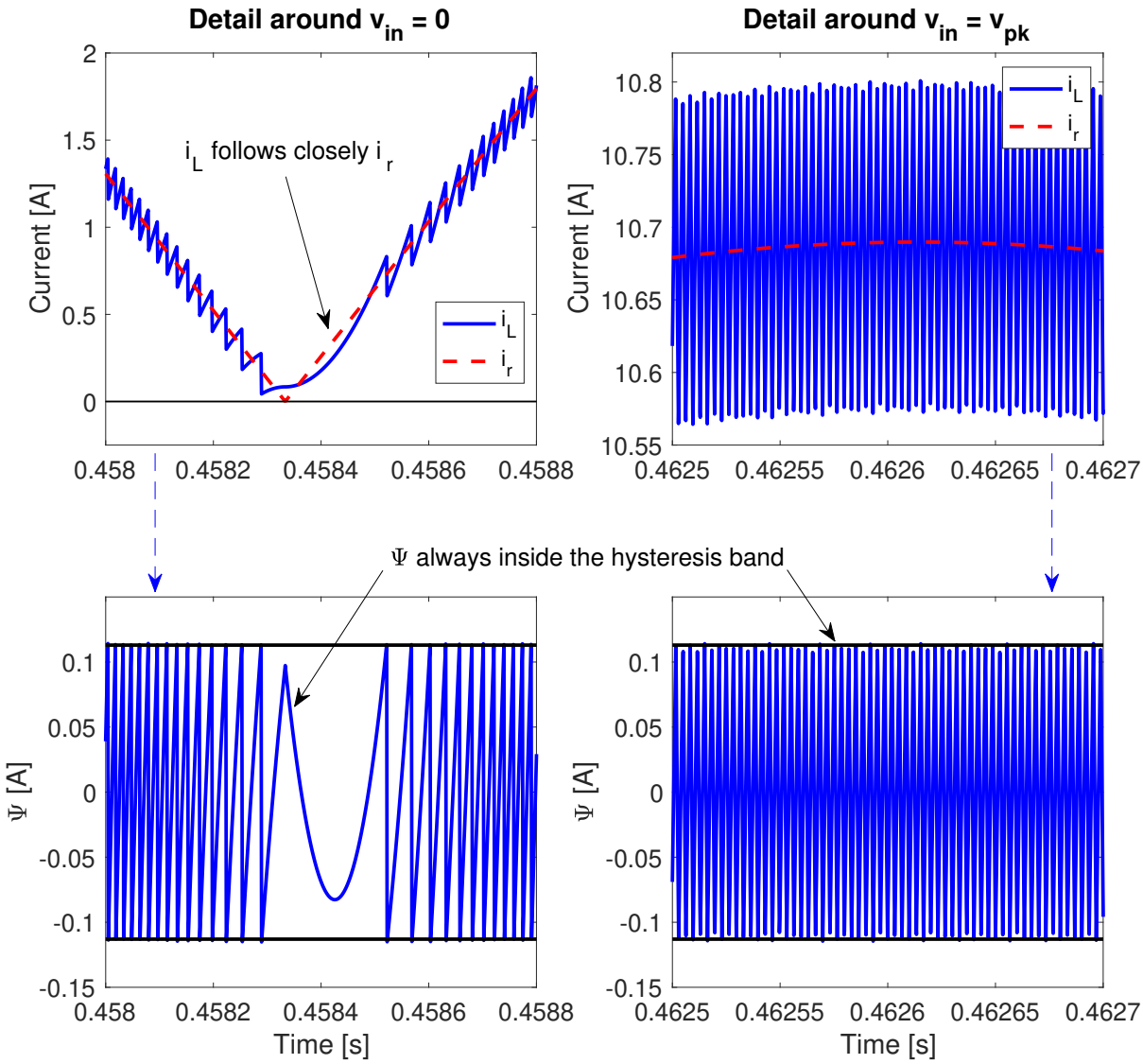

Figure 15. Zoom at v_{in} around 0 V (**left**) and v_{in} around v_{pk} (**right**).

The previous fact is emphasized by changing the inductor value as given in Figure 16: the first simulation at the left is performed with an inductor with half the designed size, which ensures global stability; however, the switching frequency is much higher than the design limit, so it is not suitable for the application example. The simulation at the middle is performed with an inductor of twice the designed size, which ensures a switching frequency lower than the design limit, but near $v_{in} = 0$ the switching function operates outside the hysteresis band, which causes a current distortion, thus degrading the power factor and THD. The simulation at the left was performed with a much higher inductor (five times the designed size) to illustrate the problem of over-dimensioning the inductor: the switching function operates much further from the hysteresis band, which causes a larger distortion into the inductor current, which is translated into a distorted grid current; in fact, the simulation shows that in this last case, 11% of the negative semi-cycle of the grid current is distorted, which significantly impact the power factor and THD. Therefore, it is confirmed that not following the proposed design process could produce excessively high switching frequencies or unstable behaviors.

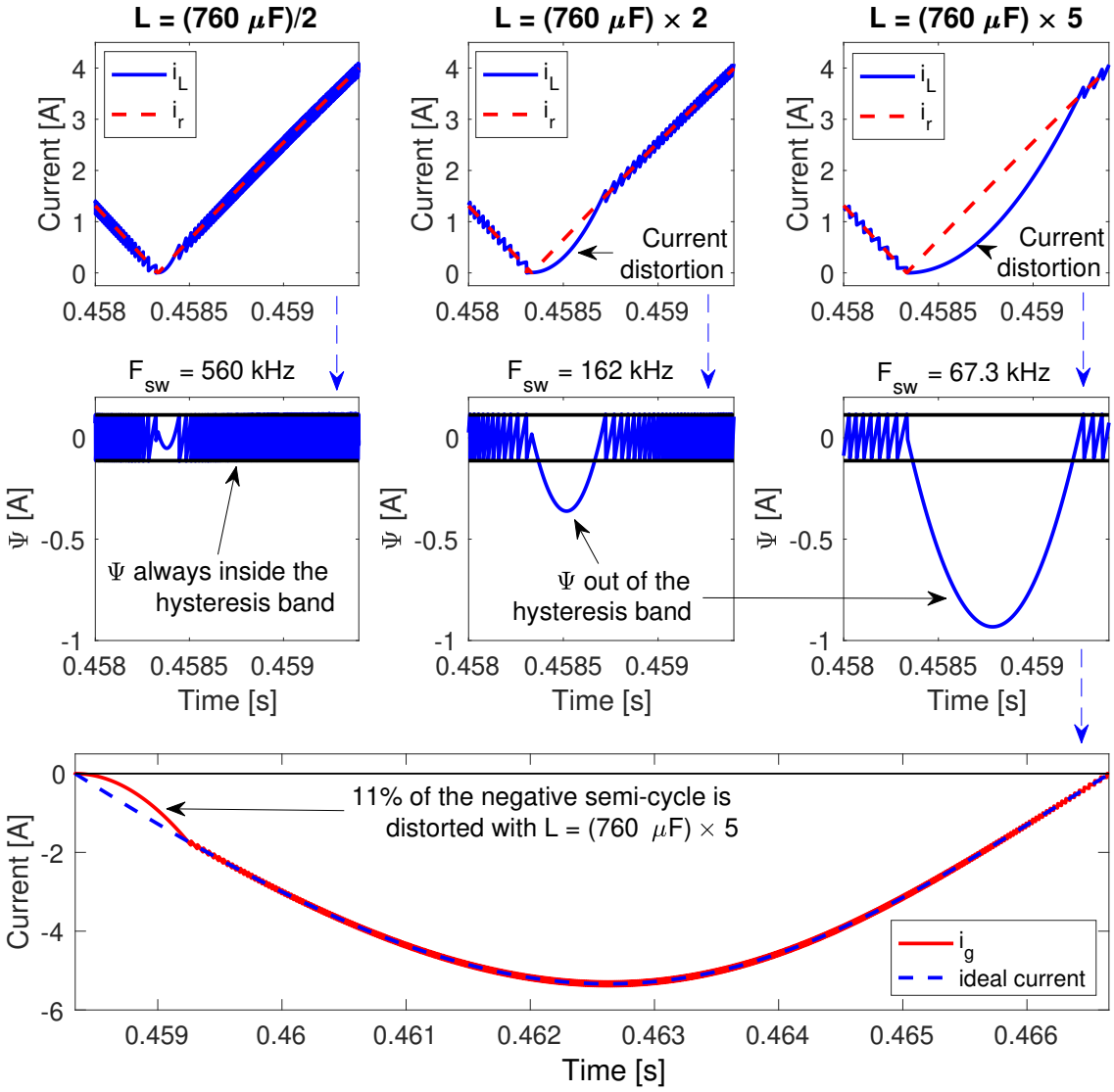

Figure 16. Effects of violating the L and $\Delta\Psi$ design.

The previous simulations have confirmed the correct operation of the proposed solution at the AC side. Similarly, the simulation reported in Figure 17 shows the waveforms at the DC side. This simulation considers a step change on the load current from 1 A to 2 A, which corresponds to I_o = 1 A and $I_{o,max}$ = 2 A. The upper waveforms show the load voltage v_{dc} and the corresponding average value $\langle v_{dc} \rangle$, which confirm the expected settling time t_s = 100 ms and maximum deviation $MO_{dc} = -9.96$ V, those in agreement with the maximum limits defined in Table 2. The figure also shows the average value of the peak current $\langle i_{pk} \rangle$, which corresponds to the output of the adaptive voltage controller; moreover, the adaptive parameters of the voltage controller (k_p and k_i) are also depicted in this figure. In conclusion, this simulation confirms the designed dynamic behavior is achieved.

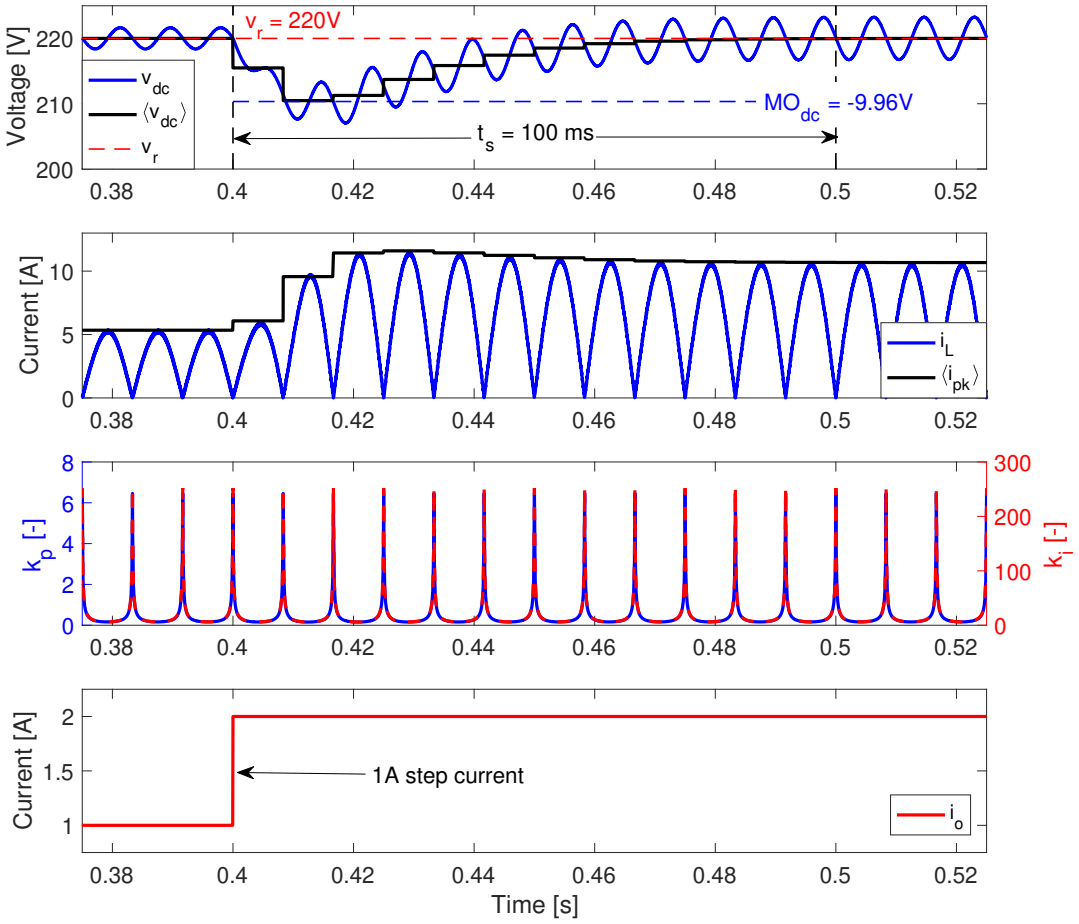

Figure 17. Validation of the capacitor and adaptive controller.

In addition, Figure 18 provides a zoom of the low-frequency ripple at both steady-state conditions (Io = 1 A and Io = 2 A). Since the design of Δv_{dc} is performed for $I_{o,max}$ = 2 A, the voltage ripple at that condition perfectly march the expected value Δv_{dc} = 3.2 V, while for Io = 1 A the voltage ripple is much smaller. Therefore, the simulations reported in Figures 17 and 18 confirm the correct operation of the adaptive voltage controller, and the correct design of C.

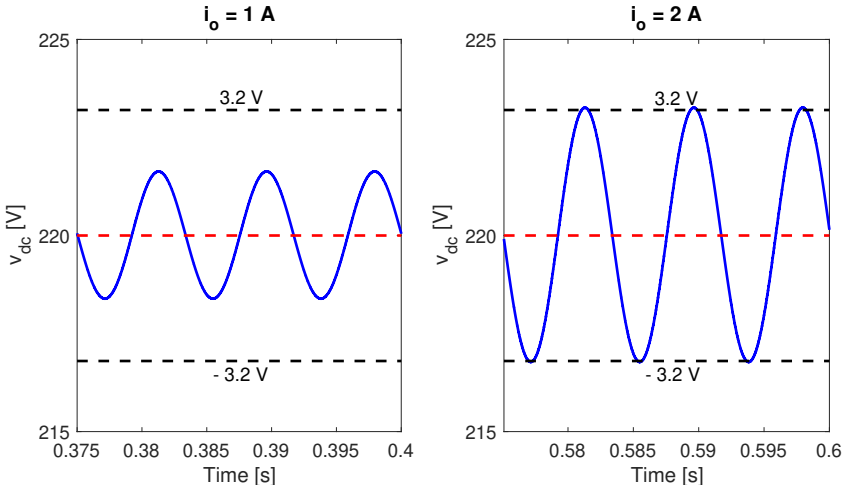

Figure 18. Validation of the low-frequency ripple.

An additional simulation was performed to evaluate the robustness of the proposed controller to changes on the grid voltage. Moreover, such a simulation also compares the performance of the proposed solution with the control system reported in [21] (named feedforward), which provides a fair comparison since both controllers have adaptive gains calculated to compensate for changes on the operating conditions, and both controllers require the same measurements (inductor current i_L, input voltage v_{in} and dc voltage v_{dc}). Figure 19 shows the simulation results, where the same Boost-based rectifier is controlled by both solutions. The simulation considers two perturbations: a 50% reduction in the load current i_o and a 50% reduction in the magnitude of the grid voltage v_g. As expected, the proposed solution is robust to perturbations on both the load current and grid voltage, providing the same performance on the DC voltage v_{dc} for all operating conditions, i.e., without additional overshoots/undershoots. Instead, the feedforward solution introduces an additional undershoot on the DC voltage $v_{dc,ff}$ when the load current is decreased; similarly, it introduces an additional overshoot on $v_{dc,ff}$ when the magnitude of the grid voltage is decreased. Moreover, the voltage deviations on the load provided by the proposed solution are smaller, and the settling-time of the DC voltage is shorter. The fast response of the SMC improves the performance of the proposed solution, where the adaptive voltage loop ensures the same performance for any operating condition. Instead, the calculation of the adaptive gains of the feedforward solution require the data generated by a peak detector, which introduces a delay equal to half of the grid period, thus delaying the compensation of the DC voltage in comparison with the proposed SMC.

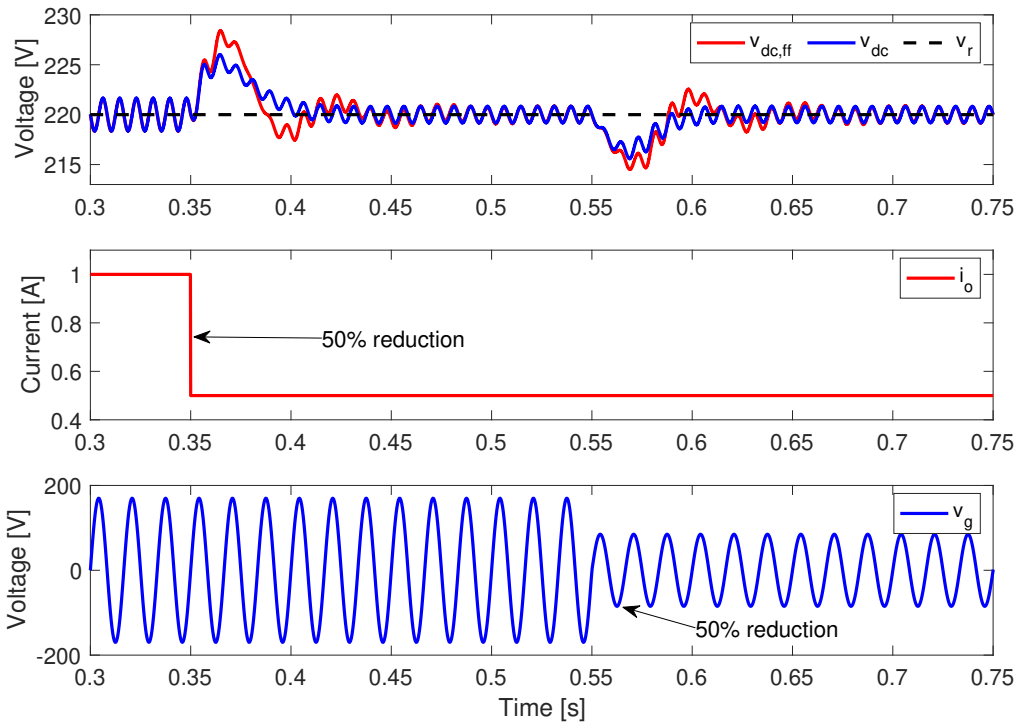

Figure 19. Performance comparison of the proposed solution with a feedforward/feedback controller.

The robustness of the proposed controller to variations on the inductor and capacitor values is evaluated in the simulation presented in Figure 20, which considers a load current perturbation of 50 %. In addition, the simulation considers variations on the inductor and capacitor from 95 % to 105 % of the nominal values. The simulation results show that the control system provides the same dynamic response on the DC voltage even with variations on those parameters. Therefore, those results verify the robustness of the proposed controller to variations on the electrical components, which could be caused by aging or manufacturer tolerances.

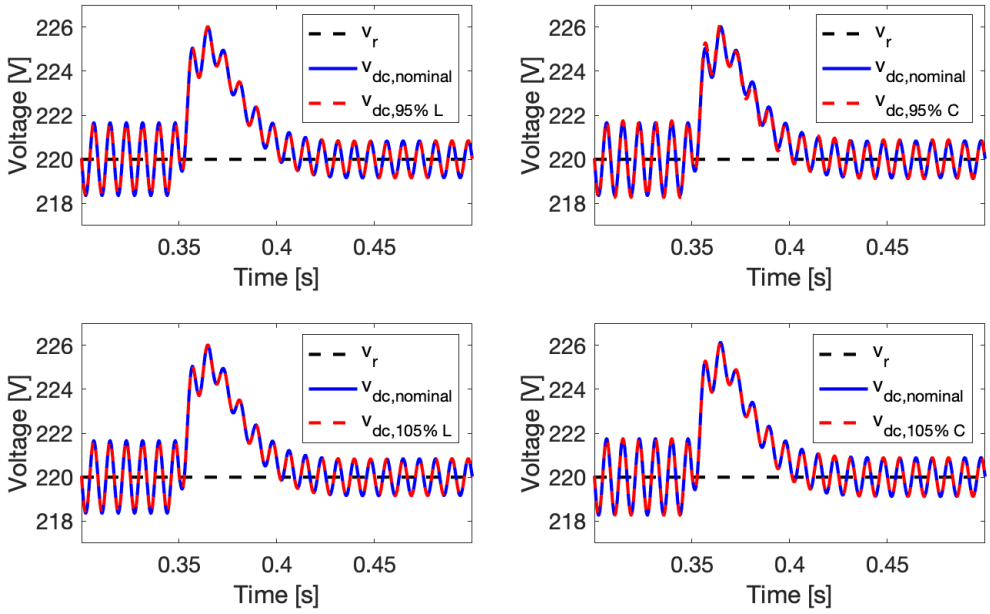

Figure 20. Evaluation of the controller robustness to variations on the inductor and capacitor.

Finally, the results presented in this section confirm the main contributions of the proposed approach for an application example, illustrating that it can be applied to other Boost-based PFC rectifiers with different power levels, design criteria, load characteristics, and grid voltage parameters. These results show that the proposed design procedure of the $\Delta\Psi$ and L guarantees the SMC stability under different disturbances and operating conditions. Moreover, the results also show that the procedure to design C provides the desired maximum overshoot and maximum ripple of v_{dc}. Further, the proposed procedure to dynamically adapt k_p and k_i of the v_{dc} PI regulator, ensures the desired damping ratio and settling time for any operating condition and disturbances on i_{dc} and v_{pk}.

4. Discussion

A co-design procedure of the control system and power stage of Boost-based PFC rectifiers has been introduced. This procedure assures the system stability in any operating condition, even when the input voltage is close to 0 V. In addition, the design procedure guarantees a maximum converter switching frequency as well as the meet of the desired dynamics of the DC voltage: maximum ripple, desired damping ratio, and settling time and maximum overshoot before load disturbances. In the proposed cascade controller, the outer loop is an adaptive PI regulator of the DC voltage and the inner loop is an SMC to set the inductor current. The paper includes the stability analysis of the SMC as well as a detailed procedure to design the converter inductor, capacitor, and the parameters of the PI regulator to meet the desired performance.

Simulation results of an application example in the specialized software PSIM validate the proposed procedure and show that the system is stable, i.e., Ψ is inside the hysteresis band, in any operating condition. Moreover, the results also show that the DC voltage meets the design requirements, since, on the one hand, it is regulated to the desired reference (220 V) with the desired maximum ripple (Δv_{dc} = 4 V), which is obtained for the maximum current load ($I_{o,max}$ = 2 A). On the other hand, the results also show that the controller provides zero steady-state errors before a step in the load with a settling time and maximum overshoot within the desired limits (100 ms and -10 V).

The future work is oriented to the experimental validation of the proposed rectifier and its integration into applications such as electric vehicle chargers or microgrids. In the first case, it requires the design and implementation of a higher-order controller to fulfill the necessities of the batteries' charging strategy. In the second case, it would

require the integration of the proposed rectifier with the microgrid controller through a communication link.

Author Contributions: Conceptualization, C.A.R.-P., A.J.S.-M. and J.D.B.-R.; methodology, C.A.R.-P., A.J.S.-M. and J.D.B.-R.; software, C.A.R.-P., A.J.S.-M. and J.D.B.-R.; validation, C.A.R.-P., A.J.S.-M. and J.D.B.-R.; writing—original draft preparation, C.A.R.-P., A.J.S.-M. and J.D.B.-R.; writing—review and editing, C.A.R.-P., A.J.S.-M. and J.D.B.-R. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the Universidad Nacional de Colombia and the Instituto Tecnológico Metropolitano under the research project "Microinversor de alta eficiencia para maximizar la extracción y transferencia de energía desde paneles fotovoltaicos ubicados en zonas con sombreado parcial a cargas de corriente alterna y voltaje estándar (110 V)" (Hermes code 49938, ITM code PE21103).

Institutional Review Board Statement: Not applicable.

Informed Consent Statement: Not applicable.

Data Availability Statement: The data used in this study are reported in the paper's figures and tables.

Acknowledgments: The authors thank the Facultad de Minas (Sede Medellin) and Facultad de Ingeniería y Arquitectura (Sede Manizales) of the Universidad Nacional de Colombia.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. De Castro Pereira, D.; Da Silva, M.R.; Silva, E.M.; Tofoli, F.L. Comprehensive review of high power factor AC-DC boost converters for PFC applications. *Int. J. Electron.* **2015**, *102*, 1361–1381. [CrossRef]
2. Ortiz-Castrillón, J.R.; Mejía-Ruíz, G.E.; Muñoz-Galeano, N.; López-Lezama, J.M.; Saldarriaga-Zuluaga, S.D. PFC Single-Phase AC/DC Boost Converters: Bridge, Semi-Bridgeless, and Bridgeless Topologies. *Appl. Sci.* **2021**, *11*, 7651. [CrossRef]
3. *IEC 61000-3-2:2018*; Electromagnetic Compatibility (EMC)—Part 3-2: Limits—Limits for Harmonic Current Emissions (Equipment Input CURRENT $\leq$16 A Per Phase). IEC: Geneva, Switzerland, 2018.
4. IEEE. *IEEE 519-2014—IEEE Recommended Practice and Requirements for Harmonic Control in Electric Power Systems*; IEEE: Piscataway, NJ, USA, 2014.
5. Memon, A.H.; Ali, R.; Memon, Z.A. Discontinuous conduction mode Buck converter with high efficiency. *3C Tecnol.* **2021**, *10*, 35–51. [CrossRef]
6. González-Castaño, C.; Restrepo, C.; Sanz, F.; Chub, A.; Giral, R. DC Voltage Sensorless Predictive Control of a High-Efficiency PFC Single-Phase Rectifier Based on the Versatile Buck-Boost Converter. *Sensors* **2021**, *21*, 5107. [CrossRef]
7. Kamalapathi, K.; Priyadarshi, N.; Padmanaban, S.; Holm-Nielsen, J.B.; Azam, F.; Umayal, C.; Ramachandaramurthy, V.K. A Hybrid Moth-Flame Fuzzy Logic Controller Based Integrated Cuk Converter Fed Brushless DC Motor for Power Factor Correction. *Electronics* **2018**, *7*, 288. [CrossRef]
8. Umamaheswari, M.G.; Uma, G.; Vijayalakshmi, K.M. Design and implementation of reduced-order sliding mode controller for higher-order power factor correction converters. *IET Power Electron.* **2011**, *4*, 984–992. [CrossRef]
9. Yang, J.W.; Do, H.L. Efficient Single-Switch Boost-Dual-Input Flyback PFC Converter With Reduced Switching Loss. *IEEE Trans. Ind. Electron.* **2015**, *62*, 7460–7468. [CrossRef]
10. Garcia-Sanchez, J.R.; Hernandez-Marquez, E.; Ramirez-Morales, J.; Marciano-Melchor, M.; Marcelino-Aranda, M.; Taud, H.; Silva-Ortigoza, R. A Robust Differential Flatness-Based Tracking Control for the 'MIMO DC/DC Boost Converter-Inverter-DC Motor' System: Experimental Results. *IEEE Access* **2019**, *7*, 84497–84505. [CrossRef]
11. Montoya, O.D.; Serra, F.M.; Gil-González, W.; Asensio, E.M.; Bosso, J.E. An IDA-PBC Design with Integral Action for Output Voltage Regulation in an Interleaved Boost Converter for DC Microgrid Applications. *Actuators* **2022**, *11*, 5. [CrossRef]
12. Hoyos Velasco, C.I.; Hoyos Velasco, F.E.; Candelo-Becerra, J.E. Nonlinear dynamics and performance analysis of a buck converter with hysteresis control. *Computation* **2021**, *9*, 112. [CrossRef]
13. Trujillo, S.C.; Candelo-Becerra, J.E.; Hoyos, F.E. Performance of the boost converter controlled with ZAD to regulate dc signals. *Computation* **2021**, *9*, 96. [CrossRef]
14. Wang, Y.; Yang, Y.; Chen, Y.; Pan, T.C.; Guo, C.; Xia, A. Adaptive total sliding mode control for the current of power factor correction circuit. *IEICE Electron. Express* **2018**, *15*, 1–12. [CrossRef]
15. Pandey, A.; Kothari, D.P.; Singh, B. Sliding mode control of PFC converter. *IETE J. Res.* **2005**, *51*, 371–377. [CrossRef]
16. Kessal, A.; Lazhar, R.; Gaubert, J.P.; Mohammed, M. Analysis and design of an isolated single-phase power factor corrector with a fast regulation. *Electr. Power Syst. Res.* **2011**, *81*, 1825–1831. [CrossRef]

17. Genc, N.; Iskender, I. DSP-based current sharing of average current controlled two-cell interleaved boost power factor correction converter. *IET Power Electron.* **2011**, *4*, 1015–1022. [CrossRef]
18. Bosque-Moncusi, J.M.; Valderrama-Blavi, H.; Flores-Bahamonde, F.; Vidal-Idiarte, E.; Martínez-Salamero, L. Using low-cost microcontrollers to implement variable hysteresis-width comparators for switching power converters. *IET Power Electron.* **2018**, *11*, 787–795. [CrossRef]
19. Chiang, H.C.; Lin, F.J.; Chang, J.K.; Chen, K.F.; Chen, Y.L.; Liu, K.C. Control method for improving the response of single-phase continuous conduction mode boost power factor correction converter. *IET Power Electron.* **2016**, *9*, 1792–1800. [CrossRef]
20. Marcos-Pastor, A.; Vidal-Idiarte, E.; Cid-Pastor, A.; Martinez-Salamero, L. Interleaved Digital Power Factor Correction Based on the Sliding-Mode Approach. *IEEE Trans. Power Electron.* **2016**, *31*, 4641–4653. [CrossRef]
21. Wu, S.T.; Chen, F.Y.; Chien, M.C.; Wang, J.M.; Su, Y.Y. A Hybrid Control Scheme with Fast Transient and Low Harmonic for Boost PFC Converter. *Electronics* **2021**, *10*, 1848. [CrossRef]
22. Kessal, A.; Rahmani, L. Ga-optimized parameters of sliding-mode controller based on both output voltage and input current with an application in the PFC of AC/DC converters. *IEEE Trans. Power Electron.* **2014**, *29*, 3159–3165. [CrossRef]
23. Zhou, Y.; Wang, B.L. PWM-quasi-sliding mode control for APFC converters. *Electr. Eng.* **2010**, *92*, 43–48. [CrossRef]
24. Karabacak, M.; Poyraz, G. Robust adaptive control of pulse-width modulated rectifiers based on adaptive super-twisting sliding-mode and state feedback controllers. *Electr. Power Compon. Syst.* **2015**, *43*, 1289–1296. [CrossRef]
25. Mohanty, P.R.; Panda, A.K. Fixed-Frequency Sliding-Mode Control Scheme Based on Current Control Manifold for Improved Dynamic Performance of Boost PFC Converter. *IEEE J. Emerg. Sel. Top. Power Electron.* **2017**, *5*, 576–586. [CrossRef]
26. Kayisli, K.; Tuncer, S.; Poyraz, M. A Novel Power Factor Correction System Based on Sliding Mode Fuzzy Control. *Electr. Power Compon. Syst.* **2017**, *45*, 430–441. [CrossRef]
27. Seleme, S.I.; Rosa, A.H.; Morais, L.M.; Donoso-Garcia, P.F.; Cortizo, P.C. Evaluation of adaptive passivity-based controller for power factor correction using a boost converter. *IET Control. Theory Appl.* **2012**, *6*, 2168–2178. [CrossRef]
28. Karami, Z.; Shafiee, Q.; Khayat, Y.; Yaribeygi, M.; Dragicevic, T.; Bevrani, H. Decentralized Model Predictive Control of DC Microgrids with Constant Power Load. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 451–460. [CrossRef]
29. Rasoolzadeh, A.; Salmasi, F.R. Reduced-order dynamic model for droop-controlled inverter/converter-based low-voltage hybrid AC/DC microgrids - part 2: DC sub-microgrid and power exchange. *IET Smart Grid* **2018**, *1*, 134–142. [CrossRef]
30. Chatrenour, N.; Razmi, H.; Doagou-Mojarrad, H. Improved double integral sliding mode MPPT controller based parameter estimation for a stand-alone photovoltaic system. *Energy Convers. Manag.* **2017**, *139*, 97–109. [CrossRef]
31. Taheri, B.; Sedaghat, M.; Bagherpour, M.A.; Farhadi, P. A New Controller for DC-DC Converters Based on Sliding Mode Control Techniques. *J. Control. Autom. Electr. Syst.* **2019**, *30*, 63–74. [CrossRef]
32. Sira-Ramirez, H. Sliding Motions in Bilinear Switched Networks. *IEEE Trans. Circuits Syst.* **1987**, *34*, 919–933. [CrossRef]
33. Sira-Ramirez, H. Nonlinear variable structure systems in sliding mode: The general case. *IEEE Trans. Autom. Control.* **1989**, *34*, 1186–1188. [CrossRef]
34. Villegas Ceballos, J.P.; Serna-Garcés, S.I.; González Montoya, D.; Ramos-Paja, C.A.; Bastidas-Rodríguez, J.D. Charger/discharger DC/DC converter with interleaved configuration for DC-bus regulation and battery protection. *Energy Sci. Eng.* **2019**, *8*, 530–543. [CrossRef]
35. Henao-Bravo, E.E.; Saavedra-Montes, A.J.; Ramos-Paja, C.A.; Bastidas-Rodriguez, J.D.; Gonzalez Montoya, D. Charging/discharging system based on zeta/sepic converter and a sliding mode controller for dc bus voltage regulation. *IET Power Electron.* **2020**, *13*, 1515–1527. [CrossRef]
36. Umamaheswari, M.G.; Uma, G.; Vijayalakshmi, K.M. Analysis and design of reduced-order sliding-mode controller for three-phase power factor correction using Cuk rectifiers. *IET Power Electron.* **2013**, *6*, 935–945. [CrossRef]
37. Gonzalez Montoya, D.; Ramos-Paja, C.; Giral, R. Improved design of sliding mode controllers based on the requirements of MPPT techniques. *IEEE Trans. Power Electron.* **2016**, *31*, 235–247. [CrossRef]
38. Intersil. HA-2557 130 MHz, Four Quadrant, Current Output Analog Multiplier. 2002. Available online: https://www.alldatasheet.com/datasheet-pdf/pdf/122864/INTERSIL/HA-2557.html (accessed on 30 March 2022).
39. Fairchild Semiconductor. RC4200 Analog Multiplier. 2001. Available online: https://www.alldatasheet.com/datasheet-pdf/pdf/54398/FAIRCHILD/RC4200.html (accessed on 30 March 2022).
40. Analog Devices. AD533 Low Cost IC Multiplier, Divider, Squarer, Square Rooter. 2022. Available online: https://www.analog.com/en/products/ad533.html (accessed on 30 March 2022).
41. Alsmadi, Y.M.; Utkin, V.; Haj-ahmed, M.A.; Xu, L. Sliding mode control of power converters: DC/DC converters. *Int. J. Control.* **2018**, *91*, 2472–2493. [CrossRef]