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The Impact of Ambient Temperature on Electrothermal Characteristics in Stacked Nanosheet Transistors with Multiple Lateral Stacks

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Abstract: With characteristic size scaling down to the nanoscale range, the confined geometry exacerbates the self-heating effect (SHE) in nanoscale devices. In this paper, the impact of ambient temperature (T_{amb}) on the SHE in stacked nanosheet transistors is investigated. As the number of lateral stacks (N_{stack}) increases, the nanoscale devices show more severe thermal crosstalk issues, and the current performance between n- and p-type nanoscale transistors exhibits different degradation trends. To compare the effect of different T_{amb} ranges, the temperature coefficients of current per stack and threshold voltage are analyzed. As the N_{stack} increases from 4 to 32, it is verified that the zero-temperature coefficient bias point (V_{ZTC}) decreases significantly in p-type nanoscale devices when T_{amb} is above room temperature. This can be explained by the enhanced thermal crosstalk. Then, the gate length-dependent electrothermal characteristics with different N_{stack}s are investigated at various T_{amb}s. To explore the origin of drain current variation, the temperature-dependent backscattering model is utilized to explain the variation. At last, the simulation results verify the impact of T_{amb} on the SHE. The study provides an effective design guide for stacked nanosheet transistors when considering multiple stacks in circuit applications.

Keywords: nanoscale device; nanosheet; self-heating effect (SHE); ambient temperature; multiple lateral stacks; thermal crosstalk

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1. Introduction

With the characteristic size of integrated circuits (ICs) scaling down to the nanoscale range, the core transistor structures have gradually evolved into gate-all-around nanosheet FET (GAA NSFET) [1]. The GAA structure exhibits excellent electrostatic performance compared to FinFET technology [2]. At the same time, the nanosheet channel with a vertically stacked structure shows great performance advantages [3]. However, the confined geometry and low thermal conductivity materials, such as gate oxide and HfO_2, greatly hinder heat transport, leading to a severe self-heating effect (SHE) [4–7]. The thermal conductivity of Si active regions decreases significantly due to intensified phonon scattering. Then, the thermal conductivity of the source/drain (S/D) causes an additional decrease due to heavy doping and the SiGe alloy material adopted. In addition, the nanosheet channels are floated and isolated from the substrate, making it difficult to transport heat. Due to the gate stack structure, phonon-boundary scattering is intensified. These factors lead to SHE issues being prominent in NSFET. The SHE can cause degradation of electrical performance and bring about reliability issues, ultimately decreasing the device's

lifetime significantly [8–12]. Some researchers have conducted a series of investigations into SHE issues, including compact models, optimization technologies, and self-heating mechanisms [13–19]. In addition, the multiple lateral stacks are fabricated in NSFETs for high performance. The self-heating will be exacerbated due to the rising current in the lateral stack structure [7]. This is one aspect of thermal issues.

On the other hand, the core transistors work in practical application circuits. The electrical performance is inevitably affected by ambient temperature (T_{amb}), where the T_{amb} includes those from inside the chip and the surrounding environment. The high T_{amb} can change the temperature-sensitivity threshold voltage (V_{th}) and introduce variability in the on-state current. At the same time, the T_{amb} plays a crucial role in thermal properties, such as thermal conductivity, lattice temperature rise, and thermal resistance (R_{th}) [20–25]. Some researchers have analyzed the electrothermal characteristics of FinFETs with multiple fins under the impact of T_{amb} [20,23,26]. However, few studies focus on the research of T_{amb} on NSFET with different numbers of lateral stacks (N_{stack}). In addition, there are few works on the geometry effect in NSFETs with different N_{stack}s. Therefore, we performed a symmetrical investigation on the electrothermal performance of NSFETs with different N_{stack}s under the T_{amb} impact. Furthermore, the geometry effect with different N_{stack}s is also studied.

In this paper, the T_{amb}-dependent SHE in NSFETs with different N_{stack}s is symmetrically measured and analyzed. The rest of the article is divided into three parts. Section 2 discusses the fabrication of NMOS and PMOS in detail. In Section 3, the current variation with different N_{stack}s is explored. Then, the geometry effect with different gate lengths is further analyzed based on the backscattering model. In addition, the simulations are conducted for verification. Finally, the conclusion is given in Section 4.

2. Device Fabrication

The integration process flow design of the NSFET is summarized in Figure 1a, where the NSFET was grown on {100} bulk Si substrates. This process flow is based on the conventional fabrication process [27]. The fabrication adopts the gate last process. Before the stacked nanosheets were formed, B and P were implanted to suppress the bottom parasitic channel in the ground plane process for NMOS and PMOS, respectively [28]. The stacked GeSi/Si layers were formed using the epitaxy process. The nanosheet channels are stacked vertically with three layers (N_{ch} = 3). In this step, the reduced pressure chemical vapor deposition was used to grow the periodical GeSi/Si multilayer with 16 nm $Ge_{0.3}Si_{0.7}$ and 10 nm Si. Then, the fin array was carried out using spacer image transfer (SIT) technology, which was formed using a SiN_x hard mask. For high-performance desire, the stacked nanosheets were fabricated with multiple lateral stacks in this step, as shown in Figure 1b. The number of parallel nanorails of lateral stacks is defined as N_{stack}. The N_{stack} is 2, 4, 8, 16, and 32. Next, the shallow trench isolation (STI) was formed to decrease the leakage current between the devices. Meanwhile, the rapid annealing process was performed to make the film compact. Then, a dummy gate was fabricated with amorphous Si to protect the nanosheets. After the deposition of amorphous Si, the chemical mechanical planarization (CMP) was used to perform the planarization process. The dummy gate image was formed using deposition and etch of Si_3N_4 hard mask. The inner spacer formation was a key process that was deposited using SiN_x and etched using reactive ion etching (RIE). After this, the in-situ doping process with highly doped doses and the activation process were carried out to form S/D. The zero-level interlayer dielectric (ILD0) with SiN_x is used to avoid the over-etch phenomenon. After the dummy gate removal, GeSi was selectively removed using the wet-etched technique. After forming the thin gate oxide layer, the HfO_2 was deposited and the nanosheet was surrounded by different metal stacks. The atom-layer-deposition technology (ALD) was used to deposit the multilayer HK/MG films, and the CMP was performed to achieve gate separation. Finally, the tungsten contact and the BEOL process were fabricated to complete the NSFETs.

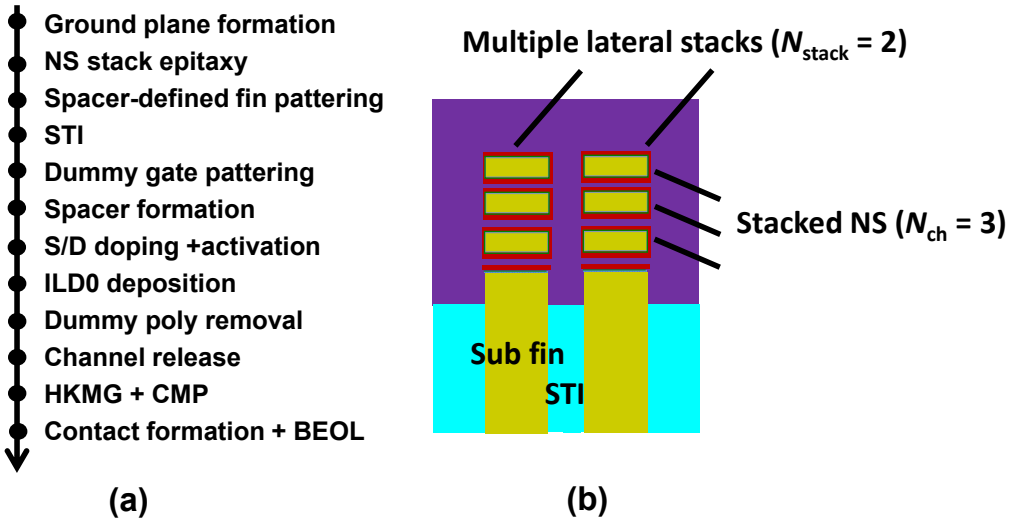

Figure 1. (**a**) Process flow of GAA NSFETs adopting the gate last process. (**b**) Schematic of the NSFET with multiple lateral stacks along the nanosheet width direction.

Through the measurement of transmission electron microscopy (TEM), Figure 2 shows the fabricated channel structure of NSFETs, which can be seen that the NSFETs are successfully fabricated according to the process flow. The nanosheets are separated using HK/MG, and the STI is formed near the sub-fin. The width of the sub-fin is similar to that of the nanosheet. The nanosheet width (W_{NS}) is about 30 nm, and the nanosheet thickness (T_{NS}) is about 10 nm. The gate length (L_G) is 30, 40, 60, and 500 nm. Then, energy-dispersive spectroscopy (EDS) is used to exhibit the distribution of elements in NSFETs, as shown in Figure 3. It shows that Ge has been completely removed, and the nanosheets are separated from each other. Each nanosheet is surrounded by Hf and oxide elements. This indicates that the nanosheets can be well controlled using bias voltages. At the same time, it can be seen that Al, Ti, N, and Ta elements are deposited surrounding the nanosheets, and the W element has been wrapped to the Si nanosheets.

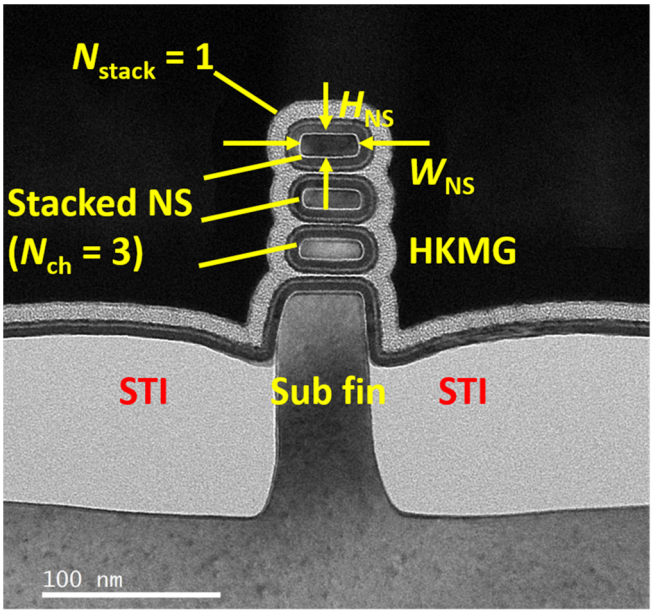

Figure 2. The TEM image of GAA NSFETs in this work. The nanosheets are separated from each other.

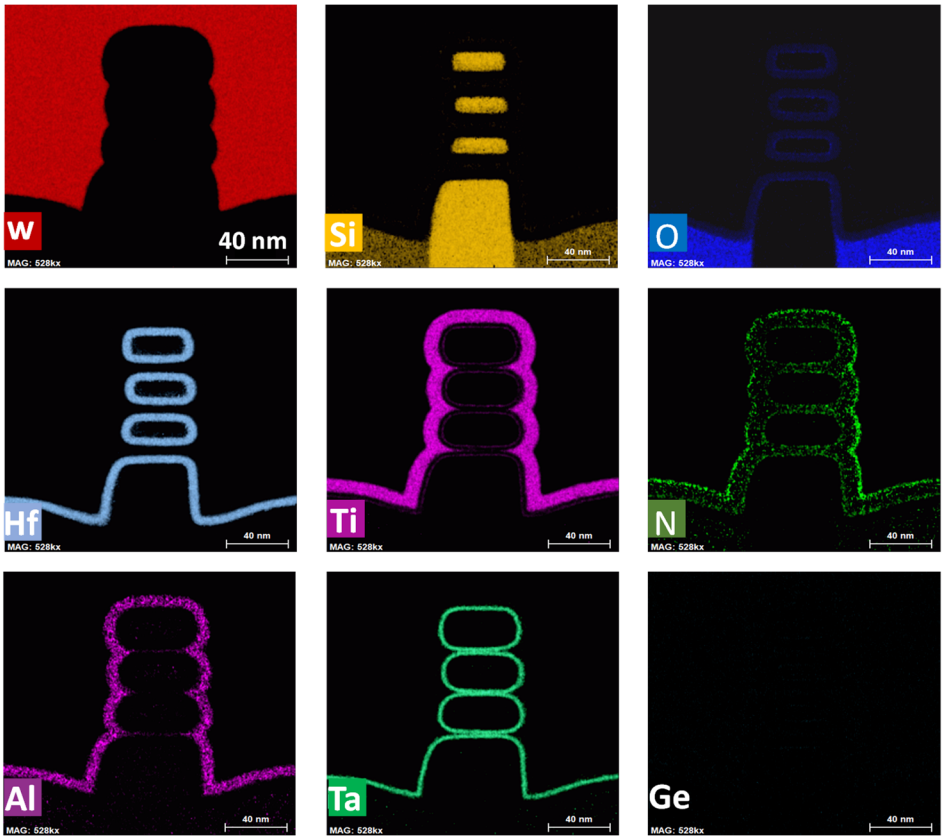

Figure 3. The EDS images of NSFETs in this work. The top figures illustrate W, Si, and O elements. The middle figures illustrate Hf, Ti, and N elements. The bottom figures illustrate Al, Ta, and Ge elements. Ge has been removed completely.

3. Results and Discussion

3.1. Electrothermal Performance of Different Numbers of Stacks under the Impact of Ambient Temperature

Since the measurement is dependent on ambient temperature (T_{amb}), the T_{amb}-dependent SHE in NSFETs is measured using the Agilent B1500 semiconductor parameter analyzer (Agilent Technologies, Santa Clara, CA, USA). The T_{amb} varies from −50 °C to 125 °C in a 25 °C step.

As shown in Figure 4, the transfer characteristic curves exhibit a variation in drain current (I_{DS}) as the T_{amb} increases for NMOS and PMOS. The threshold voltages (V_{th}s) are 300 mV and −300 mV at T_{amb} = 25 °C of room temperature (T_{rt}) for NMOS and PMOS, respectively. The V_{th} is extracted using the constant current method. As the T_{amb} increases, the $|V_{th}|$ decreases because the carrier concentration is positively correlated with the T_{amb}. In Figure 4a, the I_{DS} of NMOS shows an increasing trend. Meanwhile, the I_{DS} of PMOS also shows an increasing trend at a lower $|V_{GS}|$. However, it exhibits a reverse temperature dependence at a larger $|V_{GS}|$, as shown in Figure 4b. This is because the effect of the V_{th} reduction exceeds that of the mobility degradation in NMOS. However, the effect of the $|V_{th}|$ reduction is inferior to that of the mobility degradation at a larger $|V_{GS}|$ in PMOS. Moreover, the I_{DS} of PMOS is higher than that of NMOS at a larger $|V_{GS}|$. The current degradation indicates that the higher current is more severely impacted by T_{amb}. In addition, it is found that the zero-temperature coefficient bias point (V_{ZTC}) occurs in PMOS, where the V_{ZTC} represents the bias voltage point that the I_{DS} is independent of the T_{amb} [29]. In addition, there are two V_{ZTC} under T_{amb} = −50~25 °C range and T_{amb} = 25~125 °C range.

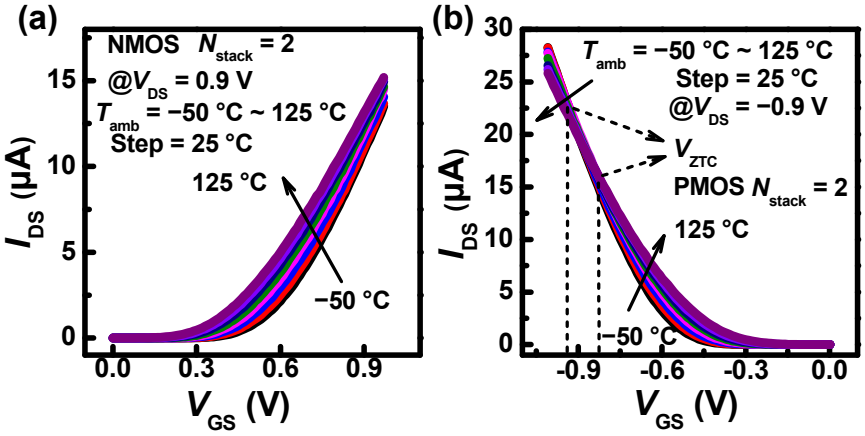

Figure 4. Experimental temperature dependence of transfer characteristics at L_G = 500 nm, N_{stack} = 2, (**a**) V_{DS} = 0.9 V for NMOS and (**b**) V_{DS} = −0.9 V for PMOS. It shows two V_{ZTC} under T_{amb} = −50~25 °C range and T_{amb} = 25~125 °C range.

To explore the T_{amb}-dependent relation, Figure 5 shows that the I_{DS} variations with different N_{stack}s under the impact of T_{amb} are extracted relative to the I_{DS} at T_{amb} = −50 °C, and the gate overdrive voltage ($V_{ov} = V_{GS} - V_{th}$) is 0.43 V and −0.43 V for NMOS and PMOS, respectively. The I_{DS} degradation of NMOS is lower than that of PMOS. At high T_{amb}, The NMOS with N_{stack} = 4 shows the largest I_{DS} degradation, and other multiple stacks have minor differences. The devices with N_{stack} = 2 have the lowest I_{DS} degradation at high T_{amb} in Figure 5a. PMOS shows a different trend when N_{stack} increases, as shown in Figure 5b. The PMOS with N_{stack} = 2 shows the largest I_{DS} degradation, and other multiple stacks have minor differences. The PMOS with N_{stack} = 32 shows the lowest I_{DS} degradation. The I_{DS} variation in NMOS with N_{stack} = 4 and PMOS with N_{stack} = 2 may be induced by random structure irregularities.

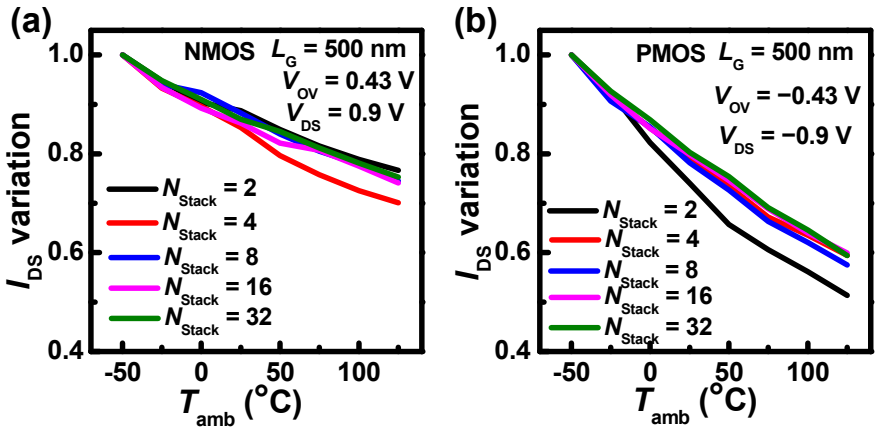

Figure 5. (**a**) I_{DS} variations of NMOS with different N_{stack}s under the impact of T_{amb} relative to the I_{DS} at T_{amb} = −50 °C, (**b**) I_{DS} variations of PMOS with different N_{stack}s under the impact of T_{amb} relative to the I_{DS} at T_{amb} = −50 °C.

To analyze the origin of the I_{DS} variation, the temperature coefficients of I_{DS} per stack (β) are extracted, as shown in Figure 6. Figure 6a shows that β in NMOS decreases in the negative direction under T_{amb} above T_{rt} when N_{stack} is from 4 to 32. This is induced by the coupling mechanism with the impact of the SHE and T_{amb}. As the N_{stack} increases, the thermal crosstalk is enhanced in stacked nanosheets, where the thermal crosstalk is part of the SHE. The SHE can intensify phonon-electron scattering, and then counteract the partial effect of T_{amb}, resulting in reduced I_{DS} degradation. In Section 3.3, the simulation results will further verify the speculation. The β in NMOS with N_{stack} = 2 is the lowest [Figure 6a]. This can be caused by difficult heat transport due to the smaller contact area

between nanosheets and the S/D region, leading to severe thermal crosstalk. Meanwhile, the β under T_{amb} below 0 °C is basically larger than that under T_{amb} above T_{rt}. This is because the impact of thermal crosstalk is weakened by enhanced heat transport ability.

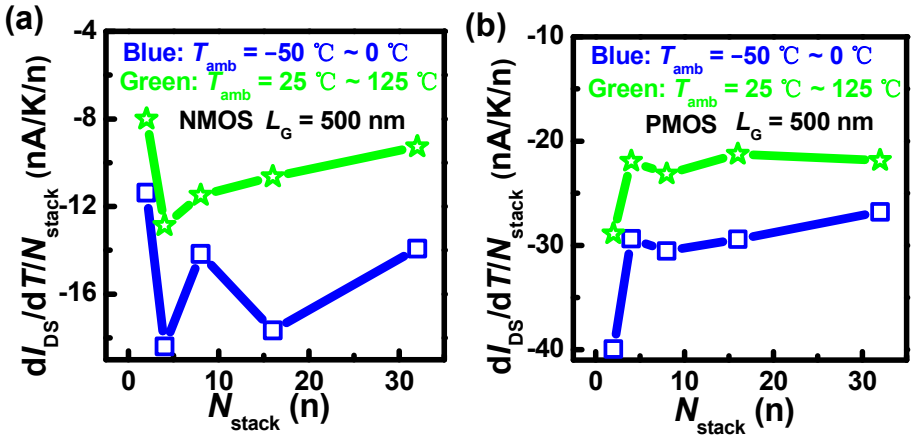

Figure 6. L_G = 500 nm, (**a**) V_{DS} = 0.9 V, V_{ov} = 0.59 V, the temperature coefficients of I_{DS} per stack in NMOS, (**b**) V_{DS} = −0.9 V, V_{ov} = −0.59 V, the temperature coefficients of I_{DS} per stack in PMOS under different T_{amb} ranges.

Figure 6b shows that the β in PMOS is larger than that in NMOS. The carrier scattering intensifies by T_{amb} because the current density (J_{DS}) in PMOS is larger than that in NMOS. The PMOS with N_{stack} = 2 exhibits the largest β. This reverse behavior is due to the highest J_{DS} in PMOS with N_{stack} = 2 compared to NMOS. In addition, the difference of β when N_{stack} = 4~32 is small. This is because the difference in J_{DS} of PMOS is small, and thus the difference in thermal crosstalk is relatively insignificant.

Then, the temperature coefficient of V_{th} (η) is extracted, as shown in Figure 7. The η in NMOS under T_{amb} above T_{rt} rapidly decreases in the negative direction with N_{stack} first, and then the velocity of decrease gradually slows down [Figure 7a]. The η of NMOS with N_{stack} = 16 is the lowest. This is because the thermal crosstalk becomes severe; therefore, the impact of T_{amb} is mitigated. However, it increases when the N_{stack} grows to 32. This can be explained by the heat transport ability that the contact area between nanosheets and S/D regions gradually increases with N_{stack}, and then the enhanced thermal crosstalk effect is weakened. Therefore, the η with N_{stack} = 32 increases. The η in NMOS under T_{amb} below 0 °C rapidly decreases first, and then increases with N_{stack} = 16. The η in PMOS exhibits a similar trend compared with that in NMOS [Figure 7b]. However, the η value is larger.

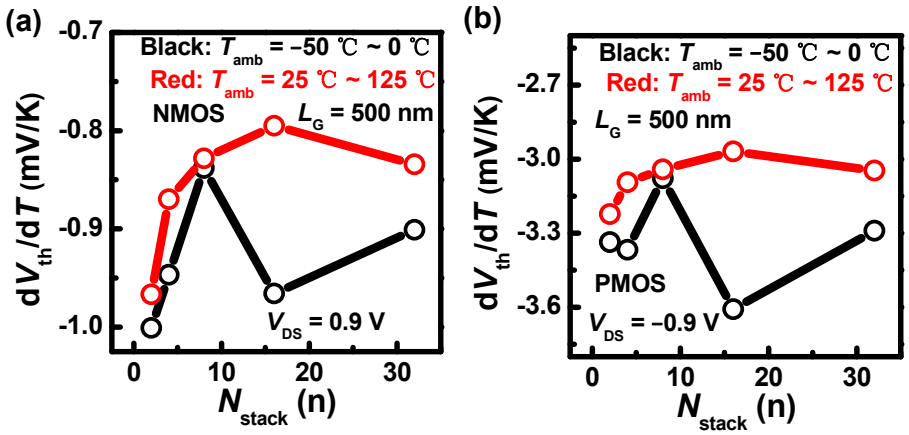

Figure 7. L_G = 500 nm, the temperature coefficients of V_{th} (η) with different N_{stack}s in (**a**) NMOS and (**b**) PMOS under different T_{amb} ranges.

The relation between the I_{DS} variation and the η based on the temperature-dependent backscattering model is also further analyzed. In the temperature-dependent backscattering model [30,31], the I_{DS} formula is defined using (1), and the linear relation of I_{DS} and T_{amb} is given using (2). Finally, the analytic expression for α concerning temperature is given using (3):

$$I_{DS} = WQ_{inj}v_{th}\left(\frac{\lambda_0/l_0}{2+\lambda_0/l_0}\right) \quad (1)$$

$$\Delta I_{DS}/I_{DS} = \alpha(T-(-50\ ^\circ\mathrm{C})) \quad (2)$$

$$\alpha = \left(\frac{1}{2}-\frac{4}{2+\lambda_0/l_0}\right)/298\ \mathrm{K} - \frac{\eta}{V_{GS}-V_{th0}} \quad (3)$$

In the equations, Q_{inj} is the inverse layer density near the source region; v_{th} is the thermal injection velocity at the thermal source; λ_0 is the mean-free path; l_0 is the critical distance when the carriers travel over a KT layer from the thermal source, where K and T are Boltzmann constant and temperature, respectively; and V_{th0} is the threshold voltage at referenced temperature −50 °C. The α includes the backscattering coefficient term and the voltage-dependence term. In Figure 7, the η in PMOS is higher than that in NMOS significantly, and thus the second term of (3) becomes larger. This leads to a greater degradation of the I_{DS} in PMOS compared to NMOS when T_{amb} increases, as shown in Figure 5.

As a special thermal phenomenon, the V_{ZTC} of PMOS is extracted in Figure 8. It is shown that the V_{ZTC} of PMOS decreases in the negative direction under T_{amb} above T_{rt} when N_{stack} grows from 4 to 32. The result can be explained by the coupling mechanism with the impact of the SHE and T_{amb}. As the N_{stack} increases, the current variation comes to balance at lower $|V_{GS}|$ due to the effect of V_{th} and mobility. However, the V_{ZTC} under T_{amb} below T_{rt} is 0.1 V higher than that under higher T_{amb} in the negative direction. This is because the SHE plays a lesser role in the case of T_{amb} below T_{rt}. Therefore, the effect of V_{th} and mobility compensate at a higher V_{GS} for the lower T_{amb}. The investigation of V_{ZTC} is useful to explore the working voltage in real applications.

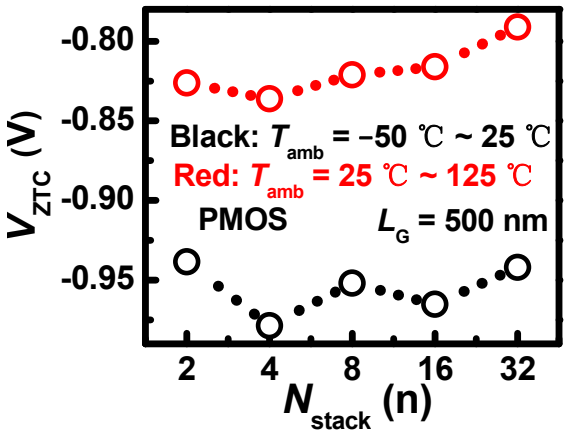

Figure 8. L_G = 500 nm, the V_{ZTC} of PMOS with different N_{stack} under T_{amb} = −50–25 °C range and T_{amb} = 25–125 °C range.

3.2. Electrothermal Performance of Different Gate Lengths with Different N_{stack}s under the Impact of T_{amb}

To explore the geometry effect, we further analyze the impact of gate lengths on electrical performance with different N_{stack}s, as shown in Figure 9. As L_G increases, the degradation of I_{DS} becomes severe. This can be explained by the temperature-dependent backscattering model.

As the L_G increases, the channel potential decreases, and then l_0 increases. Thus, the first term of (3) declines. This is an inverse result with the I_{DS} degradation [Figure 9a]. Furthermore, the η is extracted, as shown in Figure 9b. The η increases in the negative direction as the L_G increases at V_{DS} = 0.9 V. Therefore, the I_{DS} degradation is the result of both terms. At the same time, when the N_{stack} increases at V_{DS} = 0.9 V, the devices with L_G = 30, 40 nm show that the η decreases in the negative direction first, then, increases, similar to the trend of devices with L_G = 500 nm. Remarkably, when V_{DS} = 0.9 V, the slope of η with N_{stack} located in the 8 and 16 range is negative first, and then positive when the L_G increases from 30 nm to 500 nm.

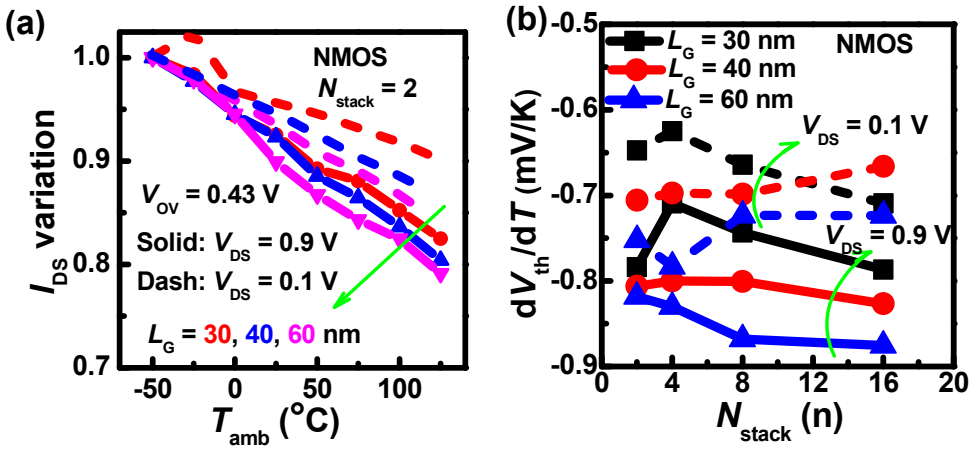

Figure 9. (**a**) I_{DS} variations with different gate lengths under the impact of T_{amb} relative to the I_{DS} at T_{amb} = −50 °C. (**b**) The temperature coefficients of V_{th} with different gate lengths when the N_{stack} increases.

In addition, the I_{DS} degradation in short gate length devices at V_{DS} = 0.9 V is higher than that at V_{DS} = 0.1 V. The difference gradually becomes larger with T_{amb}, and the device with L_G = 30 nm has the largest difference. Figure 9b shows that the η increases in the negative direction as the V_{DS} increases, and thus the second term of (3) becomes larger. Then, the λ_0/l_0 also increases with larger V_{DS}, and the first term of (3) becomes larger. Finally, the I_{DS} degradation is higher with larger V_{DS}.

3.3. Simulation Verification

The coupling mechanism with the impact of the SHE and T_{amb} is verified using the simulation method. To clarify the SHE clearly, the 16 nm gate length devices are simulated. The simulated devices are 3 nm node NSFETs, referring to [1]. The electrothermal parameters are set according to [32], where the L_G, W_{NS}, and T_{NS} are set to 16, 20, and 6 nm, respectively. The nanosheets adopt three layers of vertically stacked structure. All simulations are performed using Sentaurus TCAD tools [33]. The SHE is calculated with the thermodynamic model (TD model). Figure 10a shows that the I_{DS} with the SHE is lower than that without the SHE at larger V_{GS}. At V_{GS} = V_{DS} = 0.7 V, the on-state I_{DS} (I_{ON}) degradation with the SHE is lower than that without the SHE as T_{amb} increases, as shown in Figure 10b. The results indicate that the SHE weakened the impact of T_{amb}. As the N_{stack} increases, the η declines in the negative direction as shown in Figure 11. At the same time, the β decreases with N_{stack}. This further verifies that the coupling heat counteracts the partial effect of T_{amb}.

To further investigate thermal characteristics, the thermal resistance (R_{th}) and the maximum lattice temperature rise (ΔT_{max}) with respect to T_{amb} are extracted. The R_{th} is defined using (4), where total heat includes Joule heat, Peltier heat, Tompson heat, and recombination heat [34].

$$R_{th} = \Delta T_{max}/\text{total heat (K/}\mu\text{W)} \quad (4)$$

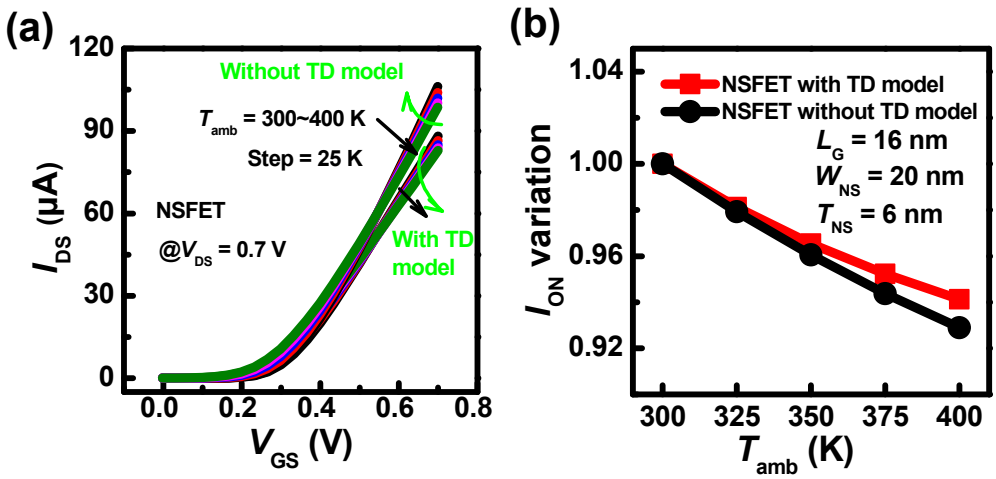

Figure 10. (**a**) The transfer characteristics of NSFET (N_{stack} = 1) with/without the SHE as the T_{amb} increases from 300 K to 400 K, (**b**) I_{DS} variations relative to the I_{DS} at T_{amb} = 300 K with/without the SHE when V_{GS} = V_{DS} = 0.7 V.

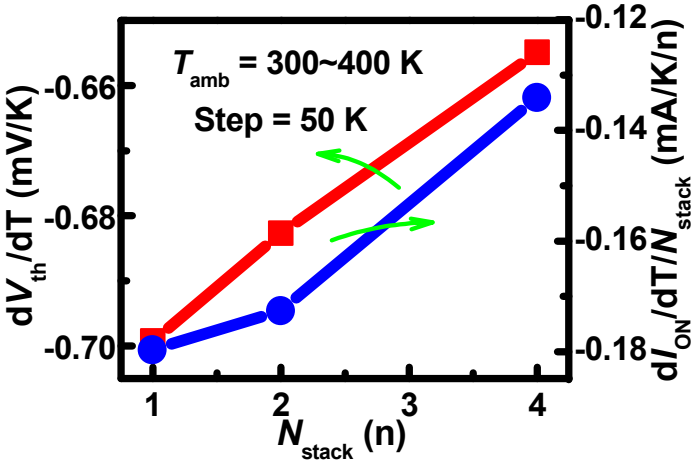

Figure 11. The temperature coefficients of V_{th} and the temperature coefficients of I_{DS} per stack with different N_{stack}s.

The ΔT_{max} and R_{th} in the devices with N_{stack} = 1 under T_{amb} = 300 K are 149 K and 2.59 K/μW, respectively, as shown in Figure 12. In Figure 12a, the ΔT_{max} decreases with T_{amb}. However, the lattice temperature gradually increases. This explains why I_{DS} with the SHE is lower at larger V_{GS} [Figure 10a]. At the same time, the ΔT_{max} increases when N_{stack} is from 1 to 2 first, and then has a minor variation when N_{stack} is from 2 to 4. This can be explained by the R_{th} variation with N_{stack}. In Figure 12b, the R_{th} per stack decreases with T_{amb}. This is because the ΔT_{max} reduction ratio exceeds the I_{ON} degradation. Then, the R_{th} per stack increases when N_{stack} is from 1 to 2, and then the rising speed increases when N_{stack} is from 2 to 4. This is induced by the coupling effect. The rising R_{th} causes an increase in lattice temperature, leading to a decrease in current density, eventually, the ΔT_{max} variation is low when N_{stack} is from 2 to 4 compared to that when N_{stack} is from 1 to 2. In addition, when the T_{amb} increases, the R_{th} decreases significantly in the devices with N_{stack} = 4 compared to that with N_{stack} = 1 and 2. This is because the coupling heat is more severe in the devices with N_{stack} = 4. These results verify that the SHE counteracts the partial effect of T_{amb}.

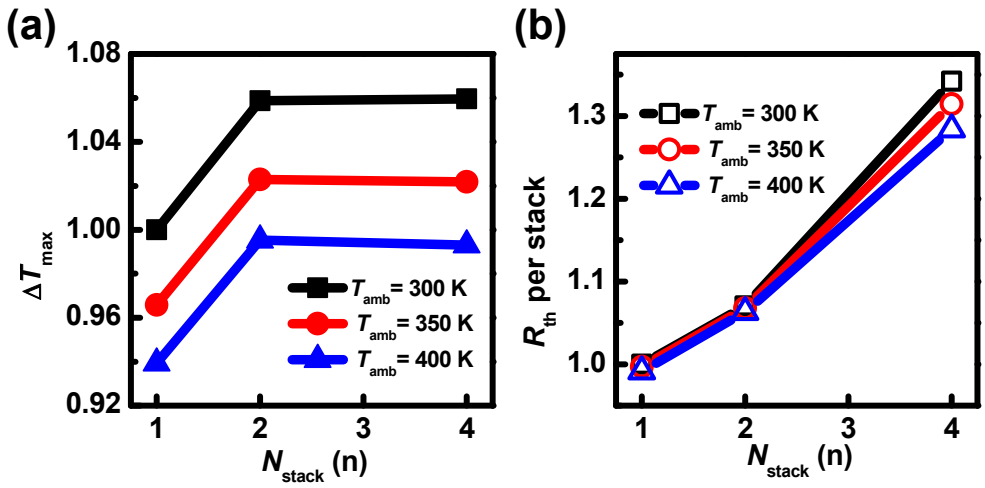

Figure 12. When V_{GS} = V_{DS} = 0.7 V, (**a**) ΔT_{max} and (**b**) R_{th} variations relative to the devices with N_{stack} = 1 under T_{amb} = 300 K.

4. Conclusions

In this paper, the impact of T_{amb} on the SHE in NSFET with different N_{stack}s is investigated. The results show that the NMOS with N_{stack} = 2 has the lowest I_{DS} degradation, and the I_{DS} degradation of PMOS with N_{stack} = 32 is lower than that with N_{stack} = 2. The results show that the I_{DS} degradation is lowest in the NMOS with N_{stack} = 2 and the PMOS with N_{stack} = 32 when the T_{amb} is at a high level. Due to the coupling mechanism with the impact of the SHE and T_{amb}, the η exhibits a decrease trend first, and then an increase trend with N_{stack} when the T_{amb} is higher than T_{rt}. Remarkably, the V_{ZTC} of PMOS decreases with N_{stack} > 4 in the negative direction when T_{amb} is higher than T_{rt}. Based on the backscattering theory, the I_{DS} degradation ratio decreases when the L_G becomes shorter. Meanwhile, the I_{DS} degradation decreases at V_{DS} = 0.1 V compared to that at V_{DS} = 0.9 V in short gate length devices. Finally, the simulations verify that the SHE counteracts the partial effect of T_{amb}. The work explores the electrothermal characteristics when NSFETs with different N_{stack}s work under the impact of T_{amb} and provides design guidelines for real applications.

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