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Review

Research Progress of High Dielectric Constant Zirconia-Based Materials for Gate Dielectric Application

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Abstract: The high dielectric constant ZrO_2, as one of the most promising gate dielectric materials for next generation semiconductor device, is expected to be introduced as a new high k dielectric layer to replace the traditional SiO_2 gate dielectric. The electrical properties of ZrO_2 films prepared by various deposition methods and the main methods to improve their electrical properties are introduced, including doping of nonmetal elements, metal doping design of pseudo-binary alloy system, new stacking structure, coupling with organic materials and utilization of crystalline ZrO_2 as well as optimization of low-temperature solution process. The applications of ZrO_2 and its composite thin film materials in metal oxide semiconductor field effect transistor (MOSFET) and thin film transistors (TFTs) with low power consumption and high performance are prospected.

Keywords: high dielectric constant; gate dielectric layer; zirconia; MOSFET; TFT

1. Introduction

Since the invention of transistors, SiO_2 has been the most practical choice of gate dielectric materials for field effect transistors. It has several significant advantages, such as high compatibility with silicon chip technology, uniform conformal oxide layer, high interface quality, good thermodynamic stability in contact with Si, etc., which has dominated the silicon microelectronics industry for decades. As the density of integrated circuit increases exponentially, the feature size of metal oxide semiconductor field effect transistor (MOSFET) decreases rapidly, resulting in the thickness of the SiO_2 layer presently used as the gate dielectric becoming thinner. When the feature size of the device continues to shrink to the nanoscale, the ultrathin SiO_2 with low dielectric constant (k = 3.9) has reached the physical limit and will eventually be hindered by the inability to reduce the oxide thickness to less than 1.3 nm [1,2]. For ultrathin SiO_2, the tunneling current caused by the quantum effect will seriously affect the operation of the device. The off-state leakage current will lead to the increase of device power consumption, and even be broken down because of the strong electric field, which makes the gate oxide lose the function of insulation and the device cannot work properly [3]. Therefore, relevant researchers have proposed the application of insulating gates with high dielectric constant (high-k) materials, which can increase their own physical thickness while ensuring the same channel control ability as ultrathin SiO_2

gate dielectrics, so as to restrain the large leakage current caused by the tunneling effect. As the core component of the flat panel display, the thin film transistor (TFT) device plays an important role in improving the performance of the flat panel display. The properties of the gate dielectric of the TFTs directly affect the performance of the devices. However, the performance of TFTs based on traditional SiO_2 gate dielectric materials cannot meet the requirements of the increasing development of flat panel display. Similar to the metal oxide semiconductor (MOS) devices, TFTs also suffer from tunneling current. Although nitride SiO_2 with improved dielectric constant has been used as the gate dielectric layer in TFTs, it is still unrealistic for continuous scaling in the long term. In order to obtain more compact performance and scaling size of TFTs, the gate dielectric with a high k value can be used in TFT devices to obtain higher on/off current ratio, lower threshold voltage and lower leakage current, which make it possible to drive TFT at low operating voltage [4,5].

High-k gate dielectric emerged into the market with Intel's new generation 45 nm microprocessors in 2007, in which silicon oxide-based insulator has been replaced by hafnium-based oxides [6]. In recent years, Samsung and Intel have announced the development of the next generation 3D transistors with high k dielectrics. This review focuses on high-k zirconium-based oxides, which are more abundant in nature also have many excellent properties similar to hafnium-based oxides.

2. Zr-Based High-k Dielectrics

A high k gate dielectric layer provides lower equivalent oxide thickness (EOT) and higher gate capacitance at the desired thickness. The EOT can be calculated as

$$\mathrm{EOT} = \frac{3.9}{K_{\mathrm{hiK}}} t_{\mathrm{hiK}} \quad (1)$$

Here 3.9 is the dielectric constant of SiO_2 and K_{hiK} is the dielectric constant of gate oxide and t_{hiK} is the thickness of the dielectric layer. Besides, it is vital that the potential barrier at conduction and the valence band offset for Si is greater than 1 eV in order to effectively reduce the leakage currents [7] (Figure 1). A sufficient band offset is required to block the additional current due to Schottky emission and thermal emission as well trap-assisted-tunneling [8]. Electrically active defects are undesirable, which give rise to electronic states in the band gap of the oxide. Charge trapped in defects scatter carriers in the channel and lowers the carrier mobility [7]. The transport performance of the device will be reduced due to impurity defects, remote interface phonons and interface roughness. Hence, it requires additional source−drain (V_{DS}) to source−gate (V_{G}) bias (voltage) as compensation to achieve a desired transistor current (I_{DS}), which in turn increases power consumption [9].

Alternative high-k gate dielectric materials have been investigated, such as HfO_2, ZrO_2, Al_2O_3, Y_2O_3 and La_2O_3. Among the high k gate dielectric materials studied at present, zirconia (ZrO_2) has an appropriate dielectric constant (theoretical value k = 25) with a wide band gap (5.8–7.8 eV) and good thermodynamic stability in direct contact with the Si substrate [3,10,11], which is almost similar as HfO_2. Nevertheless, ZrO_2 can be more easily stabilized in the form of cubic or tetragonal polymorphs with enhanced effective dielectric constant value compared with HfO_2 [12]. In addition, its high melting point (2680 °C), good oxidation resistance, high refractive index (2.15–2.22) [13] and low absorption from near ultraviolet (more than 240 m) to mid-infrared (below 8 μm) further highlight its technical importance [10,14,15]. It is considered to be one of the most promising high-k dielectric materials and has become a research hotspot. Hence, the purpose of this paper is to introduce the research progress of ZrO_2 and its composite materials as dielectric layers in recent years. Materials and electrical properties of ZrO_2 films prepared by several frequently used deposition methods are described. The main approaches to improve their electrical properties and application prospects in advanced MOSFET and TFT devices are introduced.

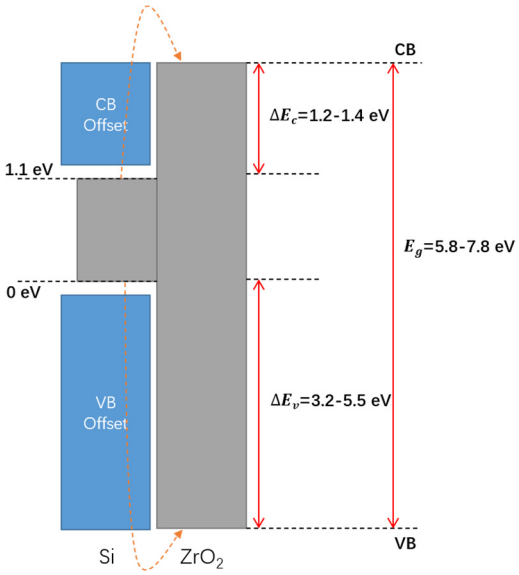

Figure 1. Schematic of bandgap and band offsets of ZrO_2 and carrier injection mechanism in its band states. CB conduction band, VB valence band.

3. ZrO_2 Thin Films Deposition

The preparation method of thin films is an important factor affecting the structure and properties of ZrO_2 gate dielectrics. ZrO_2 has three kinds of crystal variants, monoclinic crystal (m-ZrO_2, k = 20), tetragonal crystal (t-ZrO_2, k = 47) and cubic crystal (c-ZrO_2, k = 37), while the average k value of amorphous phase (a-ZrO_2) is 22 [10,15,16]. As thin films, ZrO_2 is usually deposited on the substrate in crystalline form. However, amorphous ZrO_2 films are preferred for microelectronic devices, because the grain boundaries and defect vacancies in crystalline ZrO_2 films can cause undesirable increased leakage current as good conductive channels. With the different deposition methods, the ZrO_2 thin films show different crystal phase structure, which leads to the heterogeneity of the k value with the film thickness, and changes the device performance. Different deposition temperatures and rates will also affect the properties of ZrO_2 films by affecting the surface roughness of the films. It can be seen that the improvement of film properties depends on the optimization of the deposition process.

Up to now, many deposition processes have been applied to the preparation of Zr-based high-k gate dielectrics, such as atomic layer deposition (ALD) [17], sol–gel process [18], chemical vapor deposition (CVD) [19], sputtering [20], molecular beam epitaxy (MBE) [21], electron beam evaporation (EBE) [22], pulsed laser deposition (PLD) [23] and so on. The following focused on several main preparation methods.

3.1. Atomic Layer Deposition

The ideal growth process for ALD is by alternately exposing the substrate surface to different precursors, which are strictly separated from each other in the gas phase [24]. The ALD deposition process can be used to achieve large area uniform, dense and non-pinhole thin films, meanwhile doping and interface modification is relatively facile. The size of the film grains can be reduced by a selection of proper precursor chemicals to reduce the processing temperature. It is widely used to precisely control the thickness of each cycle [25]. $ZrCl_4$ and H_2O are commonly used as reactants (Figure 2). However, hydrogen impurities are introduced from H_2O, which may combine with residual chlorine impurities in the film to form hydrogen chloride and corrode the main metal oxide structure. Therefore, the hydrogen free process is the first choice [26]. Hausmann et al. [27] used highly volatile zirconia alkylamide precursors to realize the preparation of ZrO_2 films by a smooth, pure and highly conformal low-temperature ALD process. Although it can be deposited at a relatively low temperature, ALD usually requires the equipment to achieve a high vacuum and a low deposition rate (0.43 Å/cycle).

At the same time, impurities (chlorine or iodine from the precursor) can be mixed into the film and reduce the dielectric properties of the film.

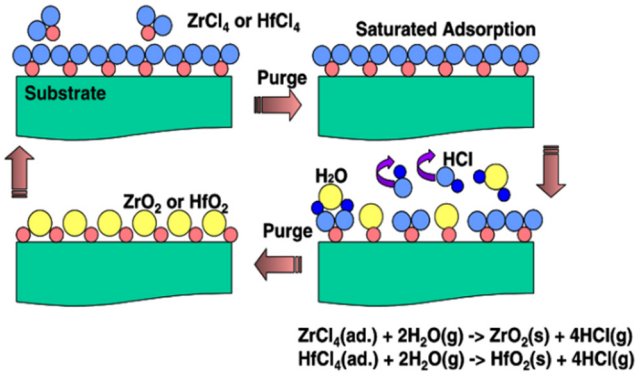

Figure 2. Schematic of the cyclic process of atomic layer deposition [7]. Reprinted with permission from [7]; 2015 Elsevier.

3.2. Physical Vapor Deposition

For physical vapor deposition (PVD), many methods have been developed to deposit thin films, which are mainly divided into two categories: vacuum evaporation coating and vacuum sputtering coating (as shown in Figure 3). The basic principle is to make the source material evaporate or eject from solid by heating or bombarding the target and finally impact (condense) on the substrate surface [28]. Among them, sputtering is the most commonly used deposition method for ZrO_2 thin films, by which a good quality of the prepared film, a firm combination with the substrate and a uniform thickness can be achieved [29]. However, sputtered oxides will have plasma-induced damage and difficult to deposited complex shape. The properties of sputtered films mainly depend on the deposition temperature, Ar/O_2 ratio, sputtering pressure and post-treatment conditions [30,31]. It was reported [32] that both the oxygen flow rate and post-annealing temperature affect the dielectric constant and surface roughness of the film. In recent years, high-power impulse magnetron sputtering (HiPIMS) systems have been used for high-rate reactive deposition of films (140 nm/min) as a result of the PVD techniques enhancement [13].

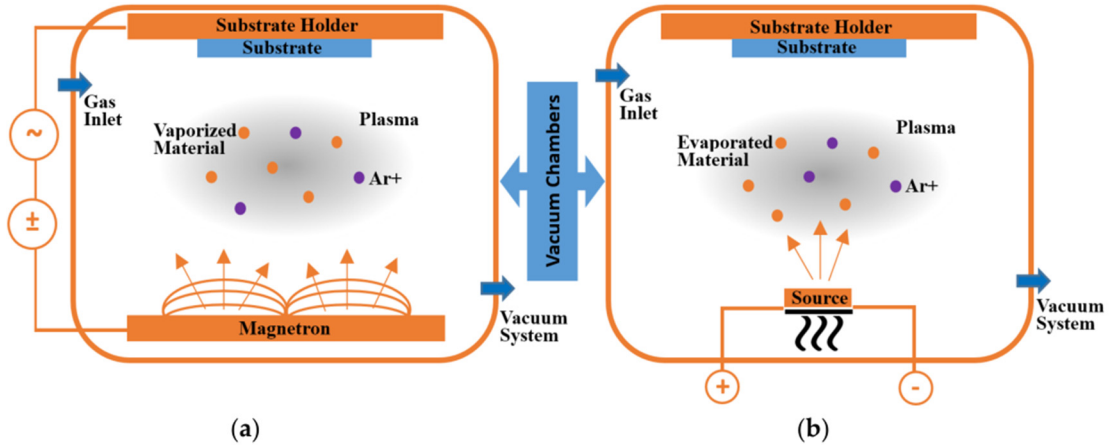

Figure 3. Schematic drawing of two conventional physical vapor deposition (PVD) processes: (**a**) sputtering and (**b**) evaporating using ionized argon (Ar+) gas [29].

3.3. Chemical Vapor Deposition

Chemical vapor deposition generally has a complex chemical system (Figure 4), which has a relatively low processing temperature and reasonably high deposition rate to produce uniform thin

films with good reproducibility and adhesion. CVD uses a volatile metal compound as a precursor, which is introduced into the chamber and oxidized during deposition onto the substrate. The chemical reactions of precursor species occur both in the gas phase and on the substrate [33]. Reactions can be promoted or initiated by heat (thermal CVD) [19], higher frequency radiation such as UV (photo-assisted CVD) [34] or a plasma (plasma-enhanced CVD) [35]. Moreover, it has capability to mass produce components that are uniformly coated with complex shapes and deposited with good conformal coverage. Furthermore, it has the ability to control the crystal structure, surface morphology and orientation of thin film through well controlled process parameters [33]. A variety of chemical precursors (i.e., halides, hydrides and organometallics) can be flexibly used to deposit target films. $ZrCl_4$ [33], zirconium acetylacetonate ($Zr(acac)_4$) [36] and $Zr(OC_4H_9)_4$ [37] are common precursors used as gaseous sources of zirconium to deposit ZrO_2 films. The oxidizing agent can be water vapor, oxygen or binary mixtures, such as H_2-O_2 or H_2-CO_2 [38]. However, for the above CVD process, the high temperature needed to prevent chlorine and carbon-based impurities from contamination usually leads to the formation of highly crystalline thin films with obvious surface roughness [38].

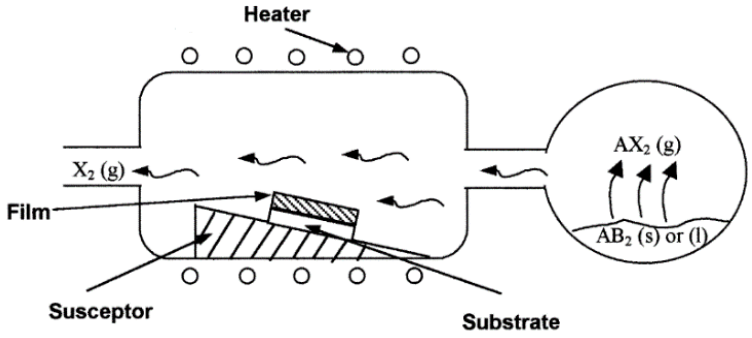

Figure 4. Schematic diagram of chemical vapor deposition (CVD) deposition system [38]. Reprinted with permission from [38]; 2003 Elsevier.

3.4. Sol–Gel Method

High quality oxide films can be obtained by traditional film preparation methods such as PVD, CVD and ALD, but the equipment requirements and cost of the vacuum treatment are high. Sol–gel chemistry is a method of synthesizing materials through phase transitions from a liquid precursor to a sol (colloidal suspension) and finally to a gel (a network structure) [39], such as spin coating, inkjet printing, spray pyrolysis, dip coating, gravure printing and so on [40]. There are three forms of reaction product, including sol, gel and nanoparticle that can be prepared by controlling the reaction temperature, reaction time, pH value and catalyst, as shown in Figure 5 [40]. By changing the concentration of the precursor solution and deposition period, sol–gel can control the thickness of films with the advantages of low cost, simplicity and high flexibility. Due to the high quality obtained under a mild condition, it is generally used to deposit the relatively thick high k dielectric layer of TFT [41]. It has also been reported that the sol–gel method was used to prepare ultrathin ZrO_2 films for MOSFET [42,43]. For the preparation of thin films by the solution method, attention should be paid to the molar ratio of the precursor solution and the condition of the post-annealing treatment [44], which are crucial to the properties of the films. Generally speaking, the properties of the films prepared by the solution method are slightly worse than those of other traditional methods such as ALD. However, sol–gel to prepare dense and uniform films that can meet the device requirements with the advantages mentioned above, which is of great significance for mass production in the future, making the solution method a promising film preparation method at present.

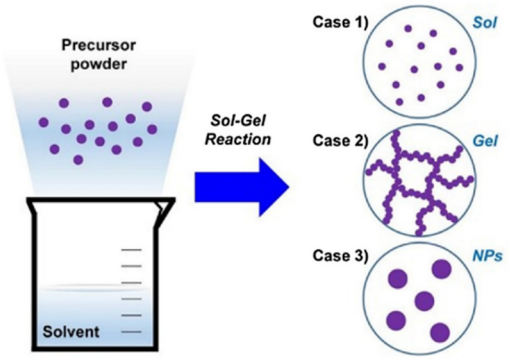

Figure 5. Typical sol–gel metal oxide reaction products [40]. Reprinted with permission from [40]; 2017 Elsevier.

4. Methods to Improve the Properties of ZrO_2 Films

Compared with the traditional SiO_2 layer, the low-temperature crystallization of ZrO_2 will lead to the formation of the polycrystalline structure in the annealing process and increase the leakage current. The high k dielectric has a high rate of oxygen diffusion, resulting in a low k interfacial layer that is formed inevitably between the silicon substrates in the O_2 ambient, which can increase the EOT. The interfacial properties are also much lower than that of the SiO_2 layer grown on the silicon substrate by thermal oxidation. Furthermore, the coulombic impurity scattering and surface optical phonon scattering cause the problem of carrier mobility loss that limits its application in the future complementary metal oxide semiconductor (CMOS) devices [45]. In this perspective, after the utilization of high dielectric ZrO_2 films, researchers optimized the properties of the derived films by doping other elements or compounds, including the design of pseudo-binary alloy systems by non-metallic elements and metal doping, adoption of new stacking structure, coupling with organic materials and utilization of crystalline ZrO_2 as well as improvement and optimization of the low-temperature solution process.

4.1. Doping of Non-Metallic Elements

Although ZrO_2 has good thermal stability in contact with Si, it is still difficult to prevent the formation of the SiO_2 interfacial layer with low *k* and high interface defects due to the diffusion of oxygen during deposition and heat treatment, which usually grows in the post-deposition annealing stage. In the early stage, it is found that the properties of the films have been improved through doping Si, N into ZrO_2. Lu et al. [46] studied the preparation of $(ZrO_2)_x(SiO_2)_{1-x}$ silicate (Zr–Si–O) thin films with different compositions on p-Si substrates by pulsed laser deposition. Compared with pure ZrO_2, Zr- silicate in direct contact with Si has higher crystallization temperature and superior thermal stability [47]. X-ray photoelectron spectroscopy (XPS) analysis shows that the $(ZrO_2)_{0.5}(SiO_2)_{0.5}$ film is still amorphous after rapid annealing in nitrogen at 800 °C for 60 s. Doping more Zr concentration in (Zr–Si–O) silicate film can obtain a higher dielectric constant. However, with the further increase of Zr concentration, obvious phase separation and precipitation of ZrO_2 will occur in Zr-silicate, which will worsen the interface between Si and Zr-silicate [48,49].

Many studies have been devoted to interface engineering solutions that introduce a high-quality oxide or nitride reaction barrier layer with very low defect density between high-k oxide and Si to separate the silicon channel from the dielectric [45,50] (Figure 6a). It can reduce the decrease of carrier mobility due to remote scattering, but at the cost of increasing the thickness of the equivalent oxide. In addition, nitrogen doping in the gate oxide layer is found to be beneficial to improving the thermodynamic properties, effectively reducing the interface layer thickness and leakage current density [35,51,52]. A further decrease of the diffusion coefficient of oxygen in the alloy, thus reduces

the crystallization rate significantly, so that the silicate can withstand the high temperature required by doping activation steps in the MOS process [53].

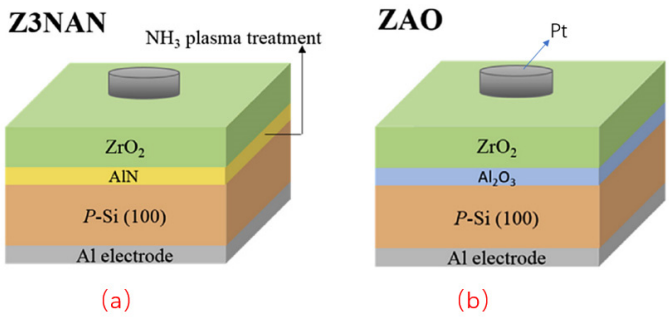

Figure 6. Schematic diagram of the (**a**) Z3NAN and (**b**) ZAO gate stacks [50]. Reprinted with permission from [50]; 2016 Elsevier.

4.2. Metal Elements Doping

The high bandgap (8.9 eV) of Al_2O_3 makes it have good thermodynamic stability with a moderate relative permittivity of 9. Incorporation of Al_2O_3 into ZrO_2 gate dielectrics combines the advantages of constituent dielectrics and markedly increases the crystallization temperature [54], which produce devices with improved performance and stability compared to the pure ZrO_2 film. In addition, the doping of small-size Al atoms into ZrO_2 that have greater densification can reduce the oxygen vacancy and smooth the gate dielectric interface [55,56]. Thereby, reducing the interface defects and gate leakage current as well as weakening the carrier mobility reduction effect caused by surface roughness scattering. Liu et al. [57] incorporated Al_2O_3 into ZrO_2 to optimize and adjust its electrical properties such as capacitance and leakage current. Our group also reported a high-k Zr–AlO_x dielectrics were fabricated by sol–gel spin coating at a low temperature annealing process, which can be applied to the preparation of high performance TFT [58]. By adjusting the *k* value of the gate dielectric from 11.3 to an appropriate value (8.1), a reasonable tradeoff is achieved between the gate screening effect on the Coulomb-impurity scattering and the surface optical phonon scattering [57], thus greatly improving the carrier mobility of the device. It has been reported that the mobility of $Zr_{0.5}Al_{0.5}O_y$ sample was 41% higher than that of the control sample (40.6 $cm^2/V{\cdot}s$) [57]. In reference [50,59], it is proposed that Al_2O_3 can be used as a transition layer to effectively block the diffusion of oxygen to the matrix and the interfacial reaction, so as to ensure the stability of the Zr-Al interface (Figure 6). Therefore, the quality of the gate dielectric layer can be effectively improved by using Al_2O_3 as the buffer layer or doping it into other high k materials.

In addition to the usual modification of doped Al, rare earth elements such as lanthanum (La) [60], gadolinium (Gd) [61], hafnium (Hf) [62] and yttrium (Y) [63] have also been studied to improve the performance of ZrO_2 films, which can effectively restrict the formation of low-k silicon oxides and obtain denser gate dielectric films with high-quality interfaces. The overall dielectric constant of pseudo-binary alloys may be lower than that of pure metal oxides, but this compromise is acceptable in order to improve stability. At present, the design of pseudo-binary alloy modified films by doping non-metal or metal elements is a mature way to improve the properties, which is the most promising structure for large-scale application in the industry.

4.3. Coupling with Organic Materials

In recent years, the development of organic–inorganic hybrid thin film materials for dielectric gate applications has aroused great interest of researchers [64]. In theory, organic materials for dielectric gate applications offer a smooth surface and good compatibility, but their low dielectric constant lead to low capacitance [9,65]. On the other hand, the high processing temperature of inorganic dielectric materials with high *k* values is not compatible with deposition on flexible plastic substrates required

in flexible electronics [66,67]. Accordingly, the appropriated incorporation of organic and inorganic phases in organic–inorganic hybrid materials, stalwartly bonded at the molecular level, is a new approach to develop dielectric materials with enhanced performance and broad application. However, it is still a challenge to deposit these materials as smooth films at temperatures compatible with flexible plastic substrates. Shang et al. [68] reported the application of bilayer poly (methyl methacrylate) (PMMA)/ZrO_2 gate dielectrics in copper phthalocyanine (CuPc) field effect transistor (FET; Figure 7a). Owing to the deposition of PMMA layers on ZrO_2, the dielectric leakage is reduced by an order of magnitude compared with single-layer ZrO_2, resulting in a high-quality interface between organic semiconductors and composite insulators. The device combines the advantages of polymer and high k inorganic materials to achieve high mobility and low threshold voltage. It is reported that the typical field-effect mobility of bilayer dielectric field-effect devices is 5.6×10^{-2} $cm^2/V{\cdot}s$ and the threshold voltage is 0.8 V [68].

In addition, there are reports on the application of ZrO_2 doped polymer modified thin films in the dielectric gate of metal oxide thin film transistor (MOTFT) [69,70] (Figure 7b) and organic thin film transistor (OTFT) [67,71,72] (Figure 7c). Among them, many of these hybrid materials can be obtained by the sol–gel method, which is a solution, low-temperature process compatible with deposition on large-area substrates. The performance of these hybrid films, including interface quality and dielectric properties, can be adjusted by controlling the content of organic and inorganic components. It can be seen that Zr-based organic hybrid films have great potential applications in a variety of large area printing flexible electronic applications such as displays, sensors and electronic bar codes [66,73].

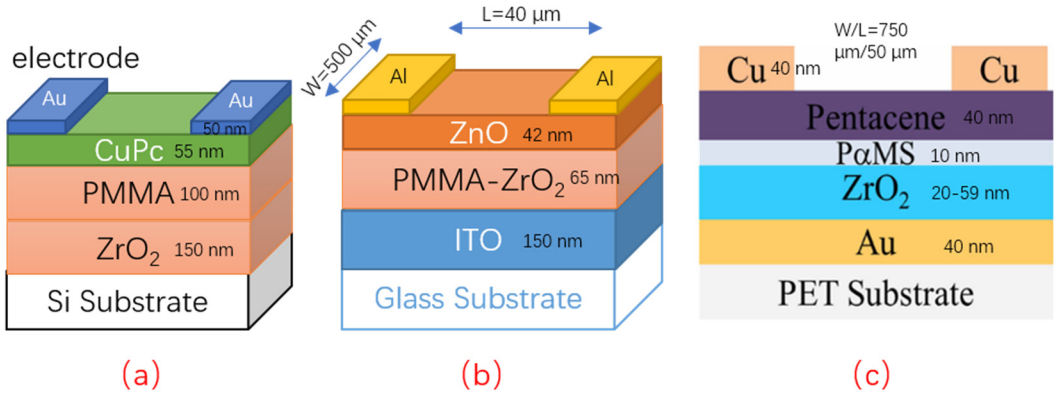

Figure 7. (**a**) Schematic structure and dimensions of the Organic Field Effect Transistors (OFET) with the PMMA/ZrO_2 bilayer as dielectrics [68]; (**b**) Schematic structure and dimensions of the metal oxide thin film transistor (MOTFT) with a ZnO semiconductor layer and PMMA−ZrO_2 hybrid films as gate dielectric [69]; (**c**) Schematic structure and dimensions of the organic thin film transistor (OTFT) with the PαMS/ZrO_2 bilayer as dielectrics [72].

4.4. Crystalline ZrO_2 Dielectric

Recently, crystalline ZrO_2 has attracted considerable attention due to the tetragonal (47) and cubic (37) phase of ZrO_2 having a much higher *k* value than amorphous ZrO_2. However, the grain boundaries may serve as the leakage current paths, which will cause a dramatic leakage current in the dielectric gate layer application. Moreover, the tetragonal and cubic phase of ZrO_2 are only stable in bulk form above 1170 and 2297 °C respectively, which is not suitable for ultra-large-scale integration (ULSI) technology [15,74]. Hereby, reducing the film thickness or grain size or doping impurities such as Si, Ge and La [14,74,75] into the lattice had been exploited to decrease their stable temperatures. The tetragonal/cubic phase of ZrO_2 can be formed by post-metallization annealing (PMA) at a low temperature of 450 °C to provide a high gate oxide dielectric constant [76]. Ge-induced stable ZrO_2 crystals can be formed by co-evaporation of Ge and ZrO_2 or thermally diffused into ZrO_2 films by Ge substrates, thus stabilizing the high-k tetragonal phase [75,77–79]. What is more, as a channel

material, Ge has many advantages, such as higher carrier mobility than traditional Si and compatibility with the Si process. In addition, some research [76,80,81] has reported that nitriding can effectively passivate grain boundaries and reduce leakage current density. On the other hand, the thermal stability is enhanced through post-deposition annealing (PDA) treatment at 800 °C (Figure 8) and the hysteresis problem affecting the threshold voltage stability is reduced to the maximum extent.

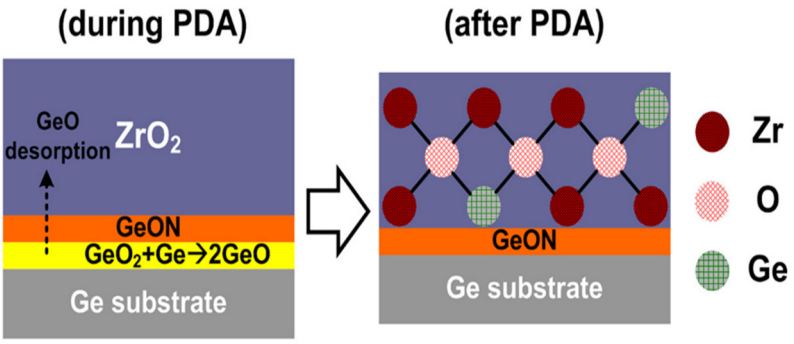

Figure 8. Nitriding treatment and GeO_2 thermal decomposition into the ZrO_2 layer to form a stable crystal state [78]. Reprinted from [78]; 2013 AIP Publishing.

Even so, how to reduce the leakage current density of the single crystalline ZrO_2 layer is still a great challenge. At present, many studies will utilize novel gate stack structures such as t-ZrO_2/Al_2O_3 [80], ZrO_2/Ge/ZrO_2/Y_2O_3 [75] or the crystallized ZrO_2/AlN [50] buffer layer to further reduce the leakage current and density of interface states. As a gate dielectric layer, crystalline ZrO_2 can significantly increase the carrier mobility and the transistor driving current with reduction of the equivalent capacitor thickness (CET) because of a high *k* value. The results demonstrate that the utility of crystalline ZrO_2 is a favorable technique to improve the electrical properties and gate dielectric performances. It opens up a new way for the development of possible applications as charge storage capacitors for active matrix display devices with high-k dielectric.

4.5. Low-Temperature Solution Process

The sol−gel process has been widely reported as a result of low processing consumption, simple and flexible operation. However, the common disadvantage of the solution process is that a higher annealing temperature (≥400 °C) is required to remove most of the solvents and impurities, and convert the precursors into dense oxide films [82] (Figure 9). The high-temperature annealing hinders the application of the plastic substrate in flexible electronic devices, and causes huge energy consumption. In recent years, due to the increasing demand for a low thermal budget and flexible electronic devices, the research on the low temperature annealing solution process has aroused extensive interest. Approaches including the sol–gel on chip process [83], high pressure annealing [84], aqueous solution [85], combustion [86,87], the light wave/microwave annealing method [88] and ultraviolet ozone irradiation [89,90] have been used to effectively reduce the processing temperature of oxide films prepared by the solution process. Our group developed an ink system for drop-on-demand (DOD) printing high performance ZrO_2 film at a low temperature [91]. In particular, ultraviolet ozone (UVO) can be employed to prepare oxide TFTs in fully solution-processed at room temperature [92]. ZrO_2 films were prepared by spin coating of zirconium acetylacetonate (ZrAcAc) precursors with high UV absorption (Figure 10). The report indicated that the film's surface became significantly smooth and led to a reduction of the oxygen vacancy defects. Moreover, the analysis revealed it could effectively facilitate the formation of metal-oxygen (M–O) bonds with high k dielectric properties (k = 13). It is found that the leakage current with UVO treatment at room temperature was significantly lower than that of ZrO_2 films treated by annealing at high temperature (Figure 11). The development of low temperature solution technology has obtained the advantages of energy saving, simplicity and low

cost compared with the traditional vacuum process. It has a great application prospect in the facile low-temperature solution production of high-quality flexible oxide electronic devices.

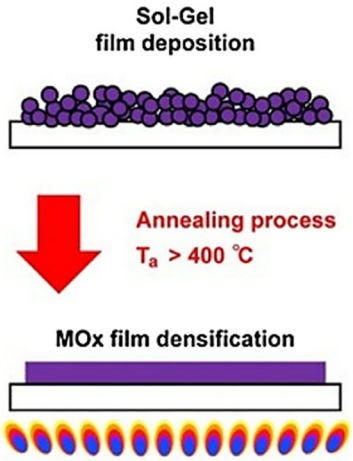

Figure 9. A schematic of densifying a sol–gel metal oxide film from as-spun xerogel via high-temperature thermal annealing [40]. Reprinted with permission from [40]; 2017 Elsevier.

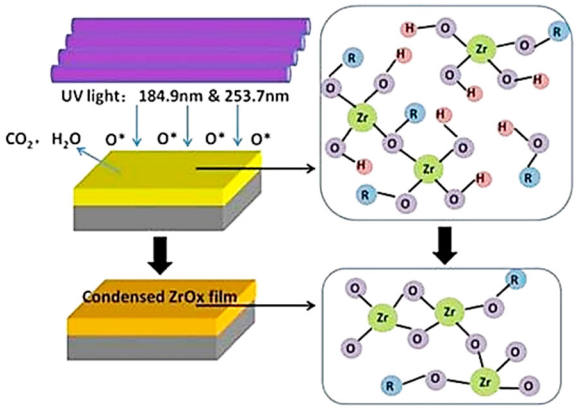

Figure 10. Schematic diagram of ZrAcAc sol–gel transformation mechanism under ultraviolet ozone (UVO) irradiation [92]. Reprinted with permission from [92]; 2017 Elsevier.

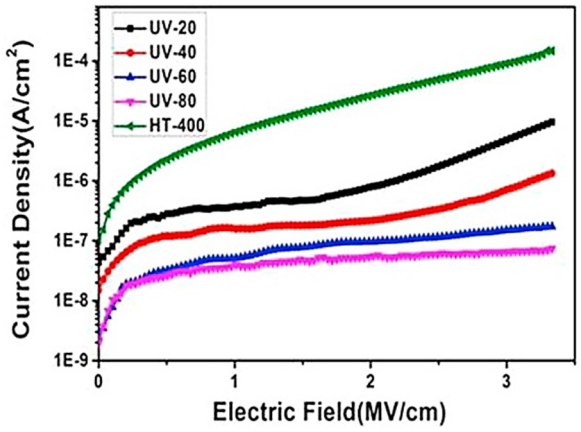

Figure 11. Comparison of leakage current in ZrO_2 films after annealing by UVO and high-temperature (HT) [92]. Reprinted with permission from [92]; 2017 Elsevier.

Table 1 shows the comparison of the properties of ZrO_2 and its optimized composite materials mentioned in this paper.

Table 1. Comparison of relevant properties of ZrO_2 and its composite material.

Material Structure	Leakage Current Density (A/cm^2)	EOT (nm)	Carrier Mobility ($cm^2/V{\cdot}s$)	Density of States ($eV^{-1}cm^{-2}$)	*k* Value	Threshold Voltage (V)	Deposition Method	Application	Ref.
ZrO_2	–	–	28	–	25	3.2	RF magnetron sputtering	TFT	[4]
$N_2 + ZrO_2$	10^{-9}~10^{-8}	–	22.5	7.06×10^{12}		0.1	EBE and PECVD	TFT	[35]
$HfZrO_2$	3.6×10^{-5}	1.6~1.8	–	–	29~37	–	ALD	MIM	[62]
ZrO_2/Si-N	-	1.6	–	5×10^{12}	11.5	–	ALD	MIM	[53]
ZrAlO	6.2×10^{-7}	19.3	40.6	3.30×10^{12}	19.67	0.71	ALD	FET	[57]
t-ZrO_2/Al_2O_3	3.43×10^{-5}	1.09	–	3.35×10^{11}	21	–	Remote plasma ALD	MOS	[81]
PMMA-ZrO_2	10^{-6}~10^{-5}	–	0.48	-	4~12	3.3	Sol–Gel	TFT	[69]
Gd-ZrO_2	1.8×10^{-6}	4.9	–	1.34×10^{11}	10.3	–	Sol–Gel	MOS	[61]
$ZrHfO_2$-PMMA	7.7×10^{-6}	–	2.45	–	7.2~9.4	1.2	Sol–Gel	TFT	[66]
PMMA-ZrO_2	3×10^{-9}	–	5.7×10^{-2}	7.5×10^{10}	–	0.8	EBE and Sol–Gel	OFET	[68]
Y-ZrO_2	1.14×10^{-7}	0.67	68	1.2×10^{12}	30~33	–	co-sputtering	FET	[63]

5. Conclusions

In summary, ZrO_2 is one of the most promising materials to replace traditional SiO_2 and Si_3N_4 dielectric layers due to its notably properties highlighting a (i) high dielectric constant, (ii) the capability of the room temperature process, (iii) high melting point, (iv) large band gap offset and (v) good thermal stability of contact with silicon and process compatibility. ZrO_2 and its optimized composite materials prepared by various deposition methods not only effectively reduced the leakage current and threshold voltage of the device, but also improved the on-to-off ratio of the device and the ability of the gate to control the current between the source and drain. It has great potential in CMOS and TFT devices and metal-insulator-metal (MIM) capacitor applications. However, there are still a series of problems to be solved to make it really practical. For example, the gate depletion effect of poly-Si will form a high resistance gate, and the interface mismatch between poly-Si gate and high k dielectric lead to the decrease of carrier mobility. The interface states caused by high k dielectric material will also cause a Fermi level pinning phenomenon, which leads to the shift of the gate voltage threshold and shows the need to find a suitable metal gate to replace the polysilicon gate electrode [24]. At the same time, the optimized and improved Zr-based films should conform to the trend of flexible, low-cost, low-temperature and printable electronic applications in the future.

The challenge that the new generation of scientists and engineers will face is not only to optimize and improve these new materials in the laboratory, but also to merge with the mature silicon process and Zr-based gate dielectric films in order to meet the requirements of the semiconductor industry. It can be expected that in the near future, the improved Zr-based and its composite gate dielectric films as high-k materials will first enter a practical stage in high-performance TFTs, and then will be used as the next generation of high-k materials in MOSFETs with the development and maturity of related technologies.

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