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Comparison of Cobalt Integration with Various Dielectric Materials under Thermal and Electrical Stress

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Abstract: Cobalt (Co) is proposed to replace copper (Cu) as a conductor in the back-end-of-line (BEOL) interconnects of integrated circuits. In this study, the electric characteristics and reliability of the integration of Co with various dielectric films (SiO_2, dense, and porous low-*k* SiOCH films) under thermal and electrical stress were compared. Thermal annealing repaired sputtering-Co-deposition-induced damage to the dielectric film but reduced the breakdown field and time-dependence-dielectric-breakdown (TDDB) times due to the diffusion of Co atoms. After annealing, the SiO_2 film had the largest reductions in the breakdown field, TDDB failure time, and electric field acceleration factor, indicating that the diffusion of Co atoms dominates in the oxygen-rich surface. Under electrical stress, the drift of Co atoms favors the porous low-*k* film with the assistance of porosity. As a result, a barrier is required for Co metallization. To achieve barrier-free or barrier-less processing in Co metallization, the dense low-*k* film is the best option to integrate with Co.

Keywords: cobalt; SiO_2; low dielectric constant; porous low-*k*; thermal stress; electrical stress; metal drift

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1. Introduction

As the feature size of integrated circuits (ICs) is continuously scaling down, the resistance–capacitance (RC) delay of the back-end-of-line (BEOL) interconnects has become a limiting factor in the performance of ICs [1,2]. As a result, copper (Cu) and low dielectric constant (low-*k*) materials have replaced the traditional use of Al and SiO_2 as conductor and insulator materials in the BEOL interconnects, since the development of the 0.18 μm technology node, in order to reduce the RC delay [3–5].

The continuous scaling of the dimensions of BEOL interconnects with the technology node resulted in an increase in the capacitance, thus requiring further reduction to the dielectric constant (*k*) of low-*k* films. The reduction of the *k* of low-*k* film could be achieved by introducing porosity into the film; the result of this is called the porous low-*k* film. On the other hand, the porous low-*k* films have weak mechanical, thermal, and electrical characteristics, thereby leading to more processing challenges and the degradation of electric performance and reliability as they are integrated into BEOL interconnects [4–7].

As the technology node advances to 10 nm and below, a dramatic increase in the resistivity of Cu conductors in the scaling interconnects has become a critical issue [8–10]. Additionally, a barrier against Cu migration would occupy a larger cross-sectional area of the metal line as the dimension of the BEOL interconnects is continuously scaling down [11,12]. Such barriers have a high resistivity, further increasing the line resistance and RC delay.

To mitigate the increase in line resistance due to the scaling effect, an alternative conductor in the BEOL interconnects to substitute Cu has been proposed. The candidates

to replace Cu must have lower product values of bulk resistivity (ρ_0) and electron mean free path (λ) than Cu in order to exhibit higher conductivity in the limit of a small line width [13–16]. Based on this rule, the potential candidates are Mo, Co, Ni, and Ru [15–18]. Among these potential candidates, Co has gained more attention because its resistivity is less sensitive to scaling [19]. Additionally, Co is expected to have better resistance against electromigration than Cu because it has a higher melting temperature (1495 °C) than Cu (1085 °C) [17,18]. Moreover, Co does not require high-resistivity nucleation layers and its grain growth can be achieved by annealing at a low temperature [16]. Last and most importantly, the migration of Co is weaker than that of Cu, thereby achieving barrier-less or barrier-free processing for Co metallization. This provides an acceptable line- or via-resistance [19,20]. Most studies indicated that Co would drift under electrical stress, with the magnitude being less than Cu; however, the integration dielectric film used was SiO_2 film [21,22]. On the other hand, studies related to Co/low-k integration are limited.

Here, various dielectric films, including SiO_2, dense, and porous low-*k* dielectric films, were integrated with Co in this study. After being subjected to thermal and electrical stress, the electrical characteristics and reliability of the integration schemes were characterized and compared.

2. Experimental Details

2.1. Sample Preparation

In this study, SiO_2, dense, and porous low-*k* dielectric films were deposited on *p*-type (100) silicon substrates as the starting materials. SiO_2 films were grown by using a dry oxidation method in a furnace at 1100 °C. Both the dense and porous low-*k* dielectric films were SiOCH materials, which were deposited in a plasma-enhanced chemical vapor deposition (PECVD) reactor (Applied Material Corp. producer system, Santa Clara, CA, USA). Diethoxymethylsilane (DEMS) and oxygen (O_2) were used as the matrix precursors during the deposition. For the production of porous low-*k* films, alpha-terpinene (ATRP), as a porogen precursor, was also introduced into the reactor. The organic porogen in the low-*k* film was then removed by performing UV thermal-assisted curing after deposition. This led to the formation of pores in the film. Details about the deposition conditions for the production of dense and porous low-*k* films can be found elsewhere [23,24]. The properties of SiO_2, dense, and porous low-*k* dielectric films are listed in Table 1. The thickness of all studied films was controlled at 130 ± 10 nm. The dielectric constant (*k*) values were 4.02 ± 0.03, 3.02 ± 0.05, and 2.56 ± 0.08 for the pristine SiO_2, dense, and porous low-*k* dielectric films, as determined by the Hg probe *C*–*V* measurement (5100 CV system).

Table 1. Properties of SiO_2, dense, and porous low-*k* dielectric films ued in this study.

Sample	Deposition Method	Precursor	UV Curing	Dielectric Constant (k)	Leakage Current Density at 1 MV/cm ($\times 10^{-12}$ A/cm^2)	Breakdown Filed at 25 °C (MV/cm)	Porosity (%)	Pore Size (nm)
SiO_2	Dry oxidation	O_2	No	4.02 ± 0.03	2.46 ± 0.35	9.98 ± 0.15	N/D	N/D
Dense low-*k*	PECVD	DEMS + O_2	No	3.02 ± 0.05	5.66 ± 0.7	8.56 ±0.16	N/D	N/D
Porous low-*k*	PECVD	DEMS + O_2 + ATRP	Yes	2.56 ± 0.08	2.69 ± 0.33	6.67 ± 0.30	15	1.35

N/D = not detected.

Following this, metal-insulator-silicon (MIS; Co/dielectric/Si) capacitors for electrical and reliability measurements were fabricated. Co was sputtering deposited onto a dielectric film through a showdown mask in the direct current (DC) magnetron sputtering system at room temperature. The base pressure in the sputtering chamber was 4.0×10^{-4} Pa. During the deposition, the working pressure was 0.53 Pa, with the introduction of Ar at a gas flow rate of 20 sccm. The DC power was kept at 50 W. The deposition thickness of Co was approximately 100 nm. The formation Co dot was square, with an area of

9.0×10^{-4} cm^2. To evaluate electrical and reliability characteristics under thermal stress, parts of the fabricated MIS capacitors were annealed in N_2 environments at 425 °C for 2 h.

2.2. Sample Characterization

The thickness of the studied films was determined by using an optical-probe system with an ellipsometer (Film TekTM 3000SE, Keithley, 6517A, Austin, TX, USA). Electrical and reliability characteristics, including capacitance–voltage (*C*–*V*), current–voltage (*I*–*V*), and time-dependence-dielectric-breakdown (TDDB) were conducted on the fabricated MIS capacitors. The *C*–*V* measurement was operated at a frequency of 1 MHz by using a semiconductor parameter analyzer (HP4280A). The *k* value of a dielectric film and the flat-band voltages (V_{fb}) in the Co-gate MIS capacitor can be determined from the measured *C*-*V* curves. The *I*–*V* and TDDB characteristics were measured by using an electrometer (Keithley 6517A). The *I*–*V* measurements were performed using a ramp-voltage-sweep (RVS) method to measure the leakage current and breakdown voltage (field). The TDDB test was used to evaluate the long-term reliability of a dielectric film. During the TDDB test, a constant electric field was continuously applied and the leakage current was monitored with stressing time. As the leakage current suddenly increased by at least three orders of magnitude, a dielectric breakdown occurred; the stressing time was defined as the TDDC failure time. To evaluate the drift of Co into the dielectric film under electrical stress, an electric field at positive polarity was applied to the Co-gate of the MIS capacitors for 100 s. After being subjected to electrical stress, the samples were measured for *I*–*V* characteristics. The measurements were conducted at room temperature (25 °C). To prevent moisture absorption and metal gate oxidation, a nitrogen gas purge was performed during the measurements.

3. Results and Discussion

Figure 1a–c plot the double direction *C*–*V* curves of the Co-gate MIS capacitors with SiO_2, dense, and porous low-*k* dielectric films, respectively, before and after annealing at 425 °C for 2 h. For all samples, the measured capacitances were accumulation, transition, and depletion capacitances in order when voltage swept from negative to positive, which are typical *p*-type MIS *C*–*V* characteristics. Double-direction *C*–*V* curves were measured by sweeping voltage either from accumulation mode to inversion mode (forward voltage sweep; FVS) or from inversion mode to accumulation mode (reverse voltage sweep; RVS). Under either a FVS or RVS measurement, the measured accumulation capacitances were identical for all MIS capacitors with various dielectric films. After annealing, the accumulation capacitances decreased for all samples. In the as-fabricated and annealed stages, the accumulation capacitance followed the order: SiO_2 > dense > porous low-*k*.

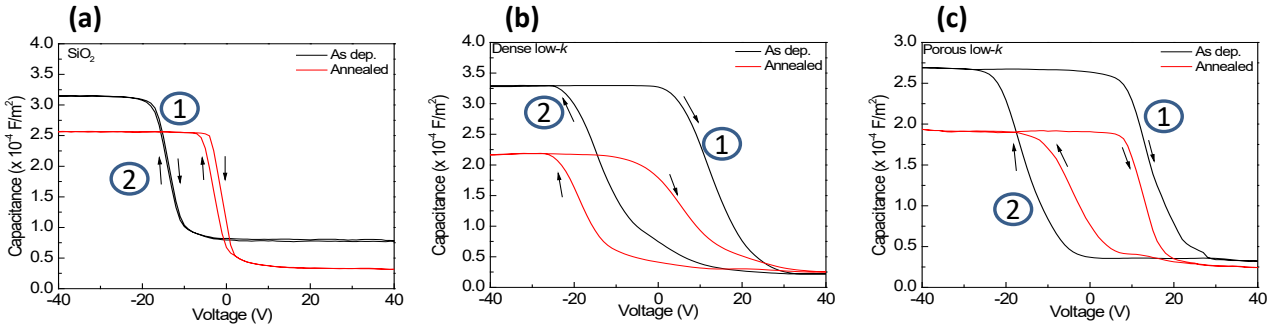

Figure 1. *C*−*V* curves of Co-gate MIS capacitors before and after annealing: (**a**) SiO_2; (**b**) dense low-*k*; (**c**) porous low-*k* films. (①: FVS; ②: RVS).

The dielectric constant (*k*) of a dielectric film in the MIS capacitor can be determined through the measured accumulation capacitance (*C*) by using the expression of $k = Cd/\varepsilon_0 A$. Here, ε_o is absolute capacitive in a vacuum (8.85×10^{-12} F/m), *d* is film thickness, and

A is the area of the MIS capacitor. The pristine k values were 4.02 ± 0.03, 3.02 ± 0.05, and 2.56 ± 0.08 for the pristine SiO_2, dense, and porous low-k dielectric films. As Co was integrated with these dielectric films, the k values increased to 4.51 ± 0.03, 4.34 ± 0.08, and 3.70 ± 0.08 for the SiO_2, dense, and porous low-k films, respectively. An increased k value is believed to be caused by the sputtering deposition of Co metal. During the sputtering deposition of Co, plasma-generated active species damage the dielectric film, thereby increasing the capacitance and k value. [25,26]. After annealing, all accumulation capacitances decreased, thus reducing the k values to 4.10 ± 0.02, 3.24 ± 0.06, and 2.97 ± 0.05 for SiO_2, dense, and porous low-k dielectric films, respectively. This result suggests that sputtering-deposition-induced damage on a dielectric film can be repaired by annealing. To evaluate the damage effect induced by sputtering deposition and the repair efficiency caused by annealing, the relative k values (relative to the k value of the pristine film) for SiO_2, dense, and porous low-k films before and after annealing were plotted in Figure 2. As shown, the relative k values were higher than 1.0 for all as-fabricated and annealed films, revealing that the capacitance would inevitably increase as Co is integrated with a dielectric film. After Co deposition by sputtering deposition, porous low-k films had the largest relative k values and SiO_2 films had the smallest relative k values, representing more plasma-induced damage on the porous low-k films and less plasma-induced damage on the SiO_2 films. The degree of plasma-induced damage is strongly dependent on the structure of a dielectric film [27]. After annealing, the relative k values reduced, demonstrating that the Co-sputtering-deposition-induced damage can be repaired by annealing. However, the k values were still higher than the pristine values, implying that such damage cannot be repaired completely. Similarly, the porous low-k film had the largest value (1.16), suggesting that the recovery of plasma-induced damage by annealing is not effective for the porous low-k film compared to the SiO_2 and dense low-k films.

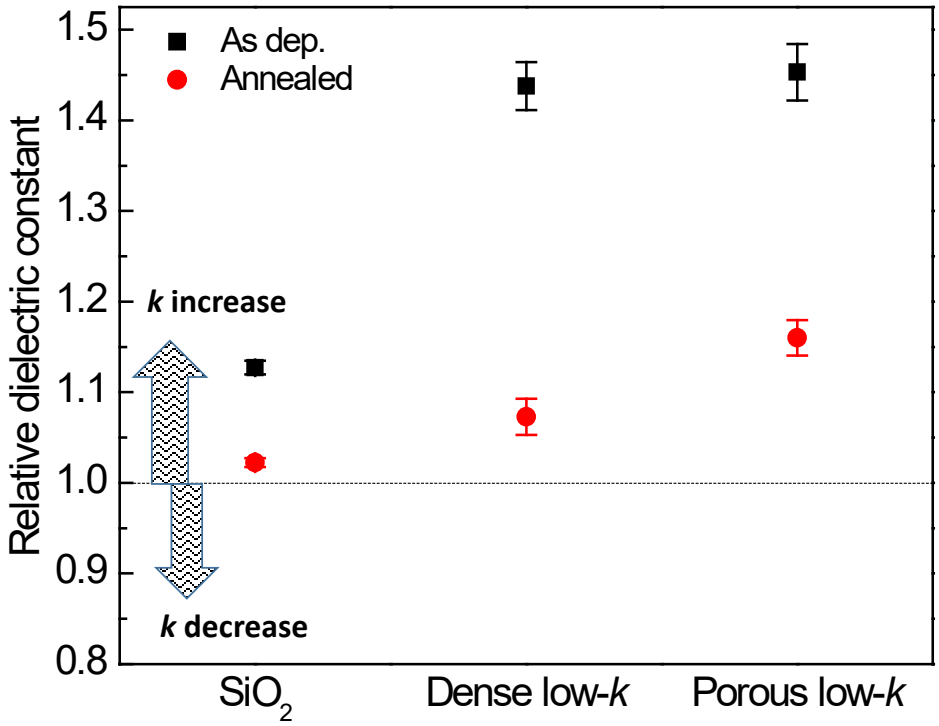

Figure 2. Relative dielectric constant of SiO_2, dense, and porous low-k dielectric films in Co-gate MIS capacitors before and after annealing.

Turning attention to the $C-V$ curves shown in Figure 1, the flat-band voltages (V_{fb}) and the hysteresis (e.g., the difference in V_{fb} between FVS and RVS $C-V$ curves) can be determined. In the ideal MIS capacitor, the V_{fb} value is the difference in work function

between the metals and the Si if the dielectric insulator has no charges. Theoretically, the work functions of *p*-type Si and Co are 5.25 eV and 5.00 eV, respectively [28]. As a result, the V_{fb} value of the Co-gate MIS capacitor is estimated to be −0.25 eV. In a real case, the thermally grown SiO_2 film reportedly has positive charges in the order of 10^{10}–10^{11} cm^{-2}, corresponding to the negative V_{fb} shift of approximately 0.01–0.1 V [29]. As a result, the V_{fb} value was −0.25 −−0.35 V. In this study, for as-deposited Co-gate MIS capacitors with SiO_2 film, the V_{fb} value was determined to be −13.68 V and no hysteresis was observed, revealing that positive charges are introduced into the SiO_2 film during the fabrication of the Co-gate MIS capacitor. After annealing, the V_{fb} value reduced to −1.0~−2.5 V but a hysteresis was detected. It is believed that sputtering-deposition-induced charges during Co deposition can be removed by annealing [30], making the V_{fb} value return back to approaching the ideal value. For the origin of the hysteresis, (a) electron (e^-) trapping; (b) hole (h^+) or positive charges trapping; (c) mobile charges; and (d) as-grown traps are the possible sources [31]. For Co-gate MIS capacitors with SiO_2 film, the V_{fb} shifted toward a negative voltage direction after annealing. As a result, the hysteresis increased to 2.52 V after annealing, which is likely to be caused by positive charges trapping (e.g., Co ions).

For both dense and porous low-*k* films, donor-like traps were reportedly generated in the bulk film during the deposition [31]. Additionally, charges were introduced into the dielectric film during the fabrication of the Co-gate MIS capacitor. Hence, a larger V_{fb} hysteresis was expected. After annealing, Co-sputtering-deposition-induced charges can be partially removed and Co ions may diffuse into the films. Hence, the V_{fb} hysteresis becomes more complex. Therefore, detailed research to verify the mechanism is required. Figure 3 compares the hysteresis of Co-gate MIS capacitors with SiO_2, dense, and porous low-*k* dielectric films before and after annealing. For dense and porous low-*k* films, the hysteresis reduced while the hysteresis increased for SiO_2 films. This suggests that the diffusion of Co ions was in progress within the SiO_2 film during annealing.

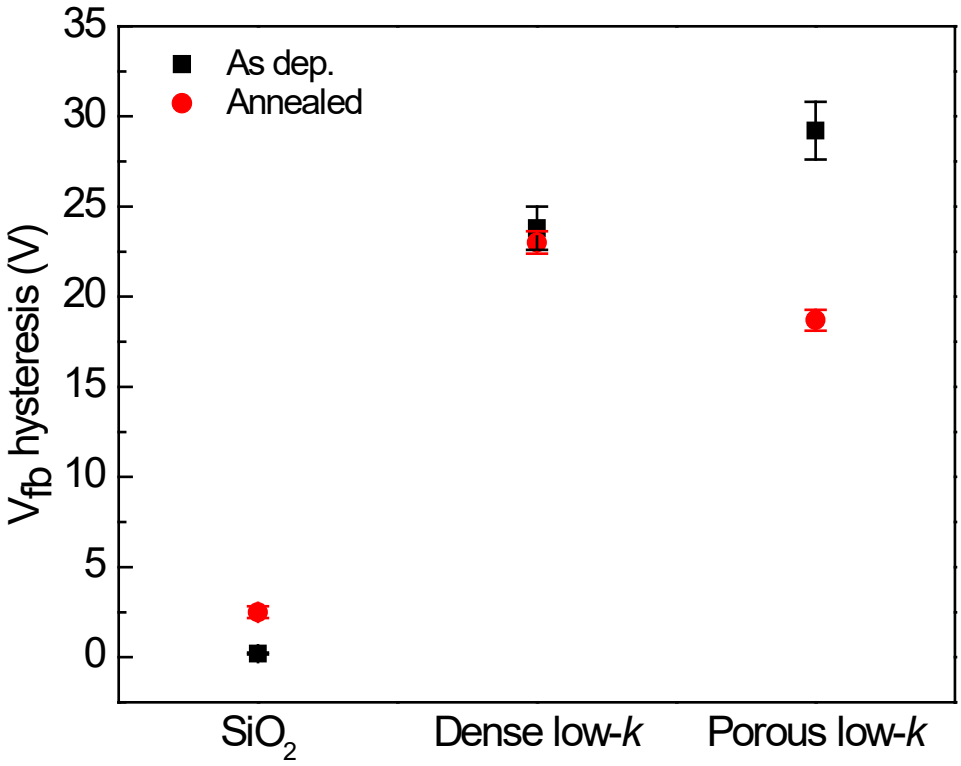

Figure 3. V_{fb} hysteresis of SiO_2, dense, and porous low-*k* dielectric films in Co-gate MIS capacitors before and after annealing.

Figure 4 plots the leakage current versus the electric-field (*I*–*E*) curves of MIS capacitors with various dielectric films before and after annealing. For the SiO_2 film, the leakage current remained constant at 10^{-11} A with the electric field being increased. For both dense and porous low-*k* films, an obvious increase in the leakage current with the applied field was observed. The dense low-*k* film had a higher leakage current than the porous film due to the bonding structure [23], suggesting that the leakage current is less sensitive to porosity. The applied field, at which the leakage current suddenly increases by at least three orders of magnitude to more than 10^{-2} A, is defined as the breakdown field of a dielectric film. As shown in Figure 4, the breakdown field followed the order of SiO_2 > dense low-*k* > porous low-*k*, which is associated with porosity. After annealing, the leakage current decreased for both low-*k* films while it slightly increased for the SiO_2 film. The repair of the sputtering-deposition-induced damage during Co deposition by annealing is likely to be responsible for the reduced leakage current. The increased leakage current in the annealed Co-gate MIS capacitor with SiO_2 film suggests that another mechanism dominates. Moreover, the breakdown field of all dielectric films reduced after annealing.

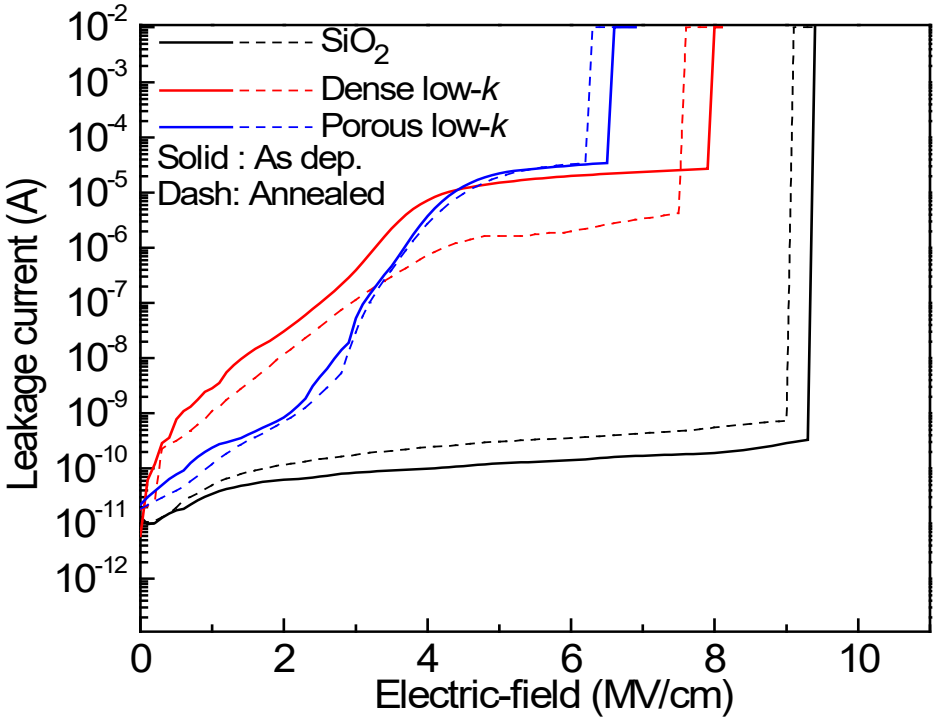

Figure 4. *I*–*E* plots of SiO_2, dense, and porous low-*k* dielectric films in Co-gate MIS capacitors before and after annealing.

Figure 5 compares the breakdown fields of SiO_2, dense, and porous low-*k* dielectric films in the Co-gate MIS capacitors before and after annealing. Here, the presented data were collected from ten samples. The calculated reduction magnitudes of the breakdown field after annealing are also listed in Figure 5. Before and after annealing, the breakdown field followed the same order: SiO_2 > dense low-*k* > porous low-*k*. The breakdown field reduced after annealing for all dielectric films. Notably, the SiO_2 film had the largest reduction magnitude. Based on the studies [32], the breakdown field would not be degraded by annealing until 450 °C for SiO_2, dense, and porous low-*k* dielectric films, provided no extrinsic factor (i.e., metal diffusion) occurs. Here, the reduction in the breakdown field after annealing at 425 °C indicates that the diffusion of Co occurs in all dielectric films in this study. The largest reduction being for the SiO_2 films suggests that more Co diffuses into the film upon annealing. This reflects that an oxygen-rich surface in the SiO_2 film favors the occurrence of Co diffusion [33].

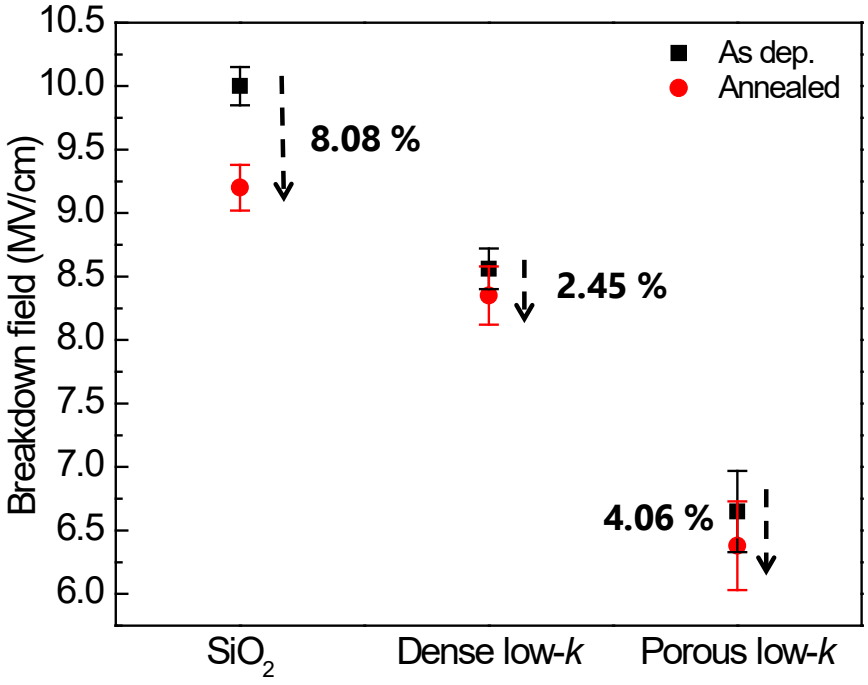

Figure 5. Breakdown fields of SiO_2, dense, and porous low-*k* dielectric films in Co-gate MIS capacitors before and after annealing.

Compared to the SiO_2 film, both the dense and porous low-*k* films, which are carbon-doped SiO_2 films, had a lower reduction in the breakdown field after annealing. This suggests that the doped carbon would slow down the diffusion of Co [34]. Additionally, the porous low-*k* film had a larger reduction in the breakdown field than the dense low-*k* film due to the presence of porosity. The porosity provides a free surface, which is typically a faster diffusion path than the bulk of the film, accelerating the diffusion of Co.

TDDB tests were carried out on the as-deposited and annealed Co-gate MIS capacitors to determine the failure time ($t_{failure}$) as he breakdown of a dielectric film occurs. Three electric fields were applied and the E model ($t_{failure}$ ~exp($-\gamma E$)) was used to describe the breakdown behavior of a dielectric film [35,36]. Here, γ is the electric-field acceleration factor. Figure 6 plots the TDDB failure times of the as-deposited and annealed Co-gate MIS capacitors with SiO_2, dense, and porous low-*k* dielectric films as a function of the applied electric field. The changes in the extracted γ values before and after annealing are plotted in Figure 7. After annealing, all Co-gate MIS capacitors with SiO_2, dense, and porous low-*k* dielectric films exhibited reduced TDDB failure times and γ values. A pronounced reduction was observed in the SiO_2 film. The change in the γ value is a useful indicator to determine the breakdown mechanism [34,37]. An unchanged γ value represents the identical breakdown mechanism while a reduced γ value is associated with the introduction of an extrinsic breakdown mechanism. This extrinsic mechanism for the Co-gate MIS capacitor after being subjected to thermal stress is likely to be the diffusion of Co atoms or ions. As a result, the diffusion of Co into the SiO_2 film upon annealing is more pronounced than with the low-*k* film. Comparing with the dense and porous low-*k* films reveals that the former had a smaller change in the γ value upon annealing. The doped carbon and the dense structure in the dense low-*k* film prevent the injection and diffusion of Co. As a result, barrier-less or barrier-free processing is possibly achieved as Co is integrated with the dense low-*k* films. For SiO_2 and porous low-*k* films integrated with Co, a barrier is required to prevent Co from diffusing into the film.

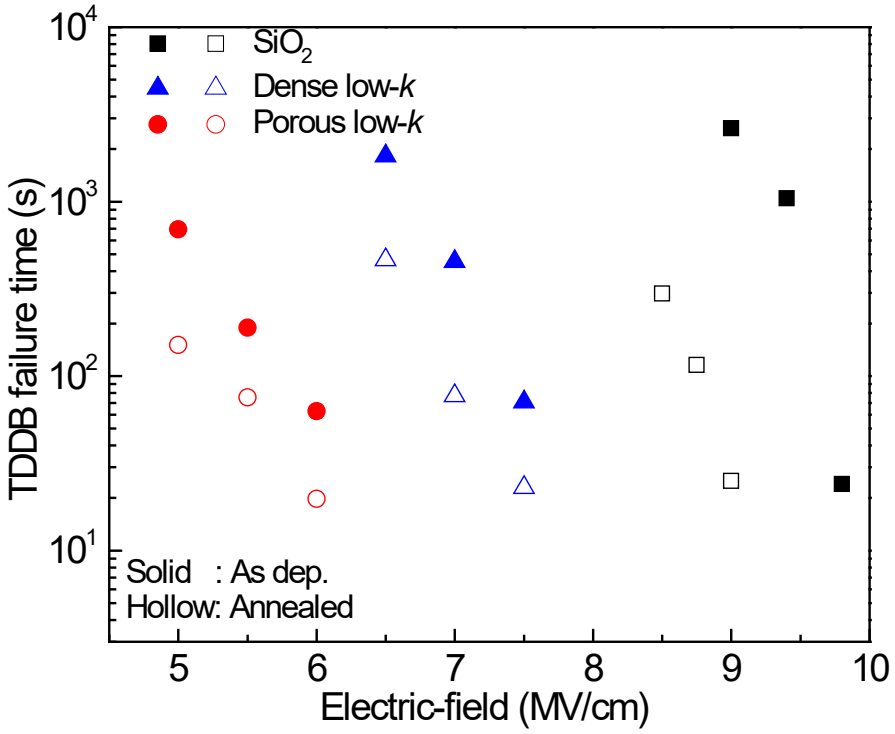

Figure 6. TDDB failure times of SiO_2, dense, and porous low-*k* dielectric films in Co-gate MIS capacitors before and after annealing as a function of stressing electric-field.

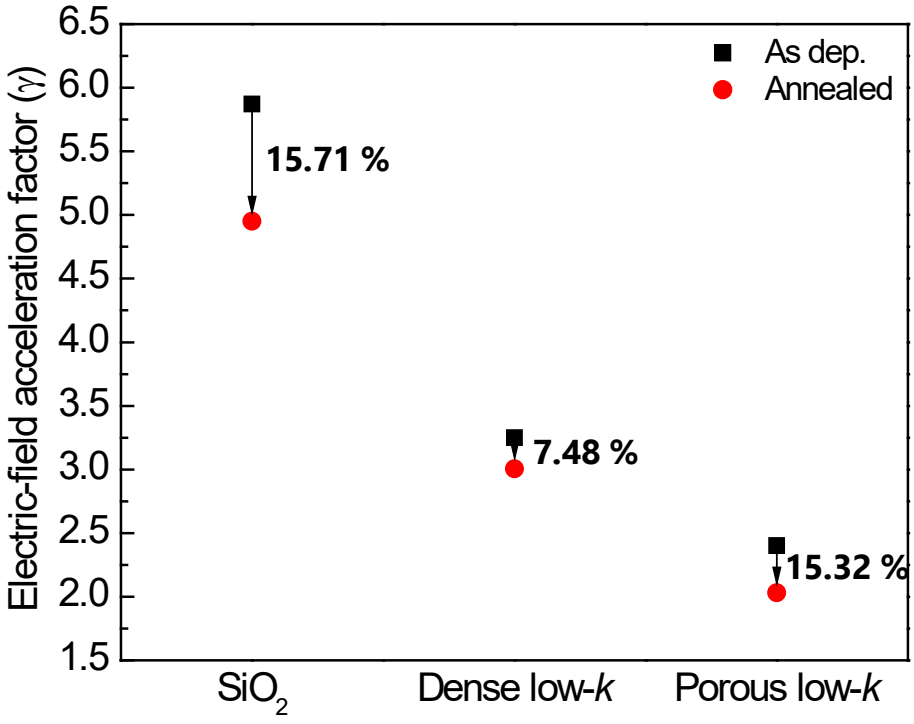

Figure 7. Changes in the electric-field acceleration factor for SiO_2, dense, and porous low-*k* dielectric films in Co-gate MIS capacitors after annealing.

To evaluate the drift of Co into the film under electrical stress for SiO_2, dense, and porous low-*k* dielectric films integrated with Co, positive-polarity fields were applied to the Co-gate MIS capacitors [38]. The stressing time was fixed at 10^2 s. After the application of the electrical stress, *I*–*V* measurements were conducted. Figure 8 plots the *I*–*V* curves of the

Co-gate capacitor with the porous low-*k* film before and after electrical stress with electric fields of 2~5 MV/cm. After the application of positive-polarity electrical stress, a hump, in which the leakage sharply increased and then returned back, was formed. Moreover, this hump amplified with the applied electric field. This hump is believed to be the ionic current due to the migration of metal (Co) ions. First, positive-polarity electrical stress oxidizes Co to form ions; they then drift into the porous low-*k* film under the external electric field. Subsequently, a negative voltage sweep in the *I*–*V* measurement pushes the injected Co ions to drift back to the previous metal–dielectric interface. In addition to the presence of the hump, the breakdown field decreased and the reduction magnitude amplified with the increasing stressing field for the porous low-*k* film after electrical stress. These features reflect the drift of Co ions under electrical stress. For SiO_2 and dense low-*k* films that underwent identical electrical stress, no hump was observed and a negligible reduction in the breakdown field was detected, indicating that the drift of Co ions was blocked. Figure 9 compares the reduction in the breakdown field for SiO_2, dense, and porous low-*k* dielectric films in the Co-gate MIS capacitors after positive-polarity electrical stress as a function of the applied electric field. As shown, the porous low-*k* film had the largest reduction in the breakdown field and the SiO_2 film had the lowest reduction, indicating that porosity and bonding in the film play a critical role in controlling Co ion migration under electrical stress. For the low-*k* films, the strength of Si–C bonding is relatively weak compared to that of Si–C bonding in the SiO_2 film. As a result, electrical stress easily destroys Si–C bonding, leading to the drift of Co ions. Moreover, porosity in the low-*k* film further accelerates the drift of Co ions. As a result, the drift of Co ions into the porous low-*k* film under positive-polarity electrical stress is pronounced, thereby seriously degrading the electrical characteristics.

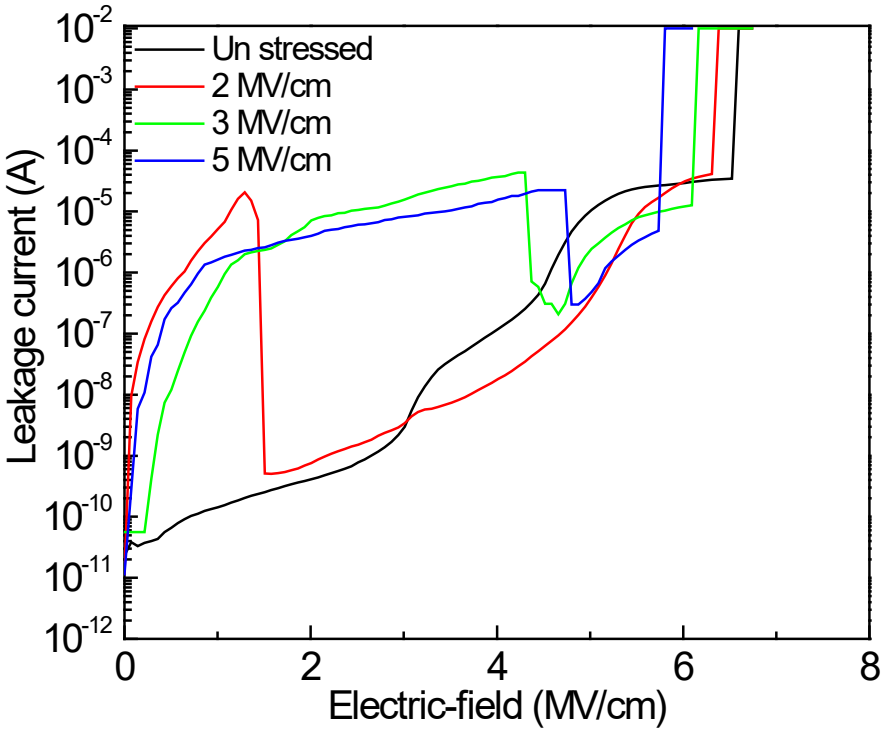

Figure 8. *I*–*E* plots of Co-gate MIS capacitors with porous low-*k* films before and after positive-polarity electrical stress with various fields.

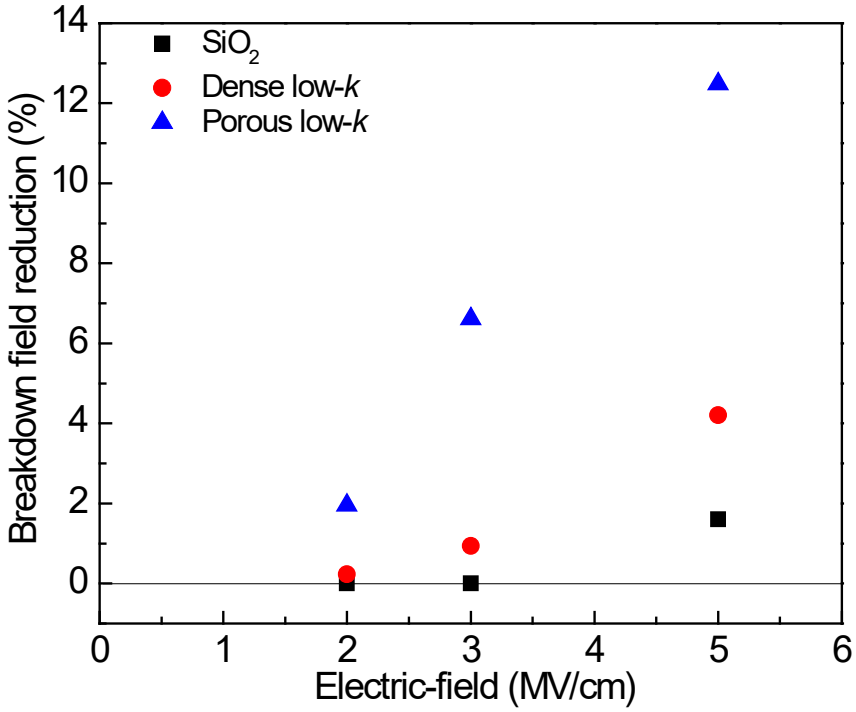

Figure 9. Reduction of the breakdown field for SiO_2, dense, and porous low-*k* dielectric films in Co-gate MIS capacitors after being subjected to positive-polarity electrical stress as a function of the stressing electric field.

4. Conclusions

The electric characteristics and reliability of the integration of Co and various dielectric films under thermal and electrical stress have been investigated in this study. The sputtering deposition of Co induced damage on the dielectric film, thereby increasing the capacitance and *k* value. This increase was pronounced for the porous low-*k* film. Thermal annealing partially repaired the damage but reduced the breakdown field and TDDB characteristics due to the diffusion of Co. After annealing, the SiO_2 film had the largest reduction due to the oxygen-rich surface, which favors the diffusion of Co. Under electrical stress, the drift of Co ions/atoms was serious in the porous low-*k* film due to the existence of porosity, thereby seriously degrading the electric characteristics. As a result, a barrier is required for SiO_2 and porous low-*k* films when integrated with Co. To achieve barrier-free or barrier-less processing in Co metallization, the dense low-*k* film is the best option to integrate with Co.

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