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Article

Impacts of Work Function Variation and Line-Edge Roughness on TFET and FinFET Devices and 32-Bit CLA Circuits †

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Abstract: In this paper, we analyze the variability of III-V homojunction tunnel FET (TFET) and FinFET devices and 32-bit carry-lookahead adder (CLA) circuit operating in near-threshold region. The impacts of the most severe intrinsic device variations including work function variation (WFV) and fin line-edge roughness (fin LER) on TFET and FinFET device I_{on}, I_{off}, C_g, 32-bit CLA delay and power-delay product (PDP) are investigated and compared using 3D atomistic TCAD mixed-mode Monte-Carlo simulations and HSPICE simulations with look-up table based Verilog-A models calibrated with TCAD simulation results. The results indicate that WFV and fin LER have different impacts on device I_{on} and I_{off}. Besides, at low operating voltage (<0.3 V), the CLA circuit delay and power-delay product (PDP) of TFET are significantly better than FinFET due to its better I_{on} and $C_{g,ave}$ and their smaller variability. However, the leakage power of TFET CLA is larger than FinFET CLA due to the worse I_{off} variability of TFET devices.

Keywords: tunnel FET (TFET); FinFET; work function variation (WFV); line-edge-roughness (LER); carry-lookahead adder (CLA)

1. Introduction

Steep subthreshold slope TFET, which utilizes the band-to-band tunneling as the conduction mechanism, is one of the most promising candidates for ultra-low voltage/power applications [1]. Recent research works on TFET-based circuits have shown significant performance improvement and power reduction at low operating voltage [2–4]. With device scaling, the impacts of random variations become more severe. Several studies on the TFET device level variability have been reported [5–8], while other works on TFET circuits employed simple parameter sensitivity methods that neglect physical non-uniformities [2,9,10], and a physics-based TFET performance and variability assessment for large logic circuits is lacking. Among all variation sources, the work function variation (WFV) caused by the granularity of different grain orientations and sizes of the metal gate material and fin Line-Edge-Roughness (LER) due to the resolution limit of the lithography and etching processes have the most significant impacts on TFET and FinFET devices. In this work, we provide an in-depth physics-based assessment on the impacts of WFV and fin LER on TFET and FinFET devices including the detailed comparative analyses on I_{on}, I_{off}, and C_g using three-dimensional atomistic TCAD simulations. To assess the variability on large logic circuits, we build look-up table based Verilog-A models, and examine the variability of TFET- and FinFET-based 32-bit CLA circuits using HSPICE simulations with Verilog-A model calibrated with TCAD simulation results. Our work provides in-depth physics-based understanding on the variability of 32-bit CLA circuits and fundamental guidelines on the implementation of TFET-based large logic circuits considering variability.

2. Device Structures, Characteristics and Simulation Methodology

2.1. Device Structures and Characteristics

The basic TFET structure under study comprises a gated p-i-n tunnel diode under reverse bias with asymmetrical source/drain doping. For N-TFET, the source is p+ region with dominant electron conduction, the channel is gated intrinsic region, and the drain is n+ region. When N-TFET is "OFF" (V_{GS} = 0), the valence band edge of the source is below the conduction band edge of the channel, and the band-to-band tunneling probability is low due to lack of available states in the channel region and wide barrier at source-channel junction. When N-TFET is "ON" (V_{GS} > 0), the conduction band edge of the channel is pulled down below the valence band edge of the source, and carriers can tunnel into available empty states of the channel region. For P-TFET, the source is n+ region with dominant hole conduction, applying V_{GS} < 0 turns P-TFET "ON". The band diagrams of TFET in ON/OFF states are shown in Figure 1.

In this work, we consider the $In_{0.53}Ga_{0.47}As$ homojunction N-TFET and $Ge_{0.925}Sn_{0.075}$ homojunction P-TFET due to their high I_{on} and compatible I_{DS}-V_{GS} characteristic [12,13]. $In_{0.53}Ga_{0.47}As$ N-FinFET and Ge P-FinFET with high mobility are considered for comparison. Figure 2 shows the 3D TFET and

FinFET device structures constructed for atomistic TCAD simulations. The device parameters and doping are shown in Table 1. We use the non-local band-to-band tunneling model which is applicable to arbitrary tunneling barrier with non-uniform electric field for TFET simulations [11], and the parameters used in the model are calibrated with [12,13]. Figure 3a shows the I_{DS}-V_{GS} characteristics of TFETs and FinFETs at V_{DS} = 0.3 V and V_{DS} = 0.03 V. The DIBL (drain-induced barrier lowering) and DIBT (drain-induced barrier thinning) values *versus* drain current for N-TFET and N-FinFET are shown in Figure 3b. DIBL for the conventional MOSFET device is estimated using the following formula in weak inversion region (subthreshold region):

$$\text{DIBL} = \frac{\Delta V_{TH}}{\Delta V_{DS}} \text{ (mV/V)} \tag{1}$$

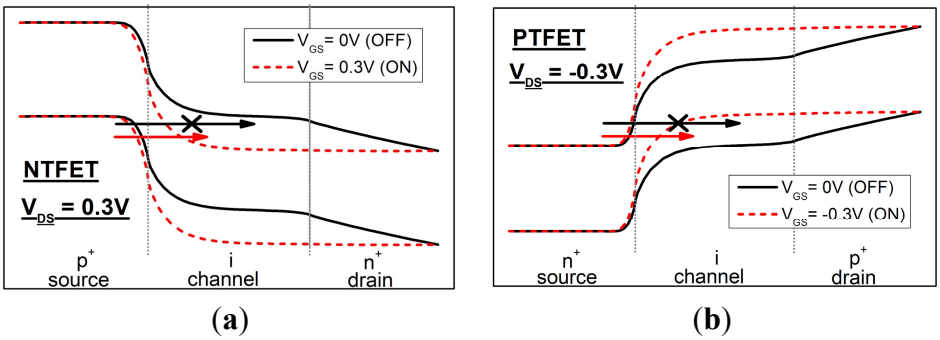


Figure 1. Energy band diagrams of (**a**) n-type and (**b**) p-type TFET in ON/OFF state.

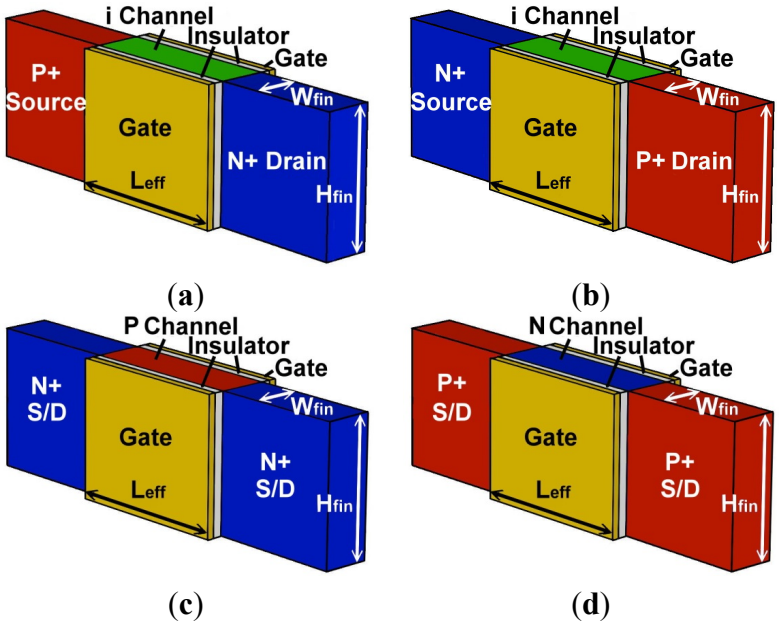


Figure 2. Physical structures of (**a**) $In_{0.53}Ga_{0.47}As$ homojunction N-TFET; (**b**) $Ge_{0.925}Sn_{0.075}$ homojunction P-TFET; (**c**) $In_{0.53}Ga_{0.47}As$ N-FinFET and (**d**) Ge P-FinFET.

Table 1. Parameters of TFET and FinFET devices.

Devices	**TFET**		**FinFET**
L_{eff} **= 25 nm**	W_{fin} **= 7 nm**	H_{fin} **= 20 nm**	EOT **= 0.65 nm**
	nTFET	***pTFET***	***FinFET***
Material	$In_{0.53}Ga_{0.47}As$	$Ge_{0.925}Sn_{0.075}$	$In_{0.53}Ga_{0.47}As$
Nch (cm^{-3})	undoped	undoped	1×10^{17}
Ns (cm^{-3})	4.5×10^{19} (p-type)	2×10^{19} (n-type)	1×10^{20}
Nd (cm^{-3})	2×10^{17} (n-type)	2×10^{17} (p-type)	1×10^{20}

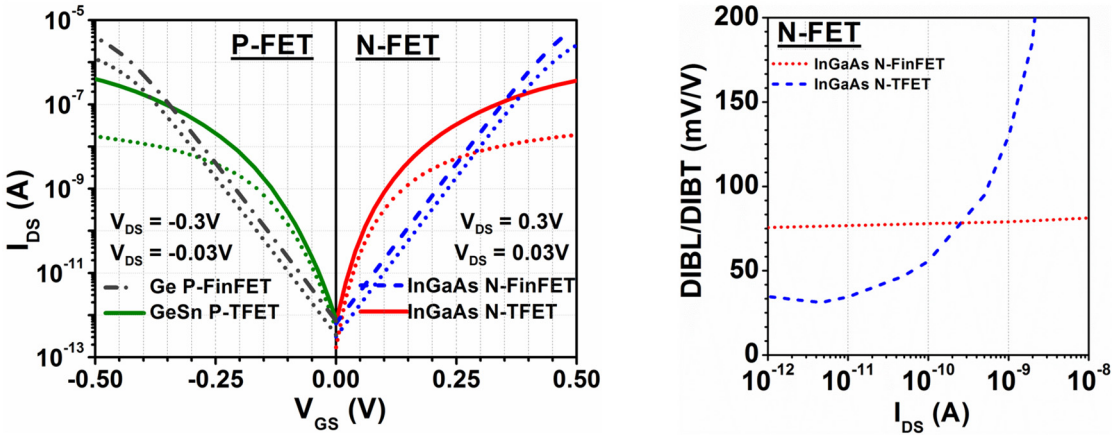
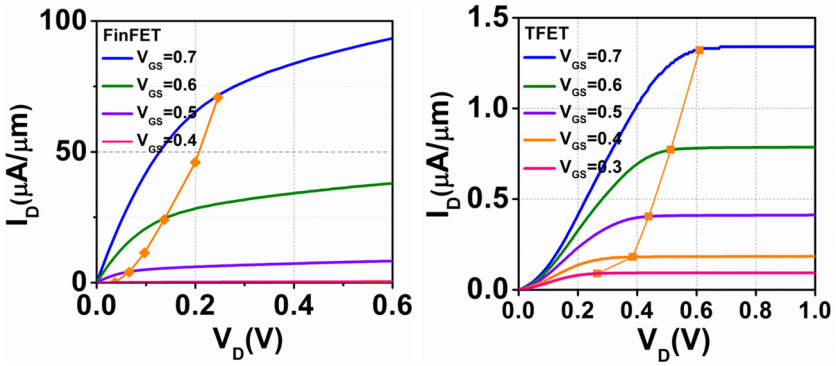


Figure 3. (**a**) I_{DS}-V_{GS} characteristics at V_{DS} = 0.3 V and V_{DS} = 0.03 V of $In_{0.53}Ga_{0.47}As$ N-TFET, $Ge_{0.925}Sn_{0.075}$ P-TFET, $In_{0.53}Ga_{0.47}As$ N-FinFET and Ge P-FinFET; (**b**) DIBL and DIBT value *versus* drain current for $In_{0.53}Ga_{0.47}As$ N-TFET and N-FinFET.

In TFET, the drain bias also plays a role in enhancing the drain current due to the drain bias induced source-channel tunneling barrier thinning effect. However, as the physics-based method for extracting the threshold voltage of TFET is still under investigation, there is no clear definition for DIBT extraction analogous to DIBL in FiFET device. Hence, for first-order approximation for estimating DIBT in TFET device, we draw the DIBT as a function of drain to source current shown in Figure 3b. As can be seen, the DIBT for TFET shows non-monotonic behavior compared with the FinFET counterpart and increases rapidly as the drain to source current increases beyond 0.2 nA. This is because TFET has smaller threshold voltage (using the constant current defined V_{th}) and enters the saturation region earlier than the FinFET which is in the weak inversion region with DIBL roughly around 80 mV/V.

Figure 4 shows the output characteristics for TFET and FinFET devices. As shown, TFET device shows larger V_{DSAT} [14] as indicated in rhombus symbol due to the fact that TFET can be regarded as a source-channel tunneling junction in series with a resistor (*i.e.*, channel resistance), hence exhibiting an upward-concaved shape in the triode-like region (analogous to FinFET). At moderate and high V_{DS}, TFET provides a better (flatter) saturation characteristic due to reduced carriers in the channel region, and the electric field from the drain side cannot penetrate into the source-channel tunnel junction, so the current increases slowly. For FinFET device, no obvious saturation is observed due to more severe short-channel effect.

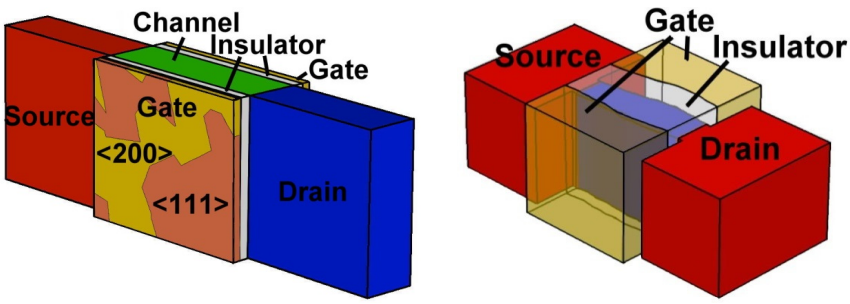


(**a**) (**b**)

Figure 4. I_{DS}-V_{DS} characteristics at various V_{GS} bias for (**a**) FinFET and (**b**) TFET device with the rhombus symbol showing the extrated V_{DSAT}.

2.2. Simulation Methodology

To assess WFV, we use the Vonoroi grain pattern [15] for TiN gate material, which has two different grain orientations <200> and <111> with the probability of 60% and 40%, respectively, as shown in Figure 5a by the yellow and orange regions, and the relevant parameters are shown in Table 2. To assess fin LER, the rough line edge patterns are generated by Fourier synthesis approach [16] with correlation length (Λ) = 20 nm and root-mean-square amplitude (Δ) = 1.5 nm as shown in Figure 5b. We analyze the impacts of WFV and fin LER on devices using 3D atomistic TCAD mixed-mode Monte-Carlo simulations with 100 samples, respectively.



(**a**) (**b**)

Figure 5. Examples of structures with (**a**) WFV and (**b**) fin LER.

Table 2. Parameters for WFV simulations.

Gate Material = TiN		**Grain Size = 5 nm**	
Work function (eV)	**Nominal**	**<200> (60%)**	**<111> (40%)**
InGaAs N-TFET	4.53	4.61	4.41
GeSn P-TFET	4.82	4.9	4.7
InGaAs N-FinFET	4.88	4.96	4.76
Ge P-FinFET	4.27	4.35	4.15

TCAD mixed-mode simulations for complex circuits with large transistor counts face the challenges of computation resources, prohibitively long simulation times and convergence problems. To overcome

these obstacles, look-up table based Verilog-A model has been employed for TFET circuit simulations in some studies [2,4]. However, these works on TFET circuits employed simple parameter sensitivity methods [2,9], and these sensitivity-based Verilog-A models cannot accurately describe the physical non-uniformities and variability. In this work, we adopt physics-based assessment to account for variability at device and circuit level. The flow chart for physics-based small signal Verilog-A model generation is shown in Figure 6. The transfer characteristics of TFET and FinFET devices and their variability with WFV and fin LER are extracted from atomistic 3D TCAD device simulations with I_{DS} (V_{GS}, V_{DS}), C_{gs} (V_{GS}, V_{DS}) and C_{gd} (V_{GS}, V_{DS}) characteristics across voltage range of interest to build two-dimensional Verilog-A look-up tables. The Verilog-A models of devices with random variations are then employed in HSPICE circuit simulations. The calibrations of Verilog-A models with TCAD results on *I-V*, *C-V* characteristics of the nominal cases for TFET and FinFET devices are shown in Figure 7. The almost exact agreements can be clearly seen.

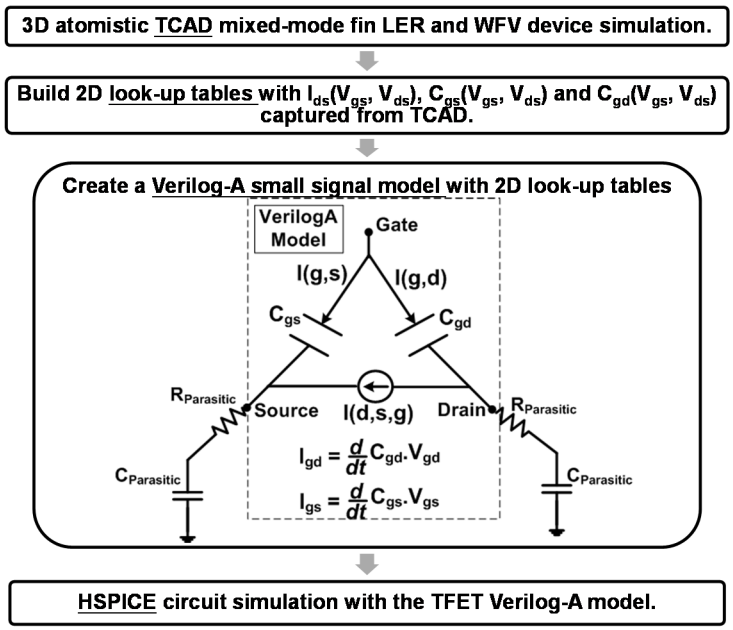


Figure 6. Flowchart for HSPICE look-up table based Verilog-A model generation from atomistic 3D TCAD simulations [2,4].

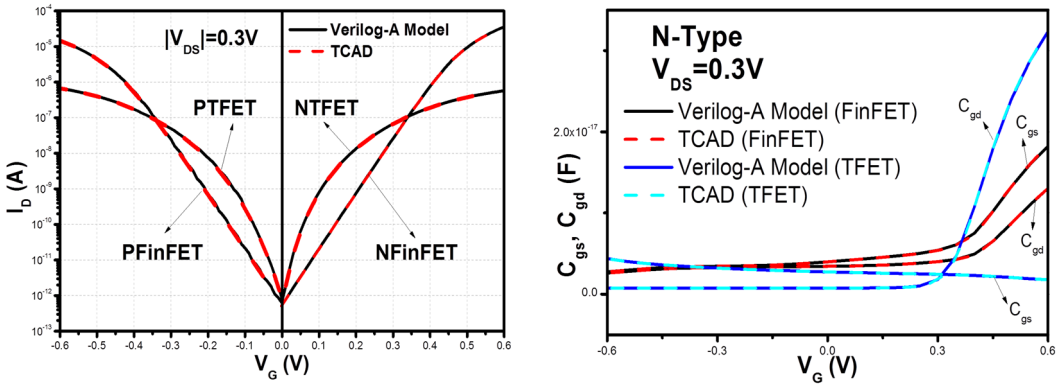


Figure 7. Calibrations of Verilog-A models with TCAD results on (**a**) *I-V* and (**b**) *C-V* charcteristics of the nominal cases for TFET and FinFET deivces at V_{DS} = 0.3 V.

3. Device Variability Due to WFV and Fin LER

3.1. I_{off} and I_{on} Variability

Figure 8 shows the impacts of WFV and fin LER on I_{DS}-V_{GS} dispersions of TFET and FinFET devices at V_{DS} = 0.3 V. Figure 9 illustrates the probability distributions of I_{on} (I_{DS} at V_{DS} = V_{GS} = 0.3 V) and I_{off} (I_{DS} at V_{DS} = 0.3 V and V_{GS} = 0 V). Note that, for TFET variability, the different structure constructs used for WFV and fin LER lead to slightly different nominal I_{DS}-V_{GS} curves. Therefore, the corresponding probability distributions show two nominal values. The mean values (μ), standard deviations (σ) and the ratio of the mean-to-standard deviation (μ/σ) are listed in the table with the figures.

For FinFETs, the V_t is a linear function of gate WF, WFV causes a V_t shift of I_{DS}-V_{GS} curves in subthreshold region with almost equal subthreshold swing (S.S.), therefore the I_{on} and I_{off} probability distributions are similar. On the other hand, fin LER influences the effective fin width and electrostatic integrity, thus impacting both V_t and S.S., so the I_{on} and I_{off} probability distributions are quite different. As can be seen, both the μ/σ of I_{on} and I_{off} are worse with fin LER than WFV, especially for I_{off}.

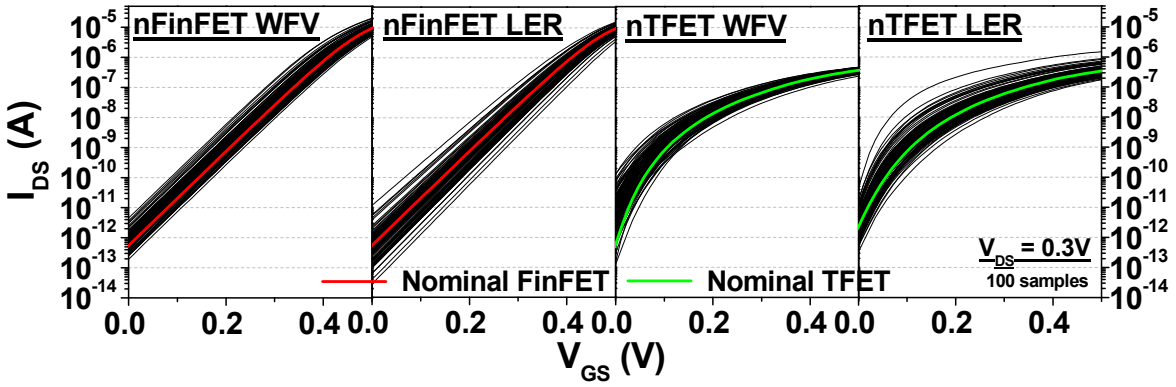
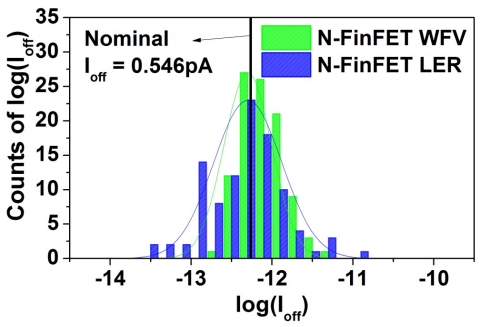


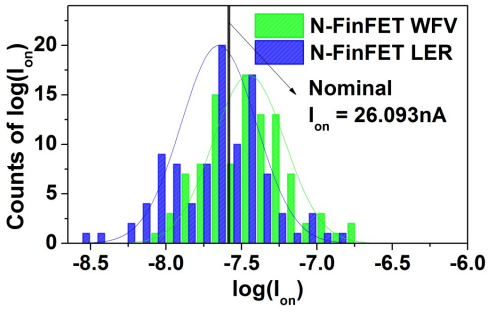
Figure 8. Simulated I_{DS}-V_{GS} characteristics at V_{DS} = 0.3 V for TFET and FinFET with WFV and fin LER.

	μIoff (pA)	σIoff (pA)	μ/σ
N-FinFET WFV	0.968	0.749	1.29
N-FinFET LER	0.856	1.466	0.58



(a)

	μIon (nA)	σIon (nA)	μ/σ
N-FinFET WFV	42.508	31.998	1.37
N-FinFET LER	28.13	22.583	1.25



(b)

Figure 9. *Cont.*

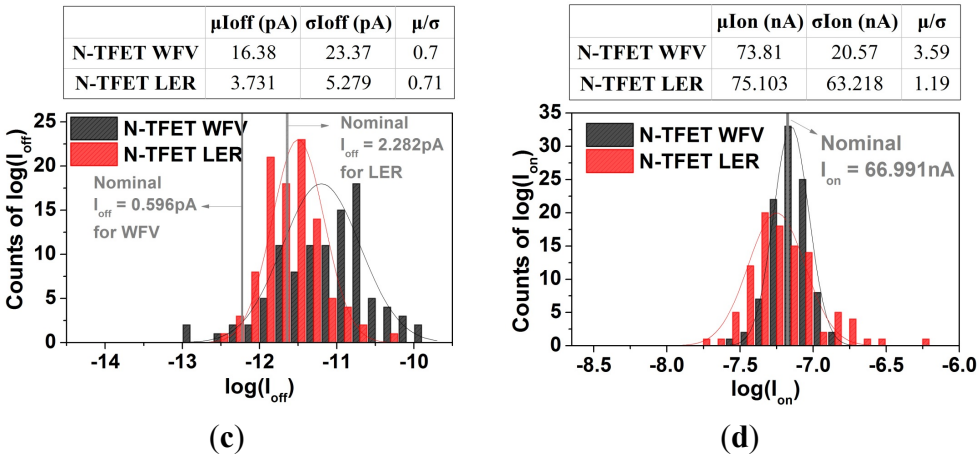


Figure 9. Probability distribution of (**a**) log(I_{off}); (**b**) log(I_{on}) for FinFET and (**c**) log(I_{off}); (**d**) log(I_{on}) for TFET at V_{DS} = 0.3 V considering WFV and fin LER.

For TFETs, the I_{off} distribution with WFV is boarder (worse) than that with fin LER since WFV leads to fluctuation in the energy bands and alters the critical tunneling path, and the effect decreases with increasing V_{GS}. The metal grains with various WF form the up and down energy bands that boost the band-to-band generation, resulting in large I_{off} distribution. Therefore, the variability of I_{off} is larger than I_{on}, and the correlation between I_{on} and I_{off} is weak. On the other hand, for fin LER, both I_{on} and I_{off} are degraded as fin width (W_{Fin}) increases due to the weaker electrostatic control of the channel from both gates, and the degradations of I_{on} and I_{off} track W_{Fin} with exponential-like behavior, especially for I_{off} which dramatically increases with decreasing W_{Fin}. Comparing with fin LER, the µ/σ (I_{on}) of WFV is better, and the µ/σ (I_{off}) of WFV is comparable to LER. In addition, WFV causes larger σ (I_{off}) than LER. Overall, comparing FinFET and TFET, the impacts due to WFV on I_{on} and I_{off} are quite different. The µ/σ (I_{off}) of TFET is worse while µ/σ (I_{on}) of TFET is better. In addition, the I_{off} distribution of TFET skews to high values, and not as symmetrical as the I_{off} distribution for FinFET, resulting in larger µ (I_{off}). On the other hand, the variation of TFET considering fin LER is slight better than FinFET.

3.2. C_g Variability

Figure 10 shows the impacts of WFV and fin LER on C_g-V_{GS} dispersions of TFET and FinFET devices at V_{DS} = 0.3 V. Figure 11 illustrates the probability distributions of $C_{g,ave}$ (the average capacitance across the gate-bias range from 0 to V_{DD} = 0.3 V) at V_{DS} = V_{DD}. For both TFET and FinFET, the C_g variation by WFV becomes more significant at larger V_{GS}. In contrast, the variation due to fin LER is more severe when V_{GS} is small. Note that $C_{g,ave}$ is extracted only for the range from V_{GS} = 0 V to 0.3 V. The µ/σ (WFV) are much better compared with µ/σ (LER). For TFET with WFV and FinFET with fin LER, the $C_{g,ave}$ skews to high values, resulting in larger µ than the nominal cases.

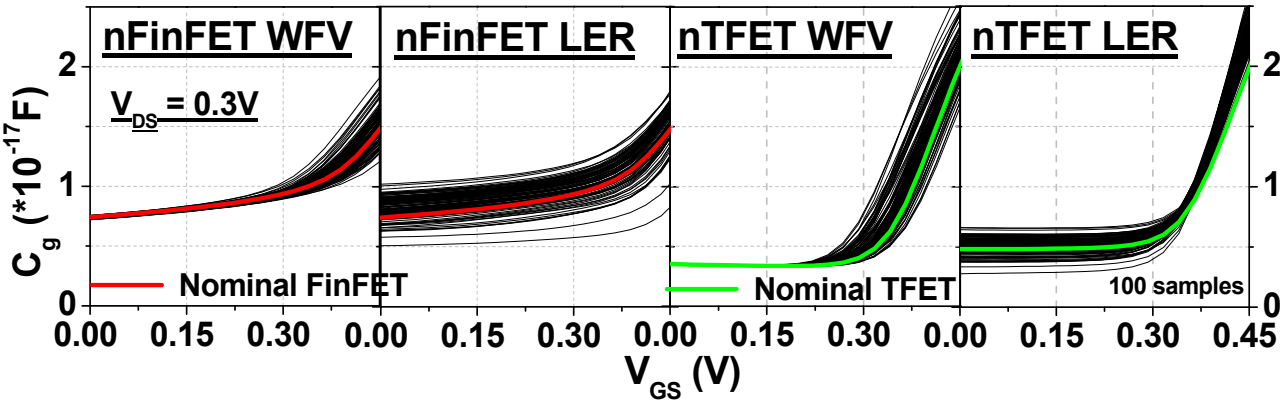


Figure 10. Simulated C_g-V_{GS} characteristics at V_{DS} = 0.3 V for TFET and FinFET with WFV and fin LER.

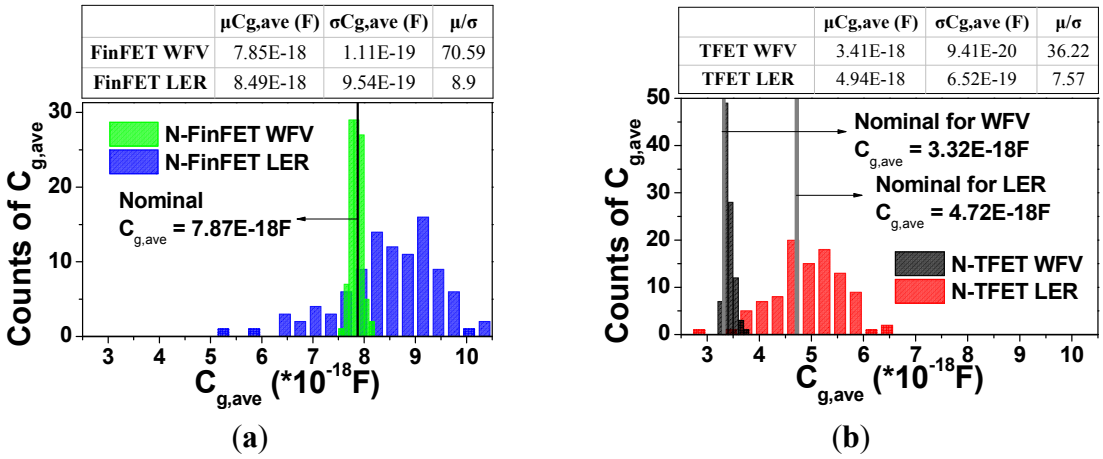


Figure 11. Probability distribution of $C_{g,ave}$ for (**a**) FinFET and (**b**) TFET at V_{DS} = 0.3 V considering WFV and fin LER.

4. Impacts of WFV and Fin LER on CLA Circuits

4.1. Delay Variability

The switching delay is commonly calculated as $\tau = (C_g V_{DD})/I_{on}$. Due to the strong bias dependence of gate capacitance (C_g), the average capacitance ($C_{g,ave}$) across the gate-bias range from 0 to V_{DD} (0.3 V in this case) at $V_{DS} = V_{DD}$ is determined for approximation: $\tau = (C_{g,ave} V_{DD})/I_{on}$.

The transient waveforms and the probability distributions of delays for 32-bit CLA of TFET and FinFET with WFV and fin LER are shown in Figures 12 and 13. As can be seen, the μ/σ (Delay) of TFET is better than FinFET in both cases (with WFV and fin LER). For both TFET and FinFET, the μ/σ (WFV) is better than μ/σ (LER). The variability of delay correlates with aforementioned I_{on} and $C_{g,ave}$ variations in Section 3. The smaller I_{on} of FinFET significantly degrades its μ/σ (Delay).

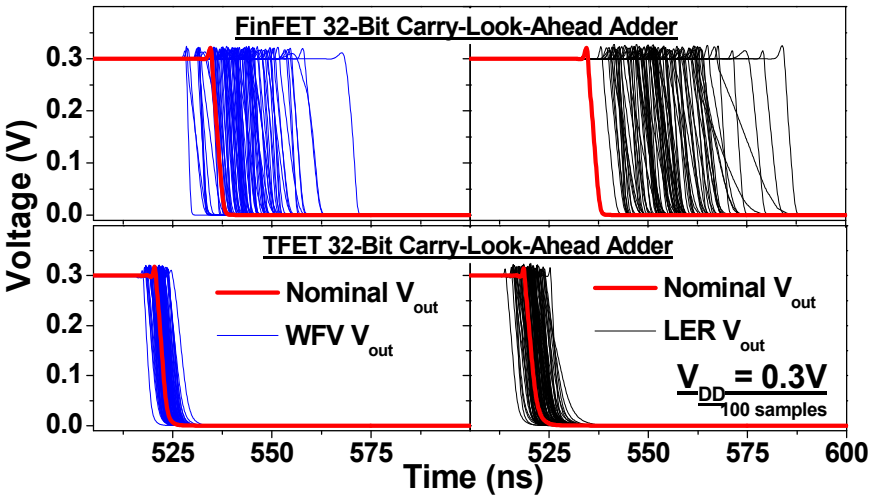


Figure 12. Transient waveforms of 32-bit CLA for TFET and FinFET at V_{DD} = 0.3 V considering WFV and fin LER.

	μDelay (ns)	σDelay (ns)	μ/σ
TFET WFV	25.05	1.11	22.51
FinFET WFV	43.79	4.25	10.3

	μDelay (ns)	σDelay (ns)	μ/σ
TFET LER	25.53	1.98	12.9
FinFET LER	61.51	6.49	9.48

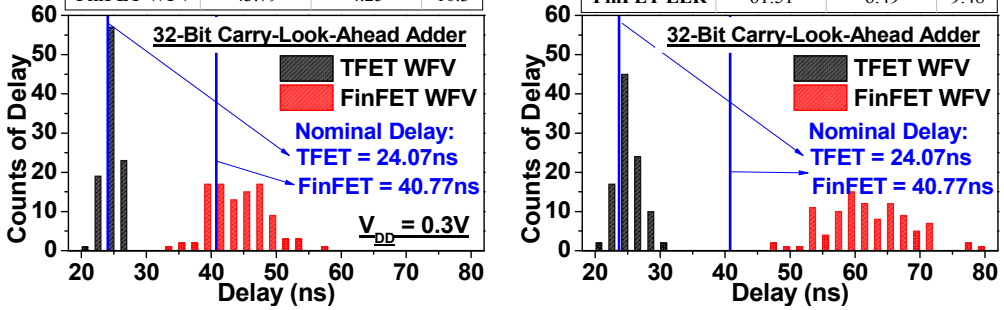


Figure 13. Probability distribution of delay for 32-bit CLA with (**a**) WFV; (**b**) fin LER for TFET and FinFET at V_{DD} = 0.3 V.

Figure 14 presents the delay for 32-bit CLA of TFET and Fin FET *versus* V_{DD} from 0.15 V to 0.35 V for the nominal cases and the cases considering WFV and fin LER (at 0.2 V and 0.3 V). The delay variability of all cases becomes worse with decreasing V_{DD} due to decreasing I_{DS}. The delay and its variability of TFET are significantly better than FinFET at low V_{DD} due to its larger I_{DS} and smaller $C_{g,ave}$ variation compared with FinFET.

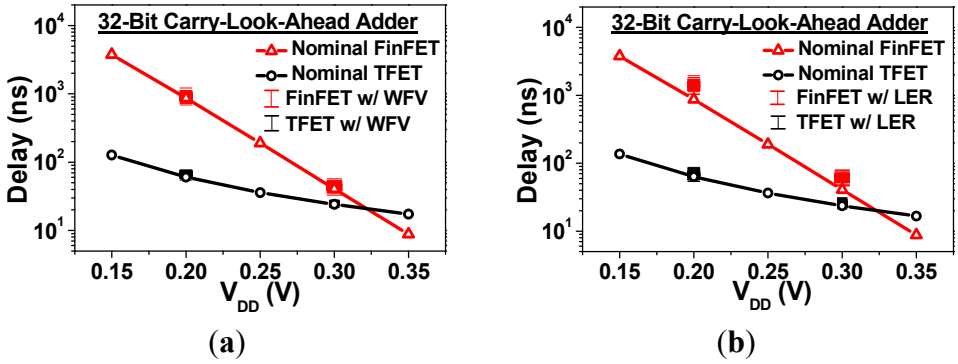


Figure 14. Delay for 32-bit CLA of TFET and FinFET *versus* V_{DD} from 0.15 V to 0.35 V for the nominal cases and the cases considering (**a**) WFV and (**b**) fin LER (0.2 V and 0.3 V).

4.2. PDP Variability

PDP is a figure of merit representing the power-performance trade-off. At a given operation frequency, PDP is calculated as PDP = $(C_g V^2_{DD} f) \times t_{delay} \approx C_{g,ave} V^2_{DD} f t_{delay}$. If the frequency is scaled up to the maximum operation frequency (*i.e.*, $f = 1/t_{delay}$), then PDP = $(C_g V^2_{DD})$ would represent the energy dissipated in a switching event.

The probability distributions of PDP 32-bit CLA of TFET and FinFET for the nominal cases and the cases with WFV and fin LER are shown in Figure 15. The μ/σ (WFV) is better than μ/σ (LER) for both TFET and FinFET, and the distributions of TFET with WFV and that of FinFET with fin LER skew to larger values.

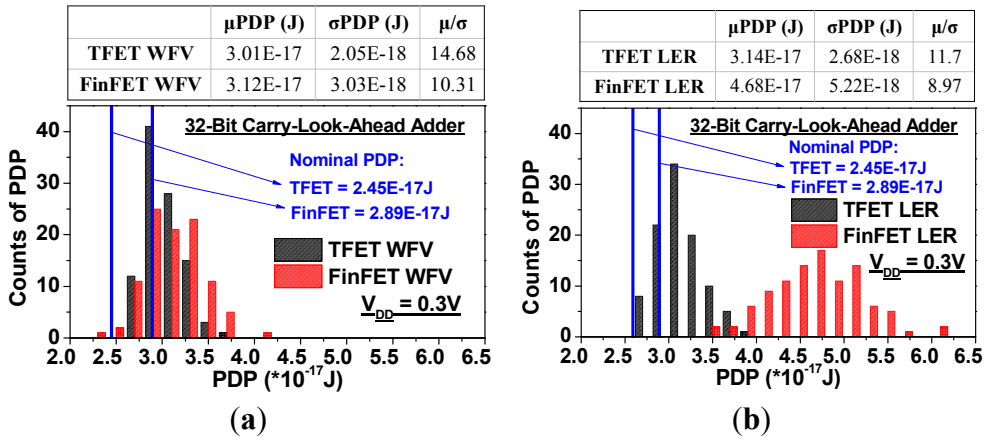


Figure 15. Probability distribution of PDP for 32-bit CLA with (**a**) WFV; (**b**) fin LER for TFET and FinFET at V_{DD} = 0.3 V.

Figure 16 shows the PDP for 32-bit CLA of TFET and FinFET *versus* V_{DD} from 0.15 V to 0.35 V for the nominal cases and the cases considering WFV and fin LER (at 0.2 V and 0.3 V). As can be seen, TFET PDP is much better than FinFET at low V_{DD} due to the fact that $C_{g,ave}$ variation of FinFET is larger and skewed to high values compared with TFET. Notice that the PDP of TFET is still better than FinFET considering random variations.

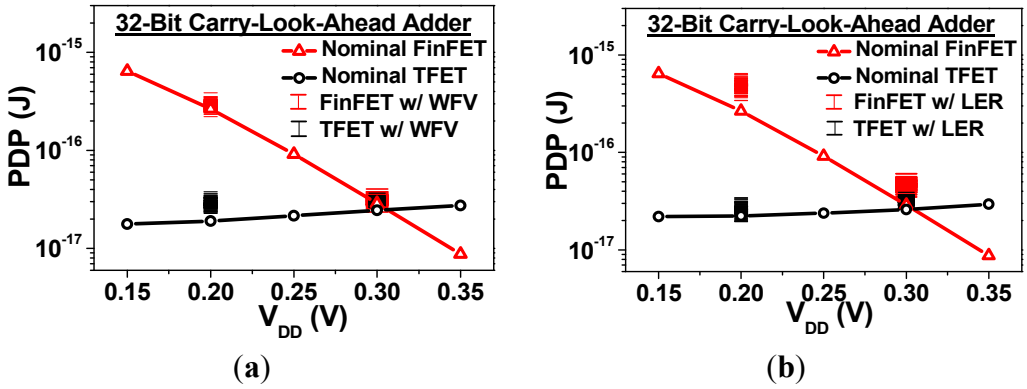


Figure 16. PDP for 32-bit CLA of TFET and FinFET *versus* V_{DD} from 0.15 V to 0.35 V for the nominal cases and the cases considering (**a**) WFV and (**b**) fin LER (0.2 V and 0.3 V).

4.3. Leakage Power Variability

The probability distributions of leakage power for 32-bit CLA of TFET and FinFET for the nominal cases and the cases with WFV and fin LER at V_{DD} = 0.3 V are shown in Figure 17. The leakage power variation of TFET with both variation sources are much worse than FinFET, and the distributions skew to larger values, especially under WFV. This correlates to aforementioned I_{off} variations in Section 3.

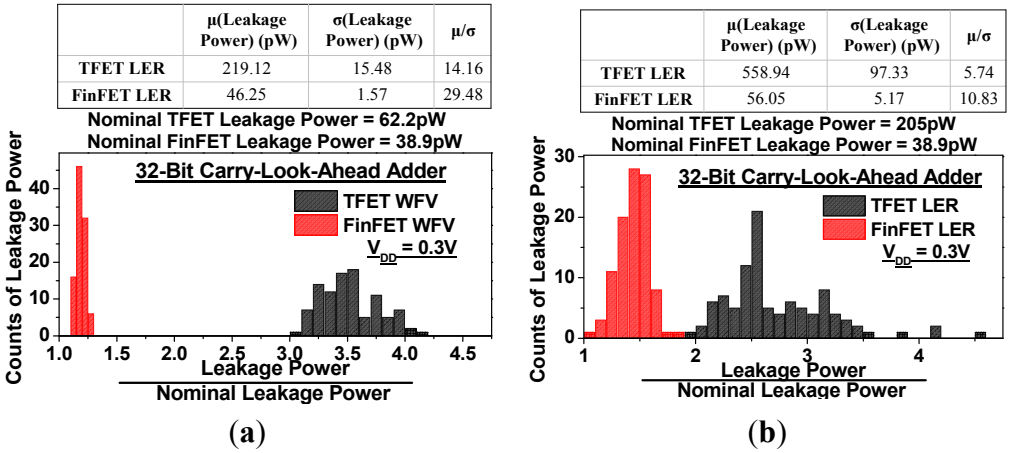


Figure 17. Probability distribution of leakage power for 32-bit CLA with (**a**) WFV; (**b**) fin LER for TFET and FinFET at V_{DD} = 0.3 V.

Figure 18 shows the leakage power for 32-bit CLA of TFET and FinFET *versus* V_{DD} from 0.15 V to 0.35 V for the nominal cases and the cases considering WFV and fin LER (at 0.2 V and 0.3 V). As the operating voltage is reduced, the leakage power decreases. Notice that the increase of leakage power by random variations is more significant than the influence by operating voltage for TFET.

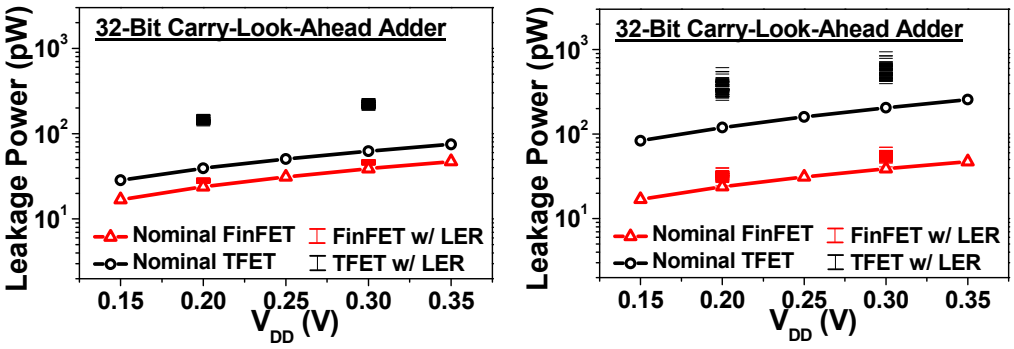


Figure 18. Leakage power for 32-bit CLA of TFET and FinFET *versus* V_{DD} from 0.15 V to 0.35 V for the nominal cases and the cases considering (**a**) work function variation (WFV) and (**b**) fin Line-Edge-Roughness (fin LER) (0.2 V and 0.3 V).

5. Conclusions

We investigate and compare the impacts of WFV and fin LER on TFET and FinFET I_{on}, I_{off} and $C_{g,ave}$ using atomistic 3D TCAD simulations with calibrated model and device parameters. Our studies indicate that considering WFV, FinFET has comparable I_{on} and I_{off} variability while TFET has smaller I_{on} variability and larger I_{off} variability. In addition, the band diagram dispersion caused by WFV increases the band-to-band generation for TFET in "OFF" state, leading to skewed I_{off} distribution to larger values. On the other hand, the impact of fin LER is similar for TFET and FinFET, resulting in comparable I_{on} and I_{off} variability. The $C_{g,ave}$ variability is worse with fin LER compared with WFV for both TFET and FinFET.

Using Verilog-A device models extracted from atomistic 3D TCAD simulations to capture the physical non-uniformities and variability, HSPICE circuit simulations are performed to assess the impacts of WFV and fin LER on TFET and FinFET 32-bit CLA. The results show that at low operating voltage (<0.3 V), the delay and PDP of TFET CLA are significantly better than the FinFET counterparts, even under the impacts of WFV and LER. However, the variability of leakage power for TFET CLA is worse than FinFET CLA, especially with WFV. The leakage power distribution of TFET CLA skews to larger values due to its worse I_{off} variability.

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Author Contributions

Author Yin-Nien Chen contributed to the literature search and coordinated the the research, discussion and prepared the manuscript. Author Chien-Ju Chen contributed to the simulated works, discussion and the manuscript. Author Dr. Ming-Long Fan and Dr. Vita Pi-Ho Hu contributed to the

technical suggestions and discussion. Author Prof. Pin Su guided this research work and contributed to technical discussions on device part about the impacts of intrinsic variations on TFET and FinFET devices. Author Prof. Ching-Te Chuang guided this research work and contributed to technical discussions on the circuit part and paper writing by reviewing all the results presented in this work and revising the technical writing and formatting of the manuscript.

Conflicts of Interest

The authors declare no conflict of interest.

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