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Modeling, Verification, and Signal Integrity Analysis of High-Speed Signaling Channel with Tabbed Routing in High Performance Computing Server Board

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Abstract: It is necessary to reduce the crosstalk noise in high-speed signaling channels. In the channel routing area, the tabbed routing pattern is used to mitigate far-end crosstalk (FEXT), and the electrical length is controlled with a time domain reflectometer (TDR) and time domain transmission (TDT). However, unlike traditional channels having uniform width and space, the width and space of tabbed routing changes by segment, and the capacitance and inductance values of tabbed routing also change. In this paper, we propose a tabbed routing equivalent circuit modeling method using the segmentation approach. The proposed model was verified using 3D EM simulation and measurement results in the frequency domain. Based on the calculated inductance and capacitance parameters, we analyzed the insertion loss, FEXT, and self-impedance in the frequency domain, and TDT and FEXT in the time domain, by comparing the values of these metrics with and without tabbed routing. Using the proposed tabbed routing model, we analyzed tabbed routing with variations of design parameters based on self- and mutual-capacitance and inductance.

Keywords: signal integrity (SI); high-speed signaling channel; tabbed routing; far-end crosstalk (FEXT); insertion loss; time domain reflectometer (TDR); time domain transmission (TDT); 3D EM simulation

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1. Introduction

Memory signaling systems require high-density and high-speed signaling in high-performance computing systems in applications for artificial intelligence and big data management. In high-performance memory signaling systems, a printed circuit board (PCB) is needed to route a high number of signal channels between the chip and the dual in-line memory module (DIMM). Figure 1 depicts a memory signaling system, including the central processing unit (CPU), PCB, and DIMM with major signal integrity (SI) design factors. To increase the speed of signaling in the memory system, it is necessary to reduce the time required by the high-speed signaling channel. Thus, to design high-speed signaling channels, the TDR impedance must be maintained at a constant value, while insertion loss and FEXT are minimized.

Within a limited space, the high density of the signaling channel causes unintentional signal degradation due to the increase in high-speed data transfer. The unintended interaction between signaling channels introduces crosstalk noise, which degrades the SI performance. In particular, FEXT is one of the dominant factors that degrades high-speed signaling channels. As a result, various attempts have been made to mitigate FEXT [1,2]. However, from an engineering perspective, the choice of mitigating FEXT by increasing the gap between channels or applying a new structure is not straightforward.

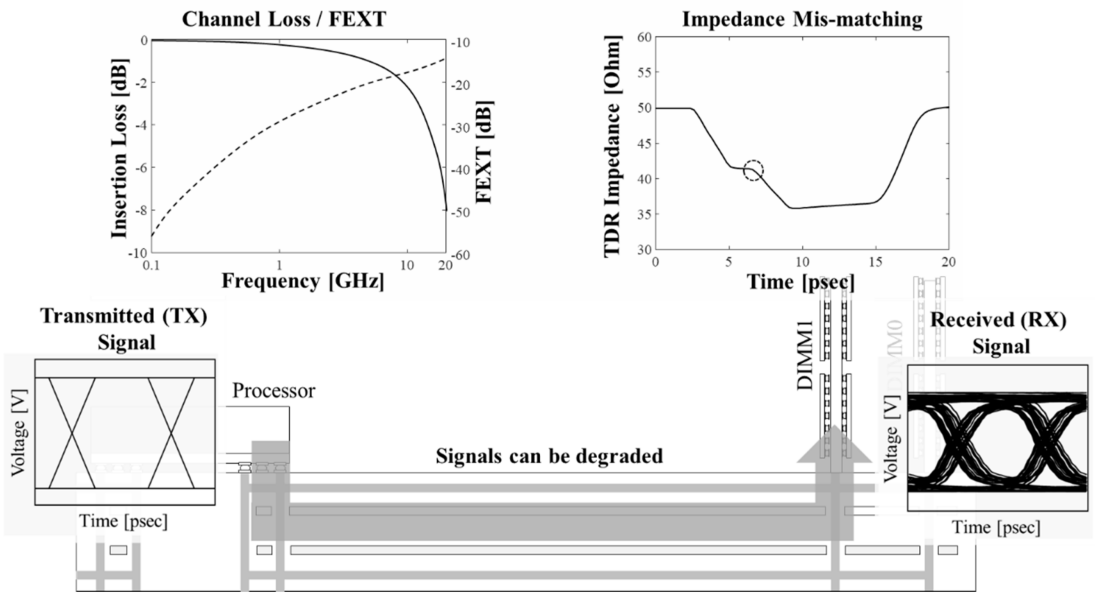
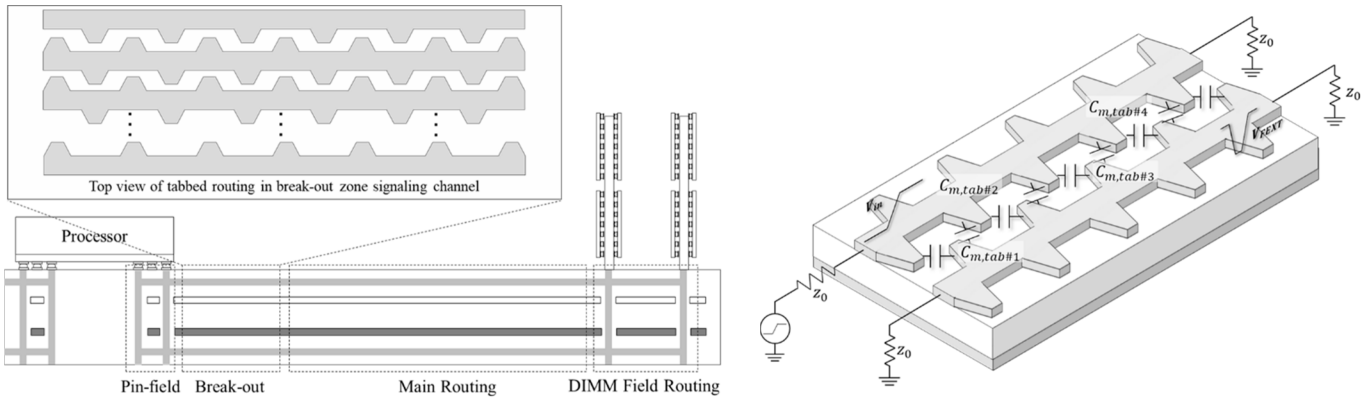


Figure 1. In the memory signaling system, the signal integrity (SI) issues of the high-speed signaling channel are shown. The received signals are degraded due to channel loss, far end crosstalk, and channel impedance mismatching. Thus, the design of the high-speed signaling channel must consider these SI issues.

For these reasons, a new routing pattern, named tabbed routing, was proposed and applied to micro-strip lines of high-performance server PCBs by Intel Corporation [3]. In general, when the CPU pins are out of the distributed pin field, the routing is performed using one bus consisting of eight DQ channels and two pairs of DQs, and the channels are routed with an even distance in the break-out zone. From the routing perspective, the routing from the CPU's pin becomes wider as it goes to the DIMM package. Thus, at the break-out zone where the spacing is narrow between the signaling channels, a trapezoid-shaped tab is added to the general signaling trace for tabbed routing, as shown in Figure 2a,b.



(**a**) (**b**)

Figure 2. (**a**) Conceptual image of high-speed signaling channel in a high-performance server board from CPU to DIMM socket. The channel continues from the processor to pin field routing, break-out zone routing, and main routing. In the break-out zone routing, tabbed routing is applied to reduce the far-end cross-talk (FEXT) and match the overall TDR impedance. (**b**) Conceptual image high-speed signaling channel with tabbed routing and induced far-end crosstalk (FEXT) due to the aggressor channel. Due to tabbed routing, the additional mutual capacitance is applied. By changing the ratio of mutual- and self-capacitance and mutual- and self-inductance, the FEXT voltage differs depending on the change of tab dimension.

As shown in Figure 2b, unlike a general micro-strip channel, an additional mutual capacitance, $C_{m,\,tab}$, is formed between the tab and the adjacent channel. The FEXT voltage is determined between the ratio of mutual- and self-capacitance, and the ratio of mutual- and self-inductance, as shown in Equation (1) below [3].

$$V_{FEXT}(t) = \frac{t_f}{2}\left(\frac{C_m}{C_{self}} - \frac{L_m}{L_{self}}\right)\frac{dV_i\left(t - t_f\right)}{dt} \quad (1)$$

However, not only is $C_{m,\,tab}$ additionally generated by tabs, but it also affects the mutual- and self-inductance and capacitance values of the channels. Furthermore, because the width and space of tabbed routing are not constant, it is a challenge to undertake modeling-based design and optimization that can minimize insertion loss and FEXT excluding 3D EM simulation and measurement.

In [4], a generalized equation-based tabbed routing model is proposed using the segmentation method with an asymmetrical coupled micro-strip line. The self- and mutual-capacitance is calculated based on the asymmetrical micro-strip line, and self- and mutual-inductance can be obtained from the calculated capacitance values. However, the self- and mutual-inductance values are affected by $C_{m,\,tab}$. Due to this difference in self- and mutual-inductance, the consistency of the tabbed routing model is degraded. Thus, to increase the accuracy of tabbed routing in relation to SI, a tabbed routing model based on more accurate inductance and capacitance values is needed.

In this paper, we propose improved modeling of tabbed routing using an asymmetrical coupled micro-strip line using the segmentation method. The calculation of the inductance is performed by considering the effect of the tab fringing capacitance value, thus improving the consistency of the overall inductance value in Section 2. In Section 3, for verification of the proposed modeling method, the manufactured PCB patterns and measurement set-up are shown.

The proposed tabbed routing model was verified by comparison of the insertion loss and FEXT for two tabbed routing designs, using 3D EM simulation and measurement results up to 20 GHz in the frequency domain. The proposed tabbed routing model was compared with the previous model in terms of insertion loss, FEXT, and self-impedance in frequency domain. In Section 4, we analyze the tabbed routing in terms of insertion loss, FEXT, self-impedance of Z_{11} in the frequency domain, and TDT and FEXT in the time domain, with and without tabbed routing. Furthermore, tabbed routing with design variations was compared and analyzed. Finally, we discuss the application of the high-speed signaling channel with tabbed routing to high-performance computing systems from the perspective of signal integrity. This SI perspective allows intuitive analysis of tabbed routing.

2. Modeling of High-Speed Signaling Channel with Tabbed Routing

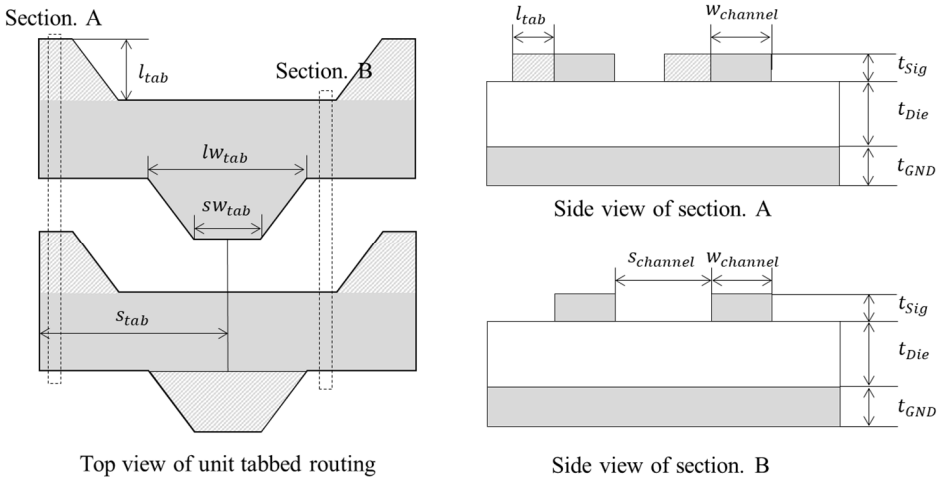
In this section, we introduce the signal integrity model and modeling procedure of the high-speed signaling channel with tabbed routing. Table 1 shows the structural parameters and definitions. Figure 3a shows the top and side views of one-unit tabbed routing. To aid understanding of the tabbed routing model, we illustrate one-unit tabbed routing in Figure 3a. In the segment A and B of Figure 3b, the channel width can differ due to the tab design parameters.

In the general micro-strip line structure, the characteristics of signaling trace, namely, insertion loss, FEXT, TDR, are determined by the dimension of the micro-strip line. Due to the non-uniform dimensions of the tabbed routing, the E- and H-fields are also non-uniformly formed through the signaling channel. Thus, it is difficult to analyze tabbed routing compared to the general micro-strip line. For this reason, reference [4] proposed modeling of tabbed routing using a segmentation method, as shown in Figure 3b. In reference [4], the capacitance and inductance were calculated for an asymmetrical coupled micro-strip line depending on the width and space change. In addition, for the fringing

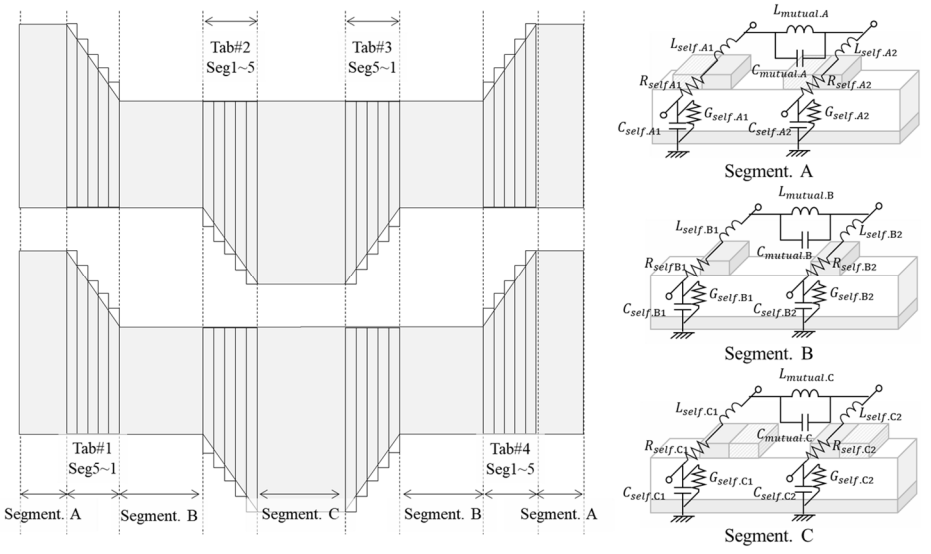
effect that occurs between tabs, an additional fringing capacitance was calculated and applied to the equivalent circuit model.

Table 1. Structural parameters and definition of the high-speed signaling channel with tabbed routing.

Parameter	Definition
$w_{channel}$	Channel width without tab
$s_{channel}$	Space between channels
lw_{tab}	Long width at tab
sw_{tab}	Short width at tab
l_{tab}	Length of tab
s_{tab}	Spacing between tab



(**a**)



(**b**)

Figure 3. (**a**) Top and side views of one-unit tabbed routing with the structural parameters. In contrast with the normal transmission line, tabbed routing is required to be modeled by a one-unit tab for signal integrity characteristics. (**b**) Conceptual image of the segmentation method for modeling of tabbed routing with the RLGC equivalent circuit model. Each segment is constructed as asymmetrical coupled micro-strip lines with different channel widths.

However, the inductance matrix values were calculated in a homogenous medium based on the capacitance value for a two-coupled asymmetrical micro-strip line, which occurs in the cross-section without reflecting the tab fringing effect [4].

Thus, in this paper, we proposed an improved modeling method, which can apply the tab fringing effect to the inductance value as shown in Figure 4. The proposed tabbed routing modeling method is constructed using the segmentation method, similar to that of reference [4]. First, the self- and mutual-capacitance values of the asymmetrical coupled micro-strip line are calculated using the equation of reference [4] from the fixed tabbed routing physical design parameters, as shown in Table 1.

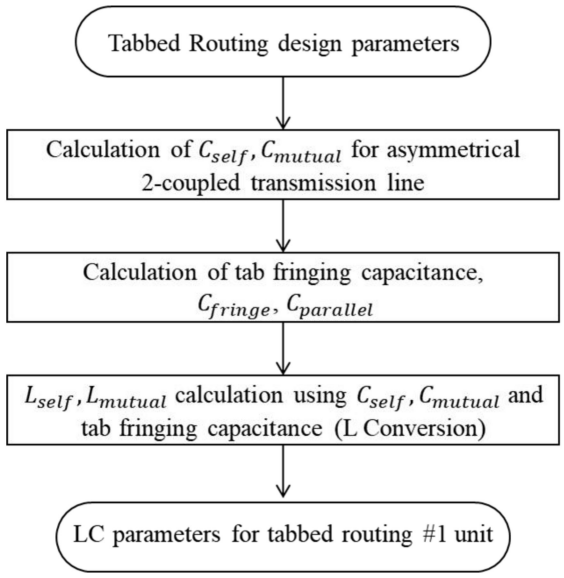


Figure 4. Proposed modeling procedure of tabbed routing is shown as block diagram based on segmentation method.

In Second, we calculate the fringing capacitance, C_{fringe}, using the fixed physical design parameters of tabbed routing. In the next step, unlike the calculation of self-and mutual-capacitance and inductance undertaken in ref. [4], the self- and mutual-inductance values are calculated through matrix calculation using the calculated self- and mutual-capacitance calculation results and fringing capacitance results. In this paper, we defined "L conversion" as an inductance matrix calculation that considers mutual-capacitance and tab fringing capacitance. Using the calculated inductance and capacitance values with resistance, and the conductance parameters, a one-unit tabbed routing model can be constructed. A detailed explanation of each step of the modeling procedure is provided in the next section.

The design parameters and definition are defined in Table 1 and Figure 3a. To obtain the total capacitance matrix, the partial capacitance parameters are illustrated in Figure 5.

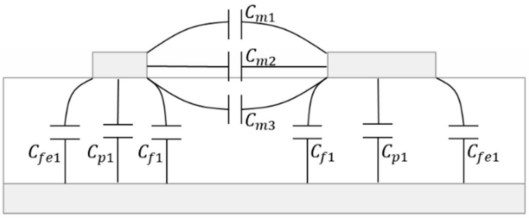


Figure 5. Cross-sectional view of coupled asymmetrical micro-strip lines and capacitance parameters. The capacitance parameters are configured by the design parameters of the coupled asymmetrical micro-strip line.

The capacitance matrix C for the two-coupled micro-strip line is:

$$C = \begin{bmatrix} C_{11} + C_m & -C_m \\ -C_m & C_{22} + C_m \end{bmatrix} \quad (2)$$

$$C_{11} = C_{f1} + C_{p1} + C_{fe1} \quad (3)$$

$$C_{22} = C_{f2} + C_{p2} + C_{fe2} \quad (4)$$

$$C_m = C_{m1} + C_{m2} + C_{m3} \quad (5)$$

The C matrix, Equation (2), is the frequency independent value, where C_{11}, C_{22}, C_m represent the self-capacitance values of line 1 and line 2 to ground, and mutual capacitance between line 1 and line 2, respectively.

Each capacitance value is formulated by Equations (3)–(5). From the design parameters, each capacitance value of the asymmetrical micro-strip line can be calculated using the equations from reference [5].

The tab fringing capacitance is calculated in the second step. In contrast to normal micro-strip lines, there is an additional tab fringing mutual-capacitance between tabs. The E-field distribution result of tabbed routing is plotted in Figure 6a. In general, the E-field vector of the micro-strip line is generated in the direction perpendicular to the direction of the electromagnetic wave. However, due to the tab, the E-field vector is distributed differently, as shown in Figure 6a. It is shown that the E-field distribution is divided into an oblique tab and the edge of the Table Fringing capacitance modeling is performed through the field for each part, as shown in Figure 6b,c [4].

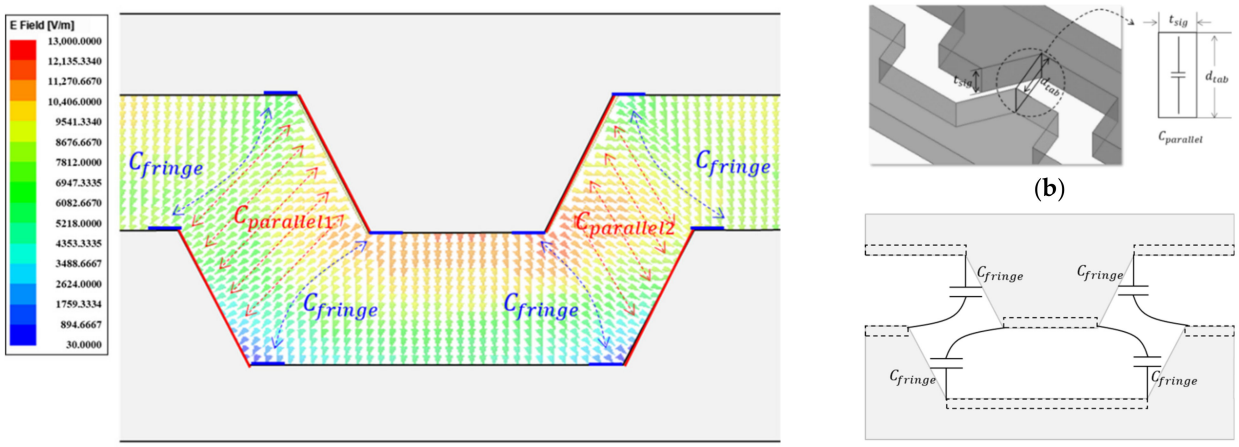


Figure 6. (**a**) Simulation result of E-field vector shown with tabbed routing. In contrast to the micro-strip line without a tab, in which an E-field in one direction is formed, for tabbed routing, an oblique E–field can be seen between the oblique tabs and fringing E-field at the top of the Table (**b**) The oblique tab is coupled with an adjacent oblique tab; the tabs are considered as parallel plates. (**c**) The edge of the tab has a fringing effect on the coupled line between tabs.

Figure 6b introduces two different fringing capacitance models according to the distribution of the E-field [4]. First, for the oblique slope, the parallel surfaces face each other, and $C_{parallel}$ can be calculated using Equation (6):

$$C_{parallel} = \varepsilon_r \varepsilon_0 \frac{t_{sig}}{d_{tab}} \ [F/m] \quad (6)$$

$$d_{tab} = \sqrt{(s_{channel} - l_{tab})^2 + \left(s_{tab} - \frac{(lw_{tab} + sw_{tab})}{2}\right)^2} \quad (7)$$

Next, as shown in Figure 6c, the fringing capacitance, C_{fringe}, is introduced via Equations (8)–(10) [4]:

$$C_{fringe} = \frac{C_t - C_{cp}}{2} \tag{8}$$

$$C_t = \frac{1}{c_0 Z_c} \tag{9}$$

$$C_{cp} = \varepsilon_r \varepsilon_0 \frac{l w_{tab}}{s_{channel} - l_{tab}} \tag{10}$$

In this paper, Equations (6)–(10) were applied to calculations based on air, the medium in which the E-field is distributed between the two-coupled micro-strip line without passivation. In addition, the proposed model is considered in an ideal micro-strip line, and the PCB etching effect is not considered. By applying the additional mutual capacitance, C_{fringe} and $C_{parallel}$, between adjacent tabs, the oblique E-field that is caused by the tabs can be approximately considered. Using the two steps mentioned above, the modeling of tabbed routing reflecting the tab effect can be undertaken. However, to increase the consistency of the modeling method, we propose and introduce an additional step. The inductance matrix of the two-coupled asymmetrical micro-strip line, L, can be calculated using Equation (11):

$$L = \begin{bmatrix} L_{11} & L_m \\ L_m & L_{22} \end{bmatrix} = \frac{1}{v_s^2} \cdot U_{2\times2} \cdot C_{air}^{-1} \tag{11}$$

Due to velocity splitting in the propagation model in non-homogeneous media [5], the inductance matrix, L, can be obtained using C_{air}, which is calculated by converting the dielectric material to air, where v_s is the wave velocity and $U_{2\times2}$ is the 2×2 identity matrix. However, the inductance calculation using Equation (11) cannot reflect the fringing capacitance value calculated in step 2.

From the perspective of the equivalent circuit model of tabbed routing, $C_{parallel}$ and C_{fringe} can be considered to be connected to each segment in series with mutual-capacitance as the half-value. Thus, the inductance at tab segments 2, 3, and 4, which are connected with $C_{parallel}$, can be calculated using Equation (12):

$$L_{tab} = \frac{1}{v_s^2} \cdot U_{2\times2} \cdot \begin{bmatrix} C_{air,\,11} & C_m || \frac{C_{parallel}}{2} \\ C_m || \frac{C_{parallel}}{2} & C_{air,\,22} \end{bmatrix}^{-1} \tag{12}$$

For the edge of the tab, the inductance at tab segments 1 and 5, which are connected with C_{fringe}, can be calculated using Equation (13):

$$L_{fringe} = \frac{1}{v_s^2} \cdot U_{2\times2} \cdot \begin{bmatrix} C_{air,\,11} & C_m || \frac{C_{fringe}}{2} \\ C_m || \frac{C_{fringe}}{2} & C_{air,\,22} \end{bmatrix}^{-1} \tag{13}$$

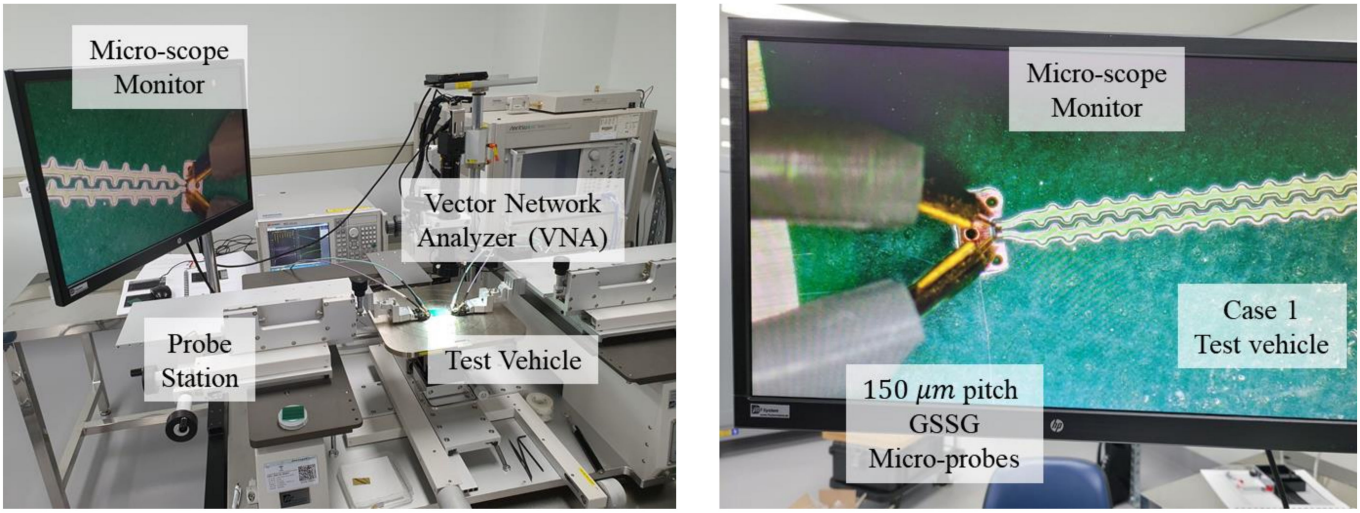
Using these three inductance calculation equations, a tabbed routing model can be configured, in which the inductance and capacitance models considering tab fringing capacitance is applied. To verify the proposed modeling and to compare results with the previous model [4] without the L conversion effect, the insertion loss and FEXT results were obtained using the proposed model. These results are compared using measurement and 3D EM simulation in the frequency domain in the following section.

3. Frequency Domain Verification of High-Speed Signaling Channel with Tabbed Routing

In this section, the proposed tabbed routing model is verified by comparing the measurement and 3D EM simulation results in the frequency domain. Six cases of micro-strip lines, as described in Table 2, were measured and used for the verification.

Table 2. Physical dimensions and material properties of test patterns for verification corresponding to Figure 7 (unit: mm).

Parameter	Case 1 (Tab #1)	Case 2 (Tab #2)	Case 3 (w/o Tab #1)	Case 4 (w/o Tab #2)	Case 5 (w/o Tab #3)	Case 6 (w/o Tab #4)
$w_{channel}$	0.102	0.102	0.102	0.102	0.165	0.165
$s_{channel}$	0.2	0.3	0.2	0.3	0.2	0.3
lw_{tab}	0.17	0.12	-	-	-	-
sw_{tab}	0.1	0.1	-	-	-	-
l_{tab}	0.1	0.19	-	-	-	-
s_{tab}	0.2	0.3	-	-	-	-
t_{sig}	0.042					
t_{Die}	0.06 ($\varepsilon_r = 4.2$, $tan\delta = 0.015$)					
$length$	30					



(**a**) (**b**)

Figure 7. (**a**) Measurement environment for experimental verification of the tabbed routing model. A VNA is used for insertion loss and FEXT measurement in the frequency domain. (**b**) Micro-scope image of the GSSG probe and test vehicle (case 1).

3.1. Test Patterns and Measurement Set-Up

For the verification of the proposed model, we manufactured the PCB following the design of Table 2. Cases 1 and 2 comprise tabbed routing, which target the break-out zone and main routing shown in Figure 2a. Cases 1 and 2 were manufactured for the verification of the proposed tabbed routing model, so that tabs exist on both sides, as shown in Figure 2b. As shown in Table 2, the signal trace width of the manufactured PCB patterns, which is less than 1 mm, is very narrow compared with the signal pin width of the SMA connector ($\approx$ 1 mm). Thus, to minimize the measurement error for test patterns, the micro-probing patterns were applied to the test PCBs. Measurements were conducted at the probe station as shown in Figure 7a,b, which shows that case 1 of the test PCB pattern was connected with a 150 μm pitch GSSG micro-probe through a vector network analyzer (VNA) to measure the insertion loss and FEXT in the frequency range of 100 MHz to 20 GHz.

Furthermore, we manufactured additional test patterns for the analysis of tabbed routing. For instance, cases 1, 2, 3, and 4 have the same physical dimensions except for the difference of the presence or absence of tabs. When ε_r of the dielectric material is 4.2 and tan δ is 0.015, cases in which the width is 0.1016 mm without a tab (cases 3 and 4) have a characteristic impedance of close to 45 ohms; cases in which the width is 0.165 mm without a tab (cases 5 and 6) are similar to those of cases 1 and 2. From the comparative analysis of cases 1, 3, and 5, and cases 2, 4, and 6, we investigated the effect of the tab on the insertion loss and FEXT in the frequency domain.

3.2. Verification and Analysis of High-Speed Signaling Channel with Tabbed Routing

For the frequency domain verification, the tab designs of cases 1 and 2 were compared using VNA measurement and 3D EM simulation in terms of insertion loss and FEXT results, as shown in Figure 8. The insertion loss and FEXT results are compared in the frequency range of 100 MHz to 20 GHz. Modeling of the tabbed routing of cases 1 and 2 shows that the insertion loss of the proposed model well matches that of the simulation results. Due to the effect of the probing pad and the extended signal trace for the VNA measurement, it can be seen that there a difference exists between the measurement results and the other two sets of results. Although there are some insertion loss differences compared to the measurement results in Figure 8a,c, it can be seen that the oscillation of the insertion loss due to impedance mismatching is similar.

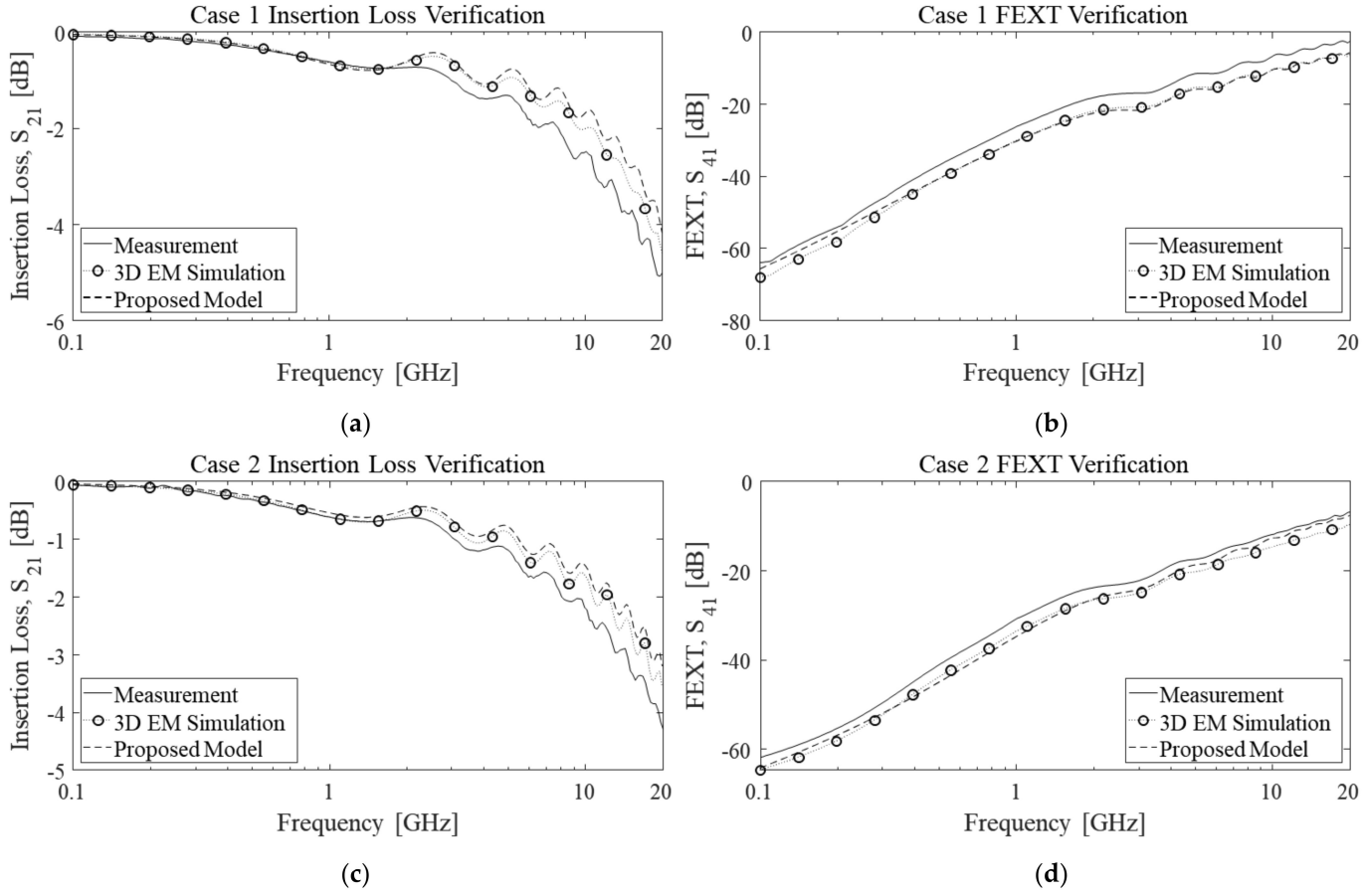


Figure 8. Frequency domain verification of the proposed model by comparison of VNA measurement and 3D EM simulation. The proposed model of case 1 is verified for (**a**) insertion loss and (**b**) FEXT; and the proposed model of case 2 with different tab designs is verified for (**c**) insertion loss and (**d**) FEXT.

In addition, when comparing the FEXT results of cases 1 and 2, Figure 8b,d shows that the FEXT of VNA measurement, 3D EM simulation, and the proposed model are well matched. Thus, by comparing the insertion loss and FEXT results in the frequency domain, the proposed model is matched well with measurements and 3D EM simulation. Next, we analyze the proposed modeling according to each modeling step as shown in Figure 4. The modeling of each step is compared with the proposed model and 3D EM simulation in the frequency domain, using the design of case 1 with or without $C_{parallel}$, C_{fringe}, and L conversion, as shown in Figure 9. As shown in Figure 9a, no significant difference occurs in the insertion loss due to the absence and presence of $C_{parallel}$ and C_{fringe}, which are marked with diamonds, stars, and circles. Overall, prior to 1 GHz, the insertion loss is dominated by the conductor loss, which is affected by the skin and proximity effects [6]. From the

perspective of the equivalent circuit model for the transmission line, the insertion loss is affected by the self-capacitance and -inductance after 1 GHz. As mentioned in Equation (1), FEXT is determined by the difference between the ratio of self- and mutual-inductance and -capacitance. At this point, $C_{parallel}$ and C_{fringe} can result in additional mutual capacitance. Because the mutual-capacitance increases while the self-capacitance and self- and mutual-inductance are fixed, FEXT can degrade as $C_{parallel}$ and C_{fringe} are applied. As shown in Figure 9b, the FEXT results are compared as $C_{parallel}$ and C_{fringe} are applied. The FEXT results of three models—(1) without $C_{parallel}$, without C_{fringe}; (2) with $C_{parallel}$, without C_{fringe}; and (3) with $C_{parallel}$, with C_{fringe}—degrade due to additional mutual capacitance.

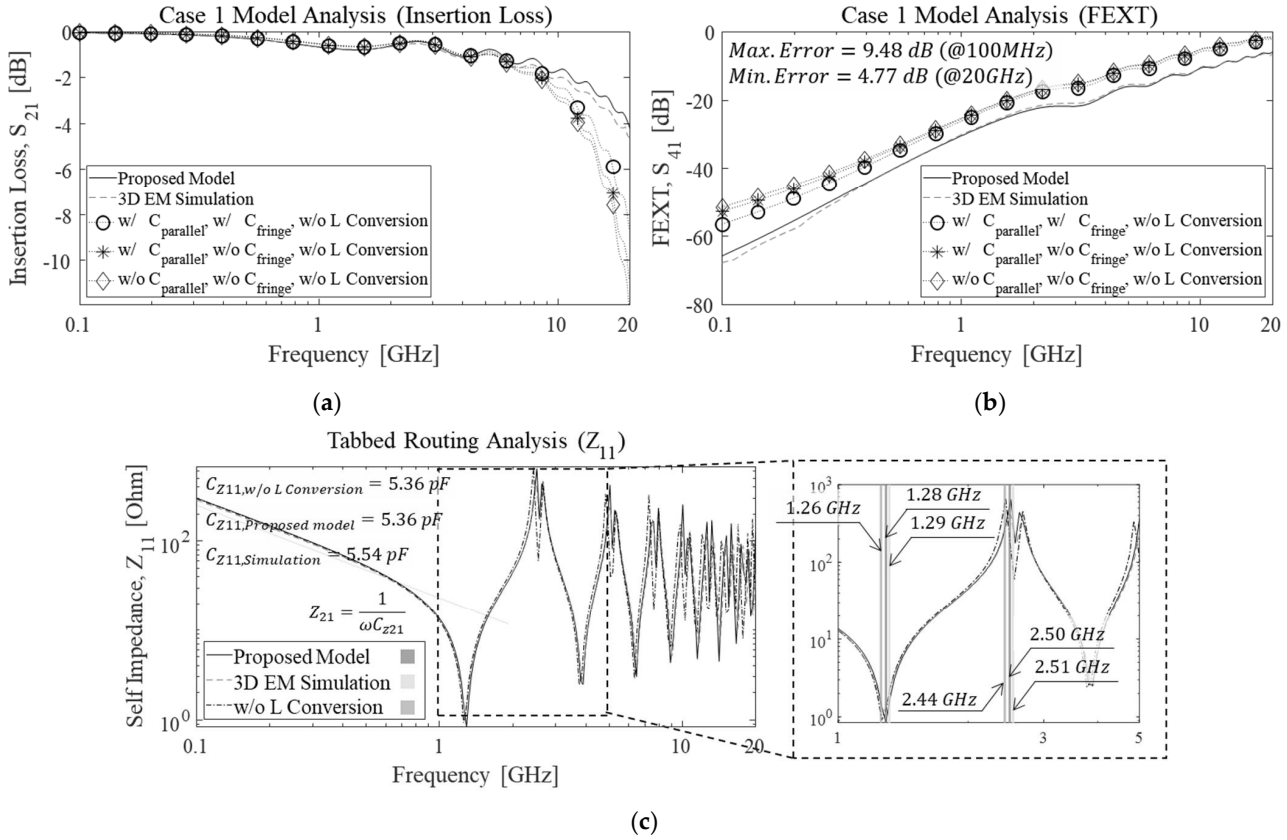


Figure 9. Frequency domain analysis of the proposed model with or without $C_{parallel}$, C_{fringe}, and L conversion for comparison of (**a**) insertion loss, (**b**) FEXT, and (**c**) self-impedance, Z_{11}. For insertion loss and FEXT, five of the results with or without $C_{parallel}$, and with or without C_{fringe}, are compared in each graph. For the self-impedance graph, three different results, namely, those of the 3D EM simulation, the proposed model, and the model without L conversion, are shown and compared in the same plot.

In addition to the effect of $C_{parallel}$ and C_{fringe}, the effect of L conversion considering $C_{parallel}$ and C_{fringe}, which is proposed in Section 2, is also compared for insertion loss and FEXT as non-marked straight line. Analysis of the inductance and capacitance parameter, self-impedance, Z_{11}, is shown in Figure 9c. Due to the L conversion, no difference exists in the capacitance values, as shown in Figure 9c. The self-impedance shows that the impedance under 1 GHz is the capacitive region. The capacitance value is calculated using Equation (14):

$$Z_{11} = \frac{1}{\omega C} \tag{14}$$

Using Equation (14), the capacitance value of self-impedance can be compared; the capacitance values from two models are the same, i.e., 5.36 pF. However, for the series resonance around 1.2 GHz, it can be seen from Figure 9c that the proposed model with L

conversion is closer to the resonance frequency of the 3D EM simulation. In addition, the figure also shows that inductance and capacitance parallel resonance occurs above 1.2 GHz. In addition, using the proposed model obtained through L conversion shows that the insertion loss and FEXT have results closer to those of the 3D EM simulation. From these results, the proposed model is verified via 3D EM simulation and measurement, indicating that the accuracy of signal integrity analysis is increased using the proposed model.

4. Signal Integrity Analysis of High-Speed Signaling Channel with Tabbed Routing

In this section, tabbed routing is analyzed in terms of signal integrity (1) with and without tabs, and (2) with variation of design parameters in the frequency domain and time domain.

4.1. Signal Integrity Analysis of High-Speed Signaling Channels with and without Tabs

Figure 10 plots cases 2, 4, and 6. Case 2 comprises tabbed routing with different tab designs, and spacing between signal traces of 0.3 mm. Case 4 is the pattern without tabs from case 2. Case 6 is the case in which the channel width is increased from 0.102 mm to 0.165 mm in case 4. Thus, case 2 is compared according to two different channel widths and without a tab, respectively. In case 4, the channel width is 0.102 mm and the TDR impedance is 45 ohms. Unlike case 4, case 6 has a channel width of 0.165 mm and a TDR impedance of 35 ohms. The TDR impedance of the tabbed routing of case 2, which has the same channel width as that of case 4, has a TDR impedance of 38 ohms. Due to these impedance differences, the insertion loss oscillation is shown in Figure 10a. Cases 1 and 5, and cases 2 and 6, which have similar TDR impedance, show similar oscillation, whereas cases 2 and 4 have a linear insertion loss due to 50 ohm of TDR impedance matching. It can be seen that, except for the difference due to TDR impedance mismatching, no difference occurs due to the additional insertion loss caused by the tab.

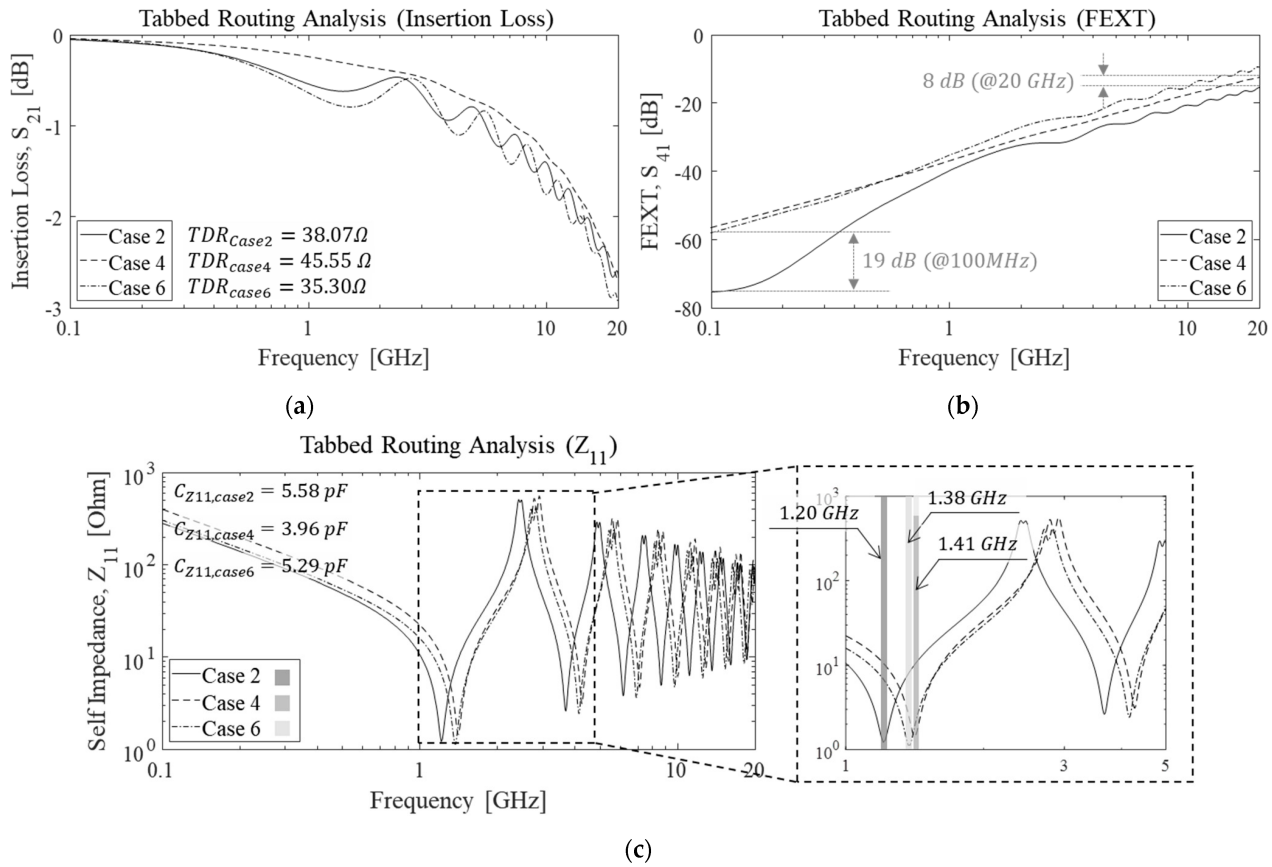


Figure 10. Frequency domain analysis of tabbed routing with or without tabs for comparison of cases 1, 3, and 5 in terms of (**a**) insertion loss, (**b**) FEXT, and (**c**) self-impedance, Z_{11}; and cases 2, 4, and 6 in terms of (**c**) insertion loss.

In contrast to the difference in insertion loss, Figure 10b shows that the FEXT results of tabbed routing in case 2 are degraded compared with other cases, i.e., cases 4 and 6. In particular, around 100 MHz, the FEXT value differs by up to 20 dB. To analyze the results of FEXT shown in Figure 10b, the self-impedance, Z_{11}, is plotted in Figure 10c. In Figure 10c, the capacitance value of self-impedance is calculated for each case. The capacitance value of case 1 is close to the capacitance value of case 6, which has a channel width of 0.165 mm. As tabs are applied from case 4, the capacitance value increases, similar to the case when the channel width increases to 0.165 mm. In addition, for cases 2 and 6, the LC series resonance frequency value is different although the capacitance value is similar. Using Equation (15), the inductance value of self-impedance can be calculated using the resonant frequency and the capacitance value of self-impedance:

$$f_{resonance} = \frac{1}{2\pi\sqrt{LC}} \tag{15}$$

The calculated inductance value of cases 2, 4, and 6 are 3.15, 3.21, and 2.51 nH, respectively, at a resonance frequency of approx. 1.2 GHz. From the calculated values, the inductance of tabbed routing is smaller than that of case 4 and larger than that of case 6. Furthermore, to analyze the self- and mutual- inductance and capacitance values according to the tabbed routing, the LC values are extracted using ANSYS Q3D simulation in Table 3. From the extracted self- and mutual-inductance and capacitance values, it can be seen that the mutual capacitance value is very large compared to the other cases, whereas the inductance value is small. In Table 3, the self-capacitance value of case 2 is 5.16 pF, which is a 67.5% increase compared to case 4, and a 2.08% increase compared to case 6. In addition, the mutual-capacitance value is 0.16 pF, which is a 5.3-fold increase compared to case 4, and a 1.2-fold increase compared to case 6. It can be seen that the mutual capacitance value increases significantly as the contact surface between channels increases when tabs are applied. As mutual- and self-capacitance increase due to the application of tabs, the inductance value is reduced compared to the cases in which there are no tabs. As a result, the FEXT of case 2 is degraded compared to that of cases 4 and 6.

Table 3. Comparison of self- and mutual-capacitance and self- and mutual-inductance values at 20 GHz for cases 2, 4, and 6 extracted from Q3D simulation.

Parameter	Case 2	Case 4	Case 6
C_{self} $[pF]$	5.16	3.08	4.27
C_{mutual} $[pF]$	0.16	0.03	0.04
L_{self} $[nH]$	8.07	16.83	15.02
L_{mutual} $[nH]$	0.41	4.00	3.11

Next, for SI analysis in the time domain, Figure 11 shows the time domain simulation set-up. TDT and FEXT simulation results were derived using the comparison of cases 2, 4, and 6. For the time domain simulation set-up, the parameters of the simulation were fixed based on the expected specification of DDR5 of 4.8 Gbps. In Figure 11b, the TDT simulation results are compared to analyze the time delay due to the tab effect. The time delay is configured by the total inductance and capacitance values.

As shown in Figure 10c, the resonance frequency of the self-impedance value is higher compared with that of other cases. Case 2 has the largest product of self-impedance inductance and capacitance, and the longest time delay with a difference of a maximum of 33 psec. In terms of signal transmission, the time delay can be adjusted by applying tabs within the same length. As shown in Figure 11c, FEXT also appears later in case 2 due to the difference in signal transmission velocity. Case 2 also has the smallest FEXT voltage of 18 mV, as shown in the frequency domain FEXT results. Comparisons of cases 2, 4, and 6 in the frequency and time domains show that tabbed routing has a lower FEXT voltage compared with cases 4 and 6, which do not have tabs. Comparison of cases 2 and 6 with

similar TDR impedance shows that tabbed routing can result in time delays, thus allowing controllable routing while reducing FEXT noise.

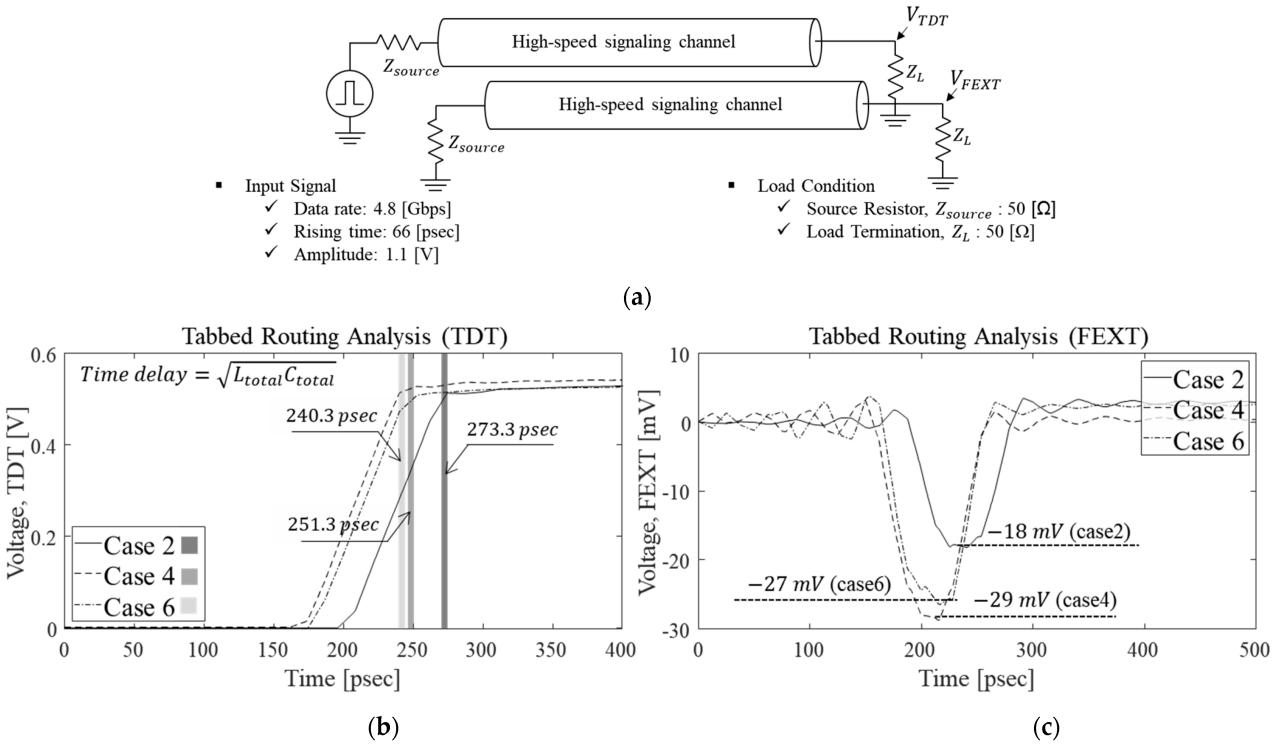


Figure 11. (**a**) Time domain simulation set-up. To evaluate SI in the time domain, the simulation parameters, including the rising time and amplitude suitable for the 4.8 Gbps target, were set. Using this set-up, SI analysis is conducted for (**b**) TDT, and (**c**) FEXT for the comparison of cases 2, 4, and 6.

4.2. Signal Integrity Analysis of Tabbed Routing with Variation of Design Parameters

As shown in Figure 12, the insertion loss, FEXT, and TDR impedance results were compared and analyzed with variations of three different tabbed routing design parameters, s_{tab}, lw_{tab}, and l_{tab}. For the TDR impedance analysis, the simulation set-up was conducted as illustrated in Figure 11a.

First, as the parameter s_{tab} increases, the ratio occupied by the channels and the self-capacitance value decrease. Because the proportion of occupied channels decreases, both the coupling between channels and the mutual capacitance also decrease. Compared to the change in capacitance value, the inductance value does not change significantly, and the TDR impedance increases as s_{tab} increases. Thus, Figure 12a,c shows the insertion loss in the case of s_{tab} = 0.4 mm with the TDR impedance approaching 40.91 ohms. In addition, as the ratio of the capacitance value decreases, the FEXT coupling value increases, as shown in Figure 12b.

Second, the insertion loss, FEXT, and TDR impedance results are shown and compared in Figure 12d–f with a variation of lw_{tab}. Changing the lw_{tab} parameter affects the value of $C_{parallel}$, but does not significantly affect the value of C_{fringe}. Thus, the variation of lw_{tab} does not change the mutual-capacitance but changes the self-capacitance due to the change in the density of metal in the limited area.

Unlike the previous s_{tab} variation, because the change in its value is not large, the insertion loss and FEXT results do not change significantly. In addition, the TDR impedance decreases by about 1 ohm as the lw_{tab} increases because the capacitance value increases and the inductance value does not change significantly, as shown in Figure 12f.

Third, the insertion loss, FEXT, and TDR impedance results are shown and compared in Figure 12g–i with a variation of l_{tab}. When the l_{tab} parameter changes, C_{fringe} and $C_{parallel}$

change together. Thus, as l_{tab} increases, mutual- and self-capacitance values also increase. In addition, when l_{tab} increases, the distance between adjacent channels is reduced, so the mutual inductance value increases. However, because the ratio of mutual- and self-capacitance becomes larger than the ratio of inductance, the FEXT value decreases, as shown in Figure 12h. These results can also be shown for the insertion loss and TDR impedance values, in which TDR impedance decreases as the capacitance value of the channel increases.

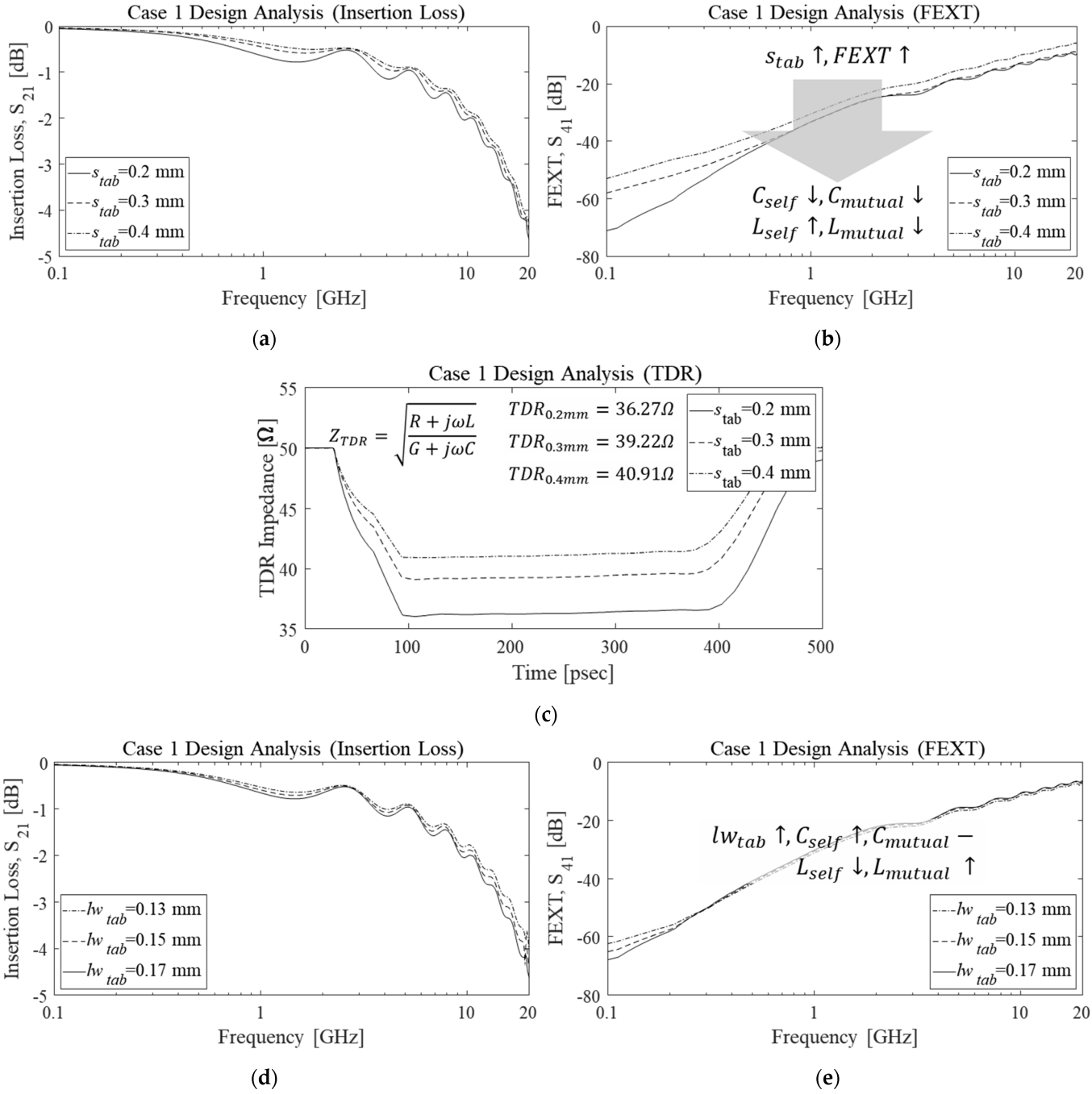


Figure 12. *Cont.*

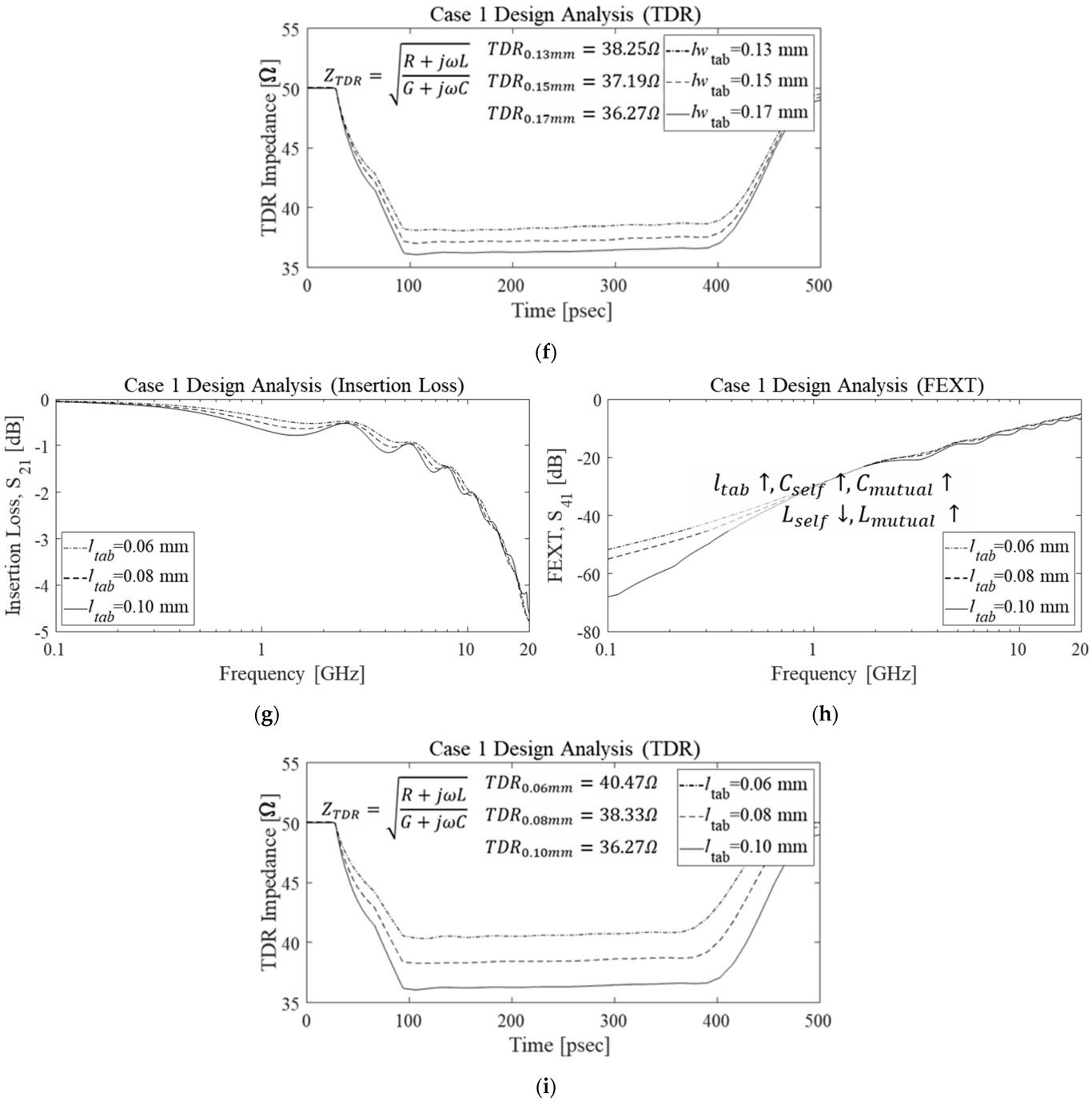


Figure 12. Results of frequency domain analysis of insertion loss and FEXT are shown with the variation of three tabbed routing design parameters. Comparison of (**a**) insertion loss, (**b**) FEXT, and (**c**) TDR impedance results for s_{tab} variation. Comparison of (**d**) insertion loss, (**e**) FEXT, and (**f**) TDR impedance results for lw_{tab} variation. Comparison of (**g**) insertion loss, (**h**) FEXT, and (**i**) TDR impedance results for l_{tab} variation.

Furthermore, from the time domain perspective, the simulation of three coupled channels was conducted, as shown in Figure 13a. Using this simulation, when a victim channel exists between two aggressors, the effect of the two aggressors is shown through TDT results. Due to the two aggressors, the victim channel is affected by the time delay for cases 1, 3, and 5, as shown in Figure 13b–d.

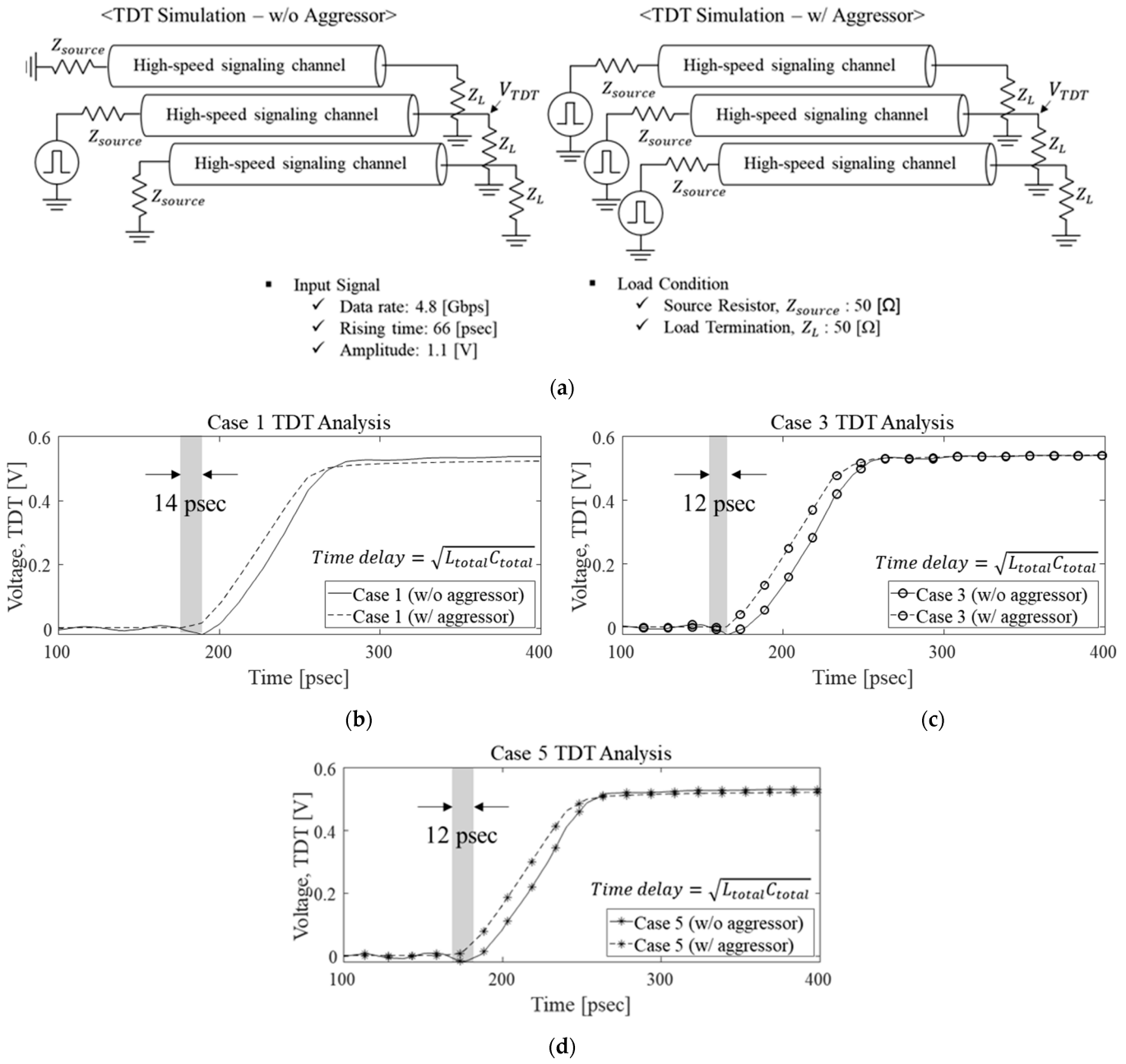


Figure 13. (**a**) Time domain simulation set-up for three coupled channels. To evaluate the effect of two aggressor channels in the time domain, the simulation parameters, including the rising time and amplitude suitable for the 4.8 Gbps target, were set. Using this set-up, the effect of the two aggressor channels is shown for (**b**) case 1, (**c**) case 3, and (**d**) case 5 with and without an aggressor source.

As the tab is applied, the time delay increases but the effect of the two aggressors is not significantly different from that in cases 3 and 5. As shown in Figure 13b, the time delay increases due to the two aggressors, resulting in an increase in the mutual- and self-inductance and capacitance due to the coupled aggressor traces. The increase in the time delay is only about 2 psec.

Depending on the presence or absence of tabs or design parameters, this analysis shows the characteristics of tabbed routing in the time domain using the TDT, TDR, and FEXT simulation. The results indicate that tabbed routing could be applied more easily in the design of high-speed signaling channels.

5. Conclusions

As the demand for high-performance computing systems increases, high-speed signaling channels should be designed in the high-frequency range with degraded loss for reliable data transmission. A high-speed signaling channel with tabbed routing has an advantage in terms of signal integrity while degrading the coupling between channels.

In this paper, we proposed and verified a tabbed routing model with an improved equivalent self- and mutual-inductance model that considers tab fringing capacitance. In frequency domain verification, we compared the insertion loss and FEXT of VNA measurement using manufactured PCBs with different tab designs. From the comparison of the measurements and 3D EM simulation, the proposed model was successfully verified in the frequency domain. In addition, the proposed model was compared with the previous tabbed routing model in the frequency domain. The effect on the L conversion proposed in this paper was shown in terms of the insertion loss, FEXT, and self-impedance of Z_{11}. In addition, we showed that the insertion loss, FEXT, and self-impedance of the proposed model match better than those of the previous model. After verification, using the proposed model we analyzed the signal integrity of high-speed signaling channels with and without tabs in the frequency and time domains. Tabbed routing was investigated using inductance and capacitance parameter analysis; results showed that FEXT degraded when tabs were applied to channels with the same space. Tabbed routing analysis also showed that tabbed routing has a larger value of mutual capacitance than that of the channel without tabs due to the increase in the facing area between channels. Furthermore, tabbed routing not only has the advantage of degrading FEXT, but also controls the TDR impedance and time delay without changing the width or space of the channel within a defined area. Using the proposed model, we also analyzed tabbed routing based on the variation of three design parameters in the frequency domain.

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