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An Optimal Digital Filtering Technique for Incremental Delta-Sigma ADCs Using Passive Integrators

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Abstract: This paper presents an optimal digital filtering technique to enhance the resolution of incremental delta-sigma modulators (incremental DSMs, IDSMs) using a low-power passive integrator. We first describe a link between a passive integrator and its impact on the output of the IDSM. We then show that the optimal digital filter design can be cast as a convex optimization problem, which can be efficiently solved. As a test vehicle of the proposed technique, we use a behavioral 2nd-order IDSM model that captures critical non-idealities of the integrator, such as gain compression and output saturation. The effectiveness of the presented technique is verified using extensive simulations. The result shows that the presented filtering technique improves signal-to-noise and distortion ratio (SNDR) by 15 dB–20 dB, achieving SNDR over 90 dB when the oversampling ratio (OSR) = 256, and this corresponds to best-in-class performance when compared to previously published DSM designs using passive integrators.

Keywords: analog-to-digital converter; delta-sigma modulator; extended ranging; passive integrator; digital calibration; optimal filtering

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1. Introduction

High-resolution and low-bandwidth analog-to-digital converters (ADC) are essential building blocks in various sensor and IoT applications. Traditionally, delta-sigma ADCs have been the dominant architecture for designing such ADCs since it can aggressively reduce the quantization noise for a sufficiently high oversampling ratio. However, the delta-sigma modulator (DSM) requires an integrator to realize the noise-shaping, thereby necessitating a power-hungry operational amplifier (op-amp) in the design. Since the power efficiency of op-amps does not directly improve with finer process nodes, such a design requirement remains a challenge when one wants to design a low-power, high-resolution ADCs in highly scaled technologies.

To address this challenge, there have been quite a few works that explored alternative design approaches that aim to achieve quantization noise shaping without op-amps. For instance, [1] uses an open-loop integrator based on a dynamic amplifier in a DSM to realize 3rd-order noise shaping. While using a dynamic amplifier may lead to lower power, it is vulnerable to process and temperature variation. As a more aggressive approach, one can use passive DSMs by removing amplifiers in the design [2–5]. Such implementations, however, suffer from the lack of a gain element. For example, the fully passive second-order DSM in [3] is constrained by the noise performance of the quantizer because the signal at the input of the quantizer is only 100 μV_{rms}. The authors in [4] compare a fully passive and a conventional DSM designed in the same process, revealing that the fully passive DSM exhibits 10 dB less SNDR than the conventional one. To overcome this challenge, hybrid approaches that mix both active and passive integrators have been explored [6–11]. The continuous-time (CT) DSM in [6] uses a two-pole active integrator structure, thereby using only two amplifiers for a 4th-order CTDSM. The 5th-order CTDSM in [7] uses a power-hungry op-amp only for the first integrator, while the rest of the four stages are passive

and g_m-C integrators. The downside, however, is that leakage in the passive integrators degrades overall noise performance, leading to a measured SNDR of only 63.4 dB. Similarly, in [8], the third-order discrete-time DSM uses a single op-amp to realize g_m-C integrator and two other poles are implemented as passive integrators, ending up with a dynamic range of only 54 dB. The 2-1 multi-stage noise shaping (MASH) CTDSM in [10], which is also a hybrid topology with a passive RC-integrator and a low-gain amplifier, achieves a slightly higher SNDR of 72 dB thanks to the digital cancellation logic that takes care of variations in open-loop gain and passive element values. The work in [11] is the most recent article that thoroughly studies the design tradeoffs of active-passive hybrid structure for designing DSMs, achieving 88 dB of SNDR with OSR of 260 from their discrete-time third-order DSM. High SNDR, however, is mainly attributed to their new third-order structure utilizing local feedbacks that realize zeros in the noise transfer function (NTF) of the DSM, and finding several design parameters is not straightforward. For instance, authors in [11] reported that seven interdependent gain parameters had to be found by recursive behavioral simulations.

Our foregoing reviews on prior publications share common design approaches aiming to overcome limitations of using low-power passive integrators—First, they rely upon some gain elements to get over the noise penalty of using passive integrators. Second, to overcome the integrator leakage inherent in passive integrators, compensation techniques such as digital cancellation logic [10] or optimized NTF zero in analog circuits [11] are used. The challenge in these cases is the lack of straightforward methods for finding the design parameters for the compensation, which is the motivation of this work.

This paper presents an optimal digital filtering technique that can enhance the linearity of a DSM utilizing hybrid passive-active integrators. We present a straightforward method for finding design parameters of the optimal digital filter without uncertainty. A test vehicle of the proposed filtering technique is a 2nd-order incremental DSM (IDSM) having an extended-range (ER) function [12,13] to further enhance the resolution. The main reason for choosing this architecture is the simplicity of the topology that does not suffer from instability as well as the potential to achieving high SNDR beyond 90 dB.

Our method is based on two recognitions that (1) the optimal digital decimation filter structure for IDSMs using leaky integrators must be redefined for the best possible SNR, and (2) the residual signal at the output of the last leaky integrator in a DSM can be combined with a filtered DSM output to further enhance the resolution of ADC. Conceptually, (2) has been demonstrated in DSMs using a conventional active integrator based on high-gain op-amps [12,13]. Our contribution, however, is showing that such an extended range method can still be applied to the DSMs using leaky integrators if a proper digital filtering technique is applied. Table 1 compares the main distinctions between our work and prior works utilizing hybrid active-passive integrators.

Table 1. Comparison with other analog-to-digital converters (ADCs) using passive integrators.

	This Work	**[1]**	**[4]**	**[11]**
Structure of ADC	2nd DT + ER	NS-SAR	2nd DT DSM	3rd DT DSM
Structure of integrator	P-H	H	A-A and P-P	P-H-H
Incremental?	Yes	No	No	No
Optimal digital filter?	Yes	No	No	No

P: passive, A: active-Resistor-Capacitor (RC), H: hybrid (passive + gain), DT: discrete time.

Section 2 reviews the fundamentals of incremental DSMs using leaky integrators and the theoretical foundation of the optimal digital filtering method. Section 3, which is the main contribution of this work, describes a straightforward procedure for finding tap weights of the optimal digital filter. Section 4 discusses design concerns when implementing DSMs using leaky integrators with a focus on integrator output swing and gain nonlinearity

issue. Section 5 presents numerical experiments based on ADC models designed using a behavioral simulator. Section 6 concludes the paper.

2. IDSM Model Using Leaky Integrators

Figure 1 illustrates a block diagram of a second-order IDSM. The DSM is a feedforward topology where a residual quantization error is generated at the output of the last integrator. Therefore, re-quantizing the residual error by an extra quantizer (ADC_{res} in Figure 1) and combining the post-filtered output from the DSM and the output from ADC_{res} with proper weights can future enhance the resolution.

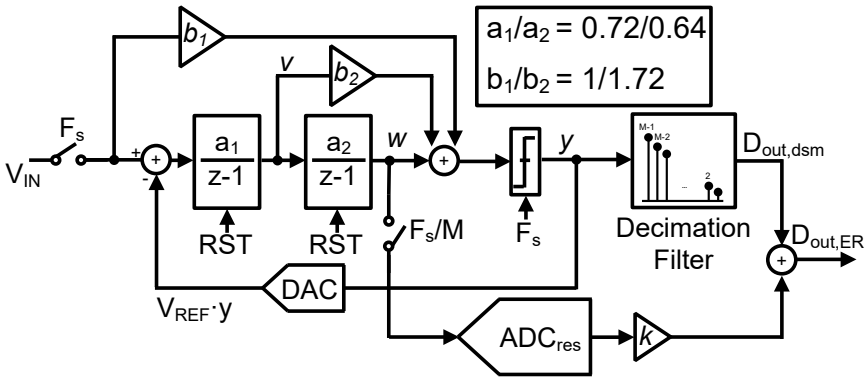

Figure 1. A block diagram of the conventional 2nd-order discrete time (DT) incremental delta-sigma modulator (IDSM) with extended range.

For decimating DSM output, a digital finite-impulse-response (FIR) CoI (cascade-of-integrator) filter is a popular choice, which is proven to be effective in maximizing SNR when the integrators are ideal [13]. However, when there is a leakage in the integrators, such a CoI filter yields suboptimal results. To further investigate the impact of leakage in the integrator, let us first consider an ideal discrete-time integrator whose output is simply a sum of previous input and stored value, i.e.,

$$y[n] = x[n-1] + y[n-1] \tag{1}$$

which leads to the z-domain transfer function

$$H_{I,ideal} = \frac{z^{-1}}{1-z^{-1}} = \frac{1}{z-1} \tag{2}$$

When there is a leakage in the integrators, the previous sample value $y[n-1]$ is not entirely transferred to the current sample value $y[n]$. To accommodate this leakage and possible signal gain in the passive-active hybrid integrator, the expression for the ideal integrator in Equation (1) needs to be modified as:

$$y_{leak}[n] = \alpha \cdot x[n-1] + \beta \cdot y[n-1] \tag{3}$$

where $\beta < 1$ accounts for the leakage of the integrator and α is the forward signal gain. Figure 2a shows a corresponding block diagram of the expression in Equation (3). Figure 2b illustrates one possible and potentially low-power, the implementation for such a leaky integrator, where the charge sharing between C_{in} and C_f realizes the passive integration, and the gain element of G compensates the signal loss. From the charge conservation, one can easily show that the leakage and the forward gain terms in Equation (3) is determined as:

$$\alpha = \frac{G \cdot C_{in}}{C_{in} + C_f}, \ \beta = \frac{G \cdot C_f}{C_{in} + C_f} \tag{4}$$

and $\alpha = 1 - \beta$ holds for the passive integrator. The z-domain transfer function of the leaky integrator is then given by:

$$H_{I,leaky} = \frac{\alpha z^{-1}}{1 - \beta z^{-1}} = \frac{\alpha}{z - \beta} \tag{5}$$

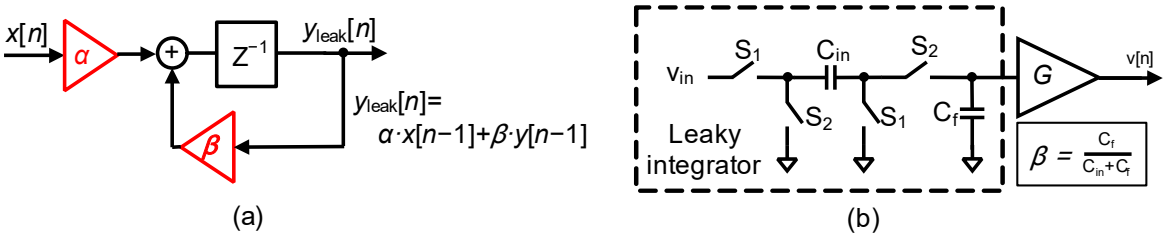

Figure 2. (**a**) A block diagram of the leaky integrator and (**b**) an implementation of the leaky integrator with a gain element.

Figure 3 redraws the IDSM model, where a leaky integrator is used for the 1st stage. We have replaced only the 1st integrator with a leaky integrator because the power dissipation of the 1st stage integrator dominates in a typical IDSM design. To compare the optimal filter expressions for an ideal and a leaky integrator, let us first consider an ideal case where there is no leakage, i.e., $\beta = 1$ and $\alpha = 1$. It can be shown that the residual signal w after M cycles (M being the oversampling ratio) at the output of the second integrator is given as [12]:

$$w[M] = a_1 a_2 \frac{M(M-1)}{2} v_{in} - a_1 a_2 V_{REF}(1 \cdot y[M-1] + 2 \cdot y[M-2] + \cdots + (M-1) \cdot y[1]) \tag{6}$$

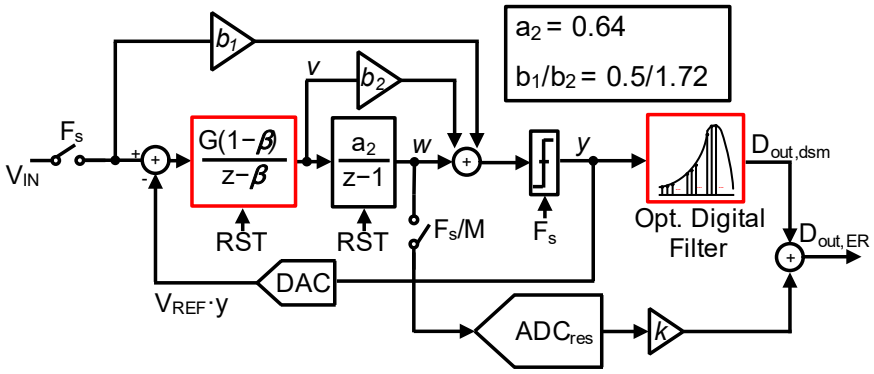

Figure 3. A block diagram of the 2nd-order DT IDSM architecture using a passive integrator and optimal digital decimation filter.

It is apparent from Equation (6) that the residual signal $w[M]$ is a linear combination of v_{in} and bitstream $y[1], \cdots, y[M-1]$. Therefore, v_{in} can be optimally reconstructed by a proper digital-domain decimation filter. The optimal filter coefficients can be found by reformulating Equation (6) as:

$$v_{in} = \frac{2}{a_1 a_2 M(M-1)} (w[M] + a_1 a_2 V_{REF}(1 \cdot y[m-1] + 2 \cdot y[M-2] + \cdots + (M-1) \cdot y[1])), \tag{7}$$

or equivalently:

$$v_{in} = E_Q + \frac{2 \cdot V_{REF}}{M(M-1)}(1 \cdot y[M-1] + 2 \cdot y[M-2] + \cdots + (M-1) \cdot y[1])), \tag{8}$$

where $E_Q = 2 \cdot w[M]/(a_1 a_2 M(M-1))$ is the quantization error. It follows from Equation (8) that the optimal decimation filter is a simple M-1 tap FIR filter with descending tap co-

efficients from $M-1$ to 1. Moreover, since $w[M]$ is linearly scaled quantization error of E_Q, it immediately follows that combining the output of the decimation filter and digitized $w[M]$ with proper scaling factor k will further enhance the resolution of the entire ADC conversion.

Now, let us consider the case with $\beta \neq 1$ that corresponds to the passive and leaky integrator. Due to the incomplete integration, the reconstructed output using the conventional CoI FIR filter is not as effective in reducing quantization noise. A detailed derivation, which is assisted by a symbolic analysis tool, shows that the residual signal $w_{leak}[M]$ when using a passive integrator is expressed as:

$$w_{leak}[M] = a_2(1-\beta)\left(\sum_{k=1}^{M} G^k\beta^{k-1}\right)v_{in} - a_2(1-\beta)\left(\sum_{j=1}^{i}\left(\sum_{k=1}^{M-j+1} G^k\beta^{k-1}\right)y[j]\right). \quad (9)$$

Expressing v_{in} using w_{leak} leads to:

$$\begin{gathered} v_{in} = \frac{1}{a_2(1-\beta)\cdot A}w_{leak}[M] + \frac{1}{A}\left(\sum_{j=1}^{i}\left(\sum_{k=1}^{M-j+1} G^k\beta^{k-1}\right)y[j]\right), \\ A = \left(\sum_{k=1}^{M} G^k\beta^{k-1}\right) \end{gathered} \quad (10)$$

or equivalently,

$$v_{in} = E_{Q,leak} + \frac{1}{A}\left(\sum_{j=1}^{i}\left(\sum_{k=1}^{M-j+1} G^k\beta^{k-1}\right)y[j]\right). \quad (11)$$

It follows from Equation (11) that even when passive integrators are used, we recognize that (1) v_{in} is still a weighted linear combination of $y[1], \cdots, y[M-1]$ and (2) $w_{leak}[M]$ is a linearly scaled quantization error $E_{Q,leak}$. The key difference, though, is that (1) the decimation filters should have different coefficients from the CoI filter and (2) the coefficient k when combining digitized $w_{leak}[M]$ and decimation filter output would be different from the case when $\beta = 1$. Therefore, once we figure out how to find these filter design parameters, effective quantization noise reduction can still be achieved for IDSMs using passive and leaky integrators.

3. Optimal Digital Decimation Filter Design

The amount of leakage β of the integrator depends on actual circuit implementations, and it is often not easy to know β precisely in real designs. Therefore, this article presents a foreground calibration method that enables accurate estimation of the optimal filter coefficients.

The calibration setup, along with the ADC structure consisting of an ADC core and a calibration filter logic, is illustrated in Figure 4. The calibration logic is a linear M-tap FIR filter having filter coefficients $h[m]$, $m = 0, \cdots, M-1$ in addition to the summer with a path gain of k for the $\mathrm{ADC_{res}}$. Since the weights of the FIR filter are fixed during the operation, they can be implemented as a combination of an adder, a register, and two multiplexers, as illustrated in Figure 4. To find filter parameters, let us assume that we apply a sinewave having a signal frequency of f_{sig} to the ADC with a sampling period T_S and conversion length of L. Obtained digital output is then expressed as $y_i[m]$, $m = 0, \cdots, M-1$ and $i = 1, \cdots, L$ from the IDSM and $D_{out,res,i}$, $i = 1, \cdots, L$ from the $\mathrm{ADC_{res}}$ for the extended range. Finding optimal digital filter coefficients can be formulated as a following convex optimization problem:

$$\begin{gathered} minimize \sum_{i=1}^{L} err[i]^2 \\ \text{subject to} \\ err[i] = \sum_{m=0}^{M-1} y_i[m]\cdot h[m] + k\cdot D_{out,res,i} - \widetilde{v}_{in,est}[i] \\ \widetilde{v}_{in,est}[i] = Asin\left(2\pi f_{sig}t_i\right) + B\cos\left(2\pi f_{sig}t_i\right) + C,\ t_i = T_s, 2T_s, \cdots, L\cdot T_S \end{gathered} \quad (12)$$

where the optimization variables are:

(1) the filter parameters $h[m]$ and k;
(2) the A, B, and C for estimating the best-fit sinewave.

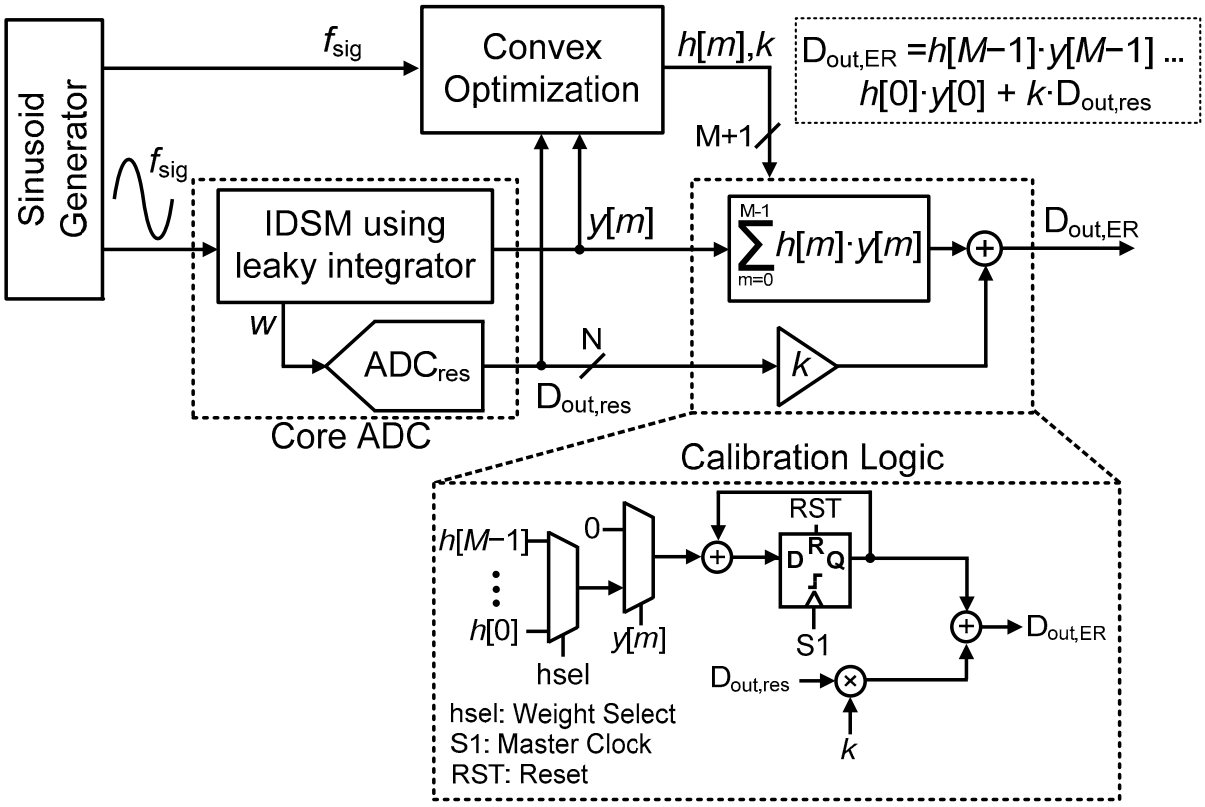

Figure 4. The setup for finding the optimal digital filter parameters.

In essence, an objective of the problem formulation in Equation (12) is to find the best filter tap weights $h[m]$ as well as the path gain k for the residue output such a way that error between the reconstructed best estimate and the actual input of length L is minimized in the least-squares sense. To numerically solve the Equation (12), this work uses CVX, a package for specifying and solving convex problems [14], where the problem is solved via an embedded interior-point method solver. In addition, to test our algorithm, we created a model of the second order IDSM in Figure 3 using CppSim [15], a time–domain behavioral simulation package. For experiments, we use $G = 2$, $b_1 = 0.5$, $b_2 = 1.72$ with an oversampling ratio of 256. Figure 5 illustrates the obtained filter coefficients for various leakage parameter β values. Interestingly, when $\beta = 0.999$, which is the case when the leakage is very small, the optimal filter coefficient is symmetrically shaped around the center tap weight. This contrasts with the CoI filter in an active-RC-based integrator. Such a difference stems from the fact that α and β are interdependent for the passive integrator. Specifically, $\alpha = \beta = 1$ h olds for an ideal active-RC integrator in Equation (4), but when β gets close to 1, α approaches 0 in the case of the passive integrator, leading to different optimal filter shape. In theory, the filter coefficients, or the impulse response, can analytically be chosen depending on β and path gain G as derived in Equation (11), but Figure 5 shows one interesting trend that the peak value of tap weights moves from the center to the end of the impulse response as β gets lower.

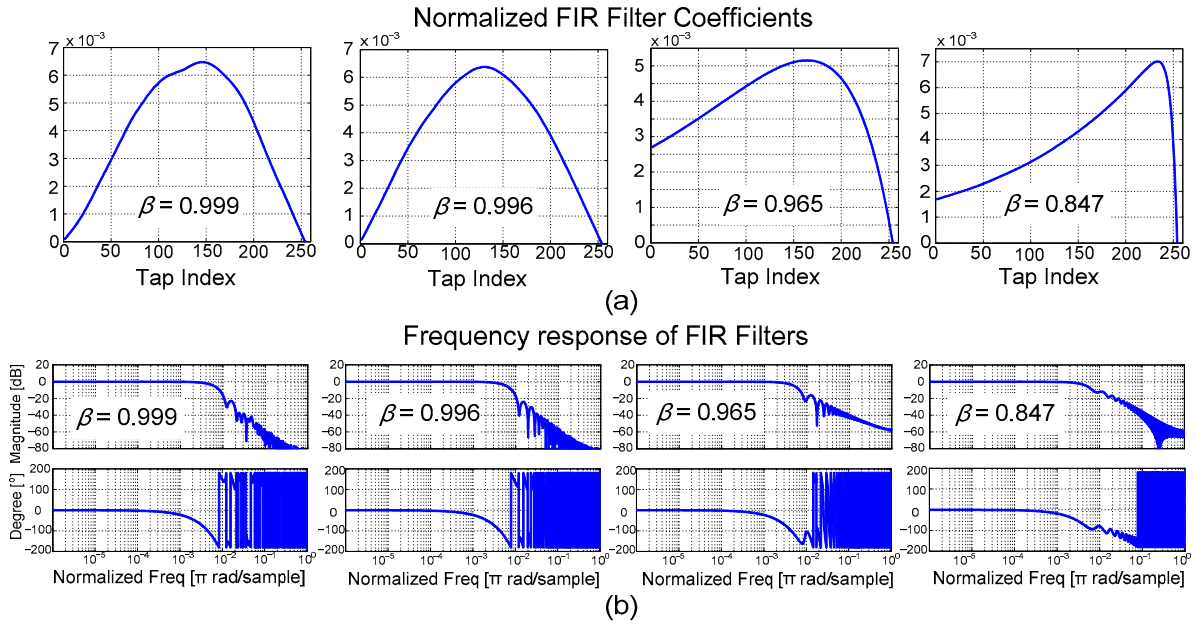

Figure 5. (**a**) Normalized optimal filter coefficient for various leakage values and (**b**) corresponding magnitude and phase response of the filter in frequency-domain.

To verify the actual performance enhancement of applying the optimal digital filter, Figure 6 shows simulated SNDRs of the ADC in Figure 3 with a conventional CoI filter and the optimal FIR filter obtained from the proposed algorithm. The simulated SNDR ranges from 50 dB and 78 dB depending on the leakage parameter β when the conventional CoI filter is used. In contrast, with the optimal filter presented in this work, the SNDR is beyond 90 dB for all β values ranging from 0.85 to 0.999, demonstrating the effectiveness of the proposed algorithm.

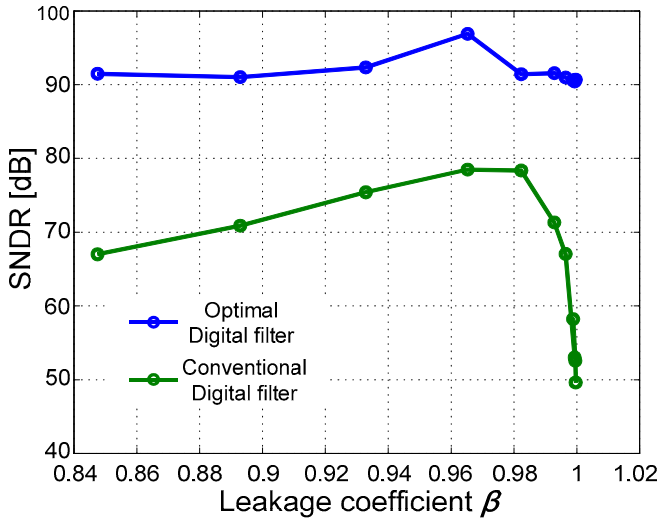

Figure 6. Comparison of signal-to-noise and distortion ratio (SNDR) versus leakage values with and without the optimal digital filter.

Table 2 highlights new contributions of this work in comparison to previously published digital filtering techniques for incremental ADCs. While they are all digitally synthesizable and can be integrated on-chip with a core ADC, there are two different categories of filtering approaches, i.e., linear and nonlinear filtering. In general, linear filtering does not have the stability issue and can naturally benefit from the thermal noise

averaging of the oversampled converters. On the other hand, in noise-free situations, a nonlinear and iterative filter can outperform the linear filter in terms of quantization error reduction. However, it is not immediately obvious that the nonlinear filter performs practically better due to the risk of instability from the iterative decoding, which may lead to thermal noise enhancement. For instance, in [16,17], the nonlinear iterative decoding filtering scheme was presented, but the performance under the influence of thermal noise was not verified. Reference [18] is an optimal linear filter approach, which is similar to this work but requires a customized algorithm to find filter coefficients. The optimal filtering technique in [19] is the most recent work, which combines the benefit of noise averaging of linear filtering and the nonlinear decoding at the cost of higher power dissipation and larger area than most linear filters such as Sinc and CoI filters. In contrast, the algorithm for finding optimal filter parameters is based on convex optimization, which already has a stable technology. Being able to easily design an optimal filter via existing solver technology such as CVX [14] is a clear advantage when compared to other methods. In addition, note that none of the previous works have shown whether it is possible to combine the extended range technique, which is to use an extra quantizer for the DSM, and the optimal filtering technique for the lossy integrator. Our additional contribution is that we showed that it is indeed possible to combine these two techniques to further enhance the SNDR.

Table 2. Comparison of various digital filter techniques for incremental delta-sigma modulator (IDSM).

	This Work	**[16]**	**[17]**	**[18]**	**[19]**
Decimation filter structure	Linear	Nonlinear	Nonlinear	Linear	Nonlinear
Test vehicle ADC for algorithm verification	2nd-order IDSM with extended range	2nd-order IDSM	MASH11 IDSM	3rd-order IDSM	2nd-order IDSM
Verified for lossy and passive integrator in DSM?	Yes	No	No	No	No
Verified for extended range?	Yes	No	No	No	No
Comments	Filter parameters are found via convex optimization. (global optimal guaranteed)	Iterative decoding may incur random noise enhancement (not verified in the paper)	High complexity due to double iteration.	Requires a custom algorithm to find filter coefficients.	Achieved only < 100 Sa/s due to high filter design complexity

4. Circuit-Level Design Considerations

There are several design tradeoffs and considerations when one wants to apply the passive integrator in Figure 2 to actual IDSM designs. The gain element G can easily be realized by any low-power open-loop amplifiers since G tends to be small (< 10) in practice, but the amplifier output may saturate. Therefore, the swing and the nonlinearity of the entire passive integrator are the paramount concern.

The passive integrator, by nature, faces a tradeoff in choosing the ratio between the memory capacitor C_f and the sampling capacitor C_{in}. From the ADC and the amplifier design perspective, large β and therefore large C_f/C_{in} ratio are beneficial because the signal swing at the input of the amplifier is attenuated by this ratio, hence meeting the output swing and the linearity requirement in the following amplifier becomes easier. However, the required C_f can be unacceptably large because the C_{in} value must be chosen considering the kT/C noise limit of the entire conversion. To give a perspective, let us assume that the full input scale is $1V_{pp,diff,}$ and we target SNR of 90 dB with OSR = 256. A quick calculation reveals that C_{in} = 1 pF and C_f = 9 pF are required if we target β = 0.9. Therefore, the area penalty of realizing C_f quickly jeopardizes the benefit of using a low-power passive integrator. On the other hand, if β is too small, the amplifier followed by the passive integrator should handle large signal amplitude, making the nonlinearity of the amplifier more pronounced. Since the gain element in the passive integrator plays a critical role

in attenuating the noise of the following integrator stages, one must consider the overall SNR budget of the ADC when choosing the gain value in the passive integrator. We found from exhaustive behavioral simulations that $\beta = 0.847$ and $G = 2$ [V/V] achieves a good compromise between the noise gain and the output signal amplitude.

Figure 7 shows the simulated histograms of the output amplitude in the integrator for both the first and the second stage by using the $G = 2$ and $\beta = 0.847$. The histograms indicate that the output swings are maintained within ± 0.35 V and ± 0.3 V for the first and the second integrator, respectively, when a ± 1 V full-scale input sinusoid is applied. Note that this level of signal swing can be easily accommodated in transistor-level amplifier designs.

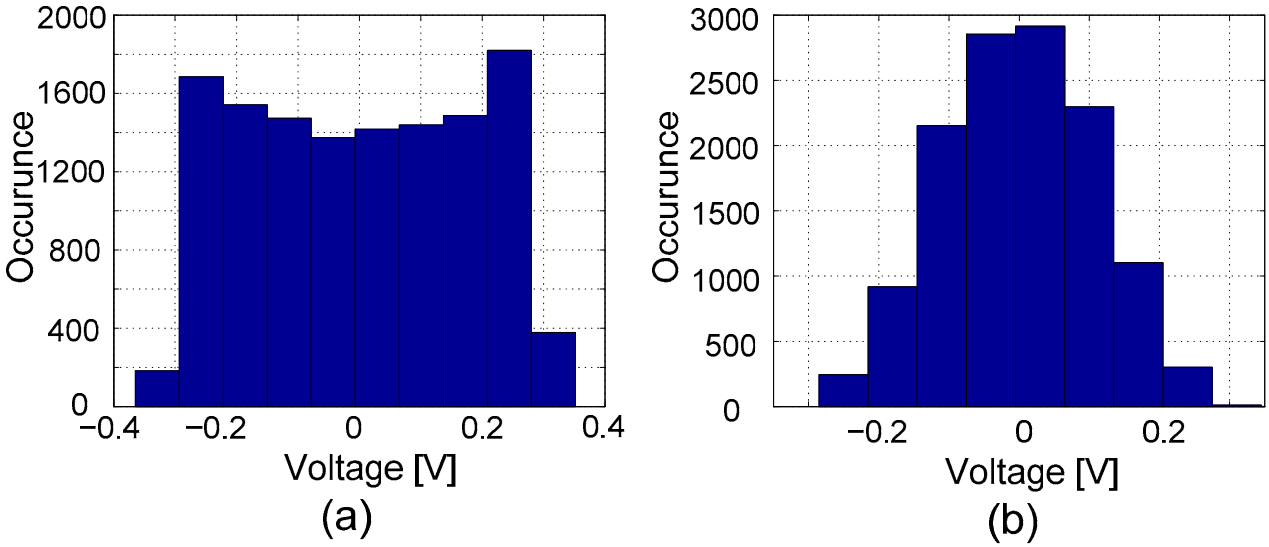

Figure 7. The simulated output range of (**a**) the 1st stage integrator and (**b**) the 2nd stage integrator.

We also evaluated the impact of the amplifier nonlinearity using behavioral simulations. Specifically, since most differential amplifiers suffer from compressive gain nonlinearity versus input magnitude, we use the following gain model

$$V_{out} = G \cdot V_{in} - \gamma \cdot V_{in}^2 \tag{13}$$

in the amplifier block within our ADC model used in the behavioral simulations. Note that V_{in} is the input magnitude and γ is a parameter that represents the degree of compressive nonlinearity, i.e., larger γ would lead to higher compressive nonlinearity. Figure 8a shows the gain versus V_{in} for several γ values and corresponding worst-case gain error. By using this amplifier model, we evaluated the SNDR of the entire ADC over various values γ. Figure 8b shows the simulated SNDR versus the worst-case gain error arising from the amplifier nonlinearity. The simulations indicate that the gain error must be smaller than 2% to achieve 90 dB, and up to 5% gain error is allowable if we allow 5 dB degradation. While the gain error smaller than 2% is certainly attainable in CMOS amplifier designs, one still must be cautious about the risk of SNDR degradation from poor amplifier linearity performance when attempting to use passive integrators in the DSM designs.

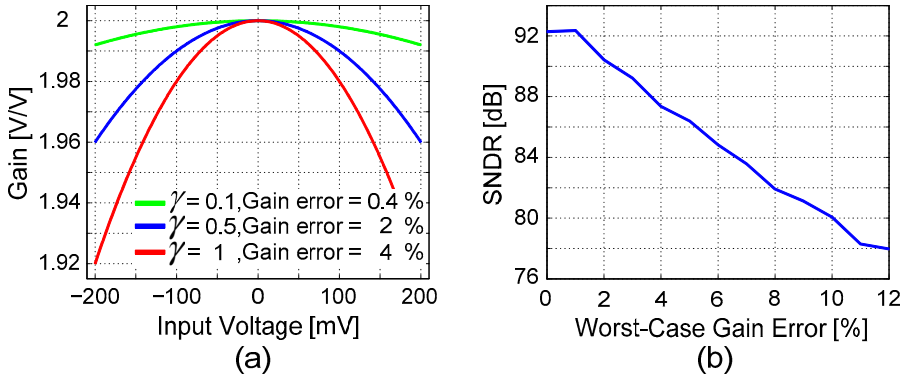

Figure 8. (**a**) Compressive gain nonlinearity and the worst-case gain error of the amplifier. (**b**) Simulated SNDR vs. gain error from the nonlinearity.

5. Numerical Experiments

For realistic and extensive numerical experiments, we designed a full switched-capacitor second-order IDSM, as shown in Figure 9 using CppSim. The parameter values used in our ADC model are summarized in Table 3. For realistic simulations, the model includes kT/C noise of the switched-capacitor circuits as well as the amplifier input-referred thermal noise. The noise density and the nonlinearity parameter value γ in Table 3 are derived from a transistor-level design in 65 nm CMOS process. The behavioral model also includes random mismatches for the sampling capacitor C_{in1} and the integration capacitor C_{f1} as well as a random gain variation for the first stage amplifier. The mismatch and variation parameters are necessary for the Monte-Carlo simulations, which are used to verify the robustness of the proposed optimal filtering technique to possible process spread and device mismatches in actual chip fabrication.

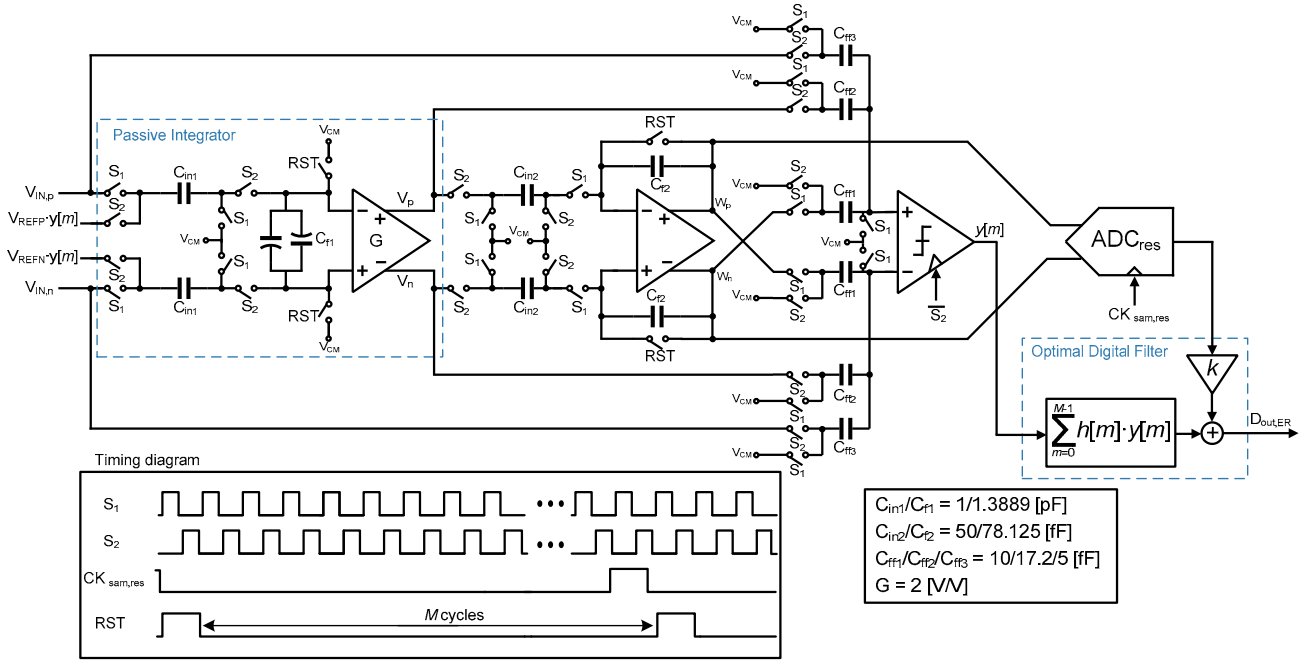

Figure 9. Overall IDSM architecture using a leaky integrator for the 1st stage and optimal digital filter.

Table 3. ADC parameters for behavioral simulations.

Parameter	Value
ADC sampling frequency (F_s)	12 (MHz)
Oversampling ratio (OSR)	64, 128, 256
Calibration signal frequency	$0.34F_s$
Input thermal noise of 1st amp	11 (nV/$\sqrt{\text{Hz}}$)
Input thermal noise of 2nd amp	15 (nV/$\sqrt{\text{Hz}}$)
G, γ	2 (V/V), 0.5
b_1, b_2	0.5, 1.72
σ of capacitor mismatch for C = 1 pF	0.03%
σ of gain variation	1%
Resolution of ADC_{res}	8-bit

Figures 10 and 11 show a few snapshots of nominal simulations with OSR = 256 and OSR = 64, respectively, with no mismatch or variation parameters. In this experiment, we applied $f_{sig} = 0.028F_s$ when OSR = 256 and $f_{sig} = 0.084F_s$ when OSR = 64, respectively, as representative inputs. Figure 10a shows the frequency domain spectrum of ADC outputs for OSR = 256 when using the conventional CoI filter (shown in blue) and the proposed optimal filter (shown in red). Figure 10b graphs the optimal FIR filter coefficients that are used to produce the frequency-domain spectrum. Similarly, Figure 11 shows the frequency-domain spectrum and the filter coefficients when OSR = 64. In both cases, applying the optimal filter enhances SNDR by 15 dB–20 dB, verifying the effectiveness of the optimal digital filtering technique regardless of oversampling ratios. Comparing Figures 10b and 11b leads us to an interesting observation that the optimal FIR filter shape is quite different for both cases even though they use the same passive integrator model. This difference stems from the fact that the optimal filter expression shown in Equation (11) is indeed a function of the oversampling ratio M, which reassures that the filter coefficients must be individually found for different oversampling ratio.

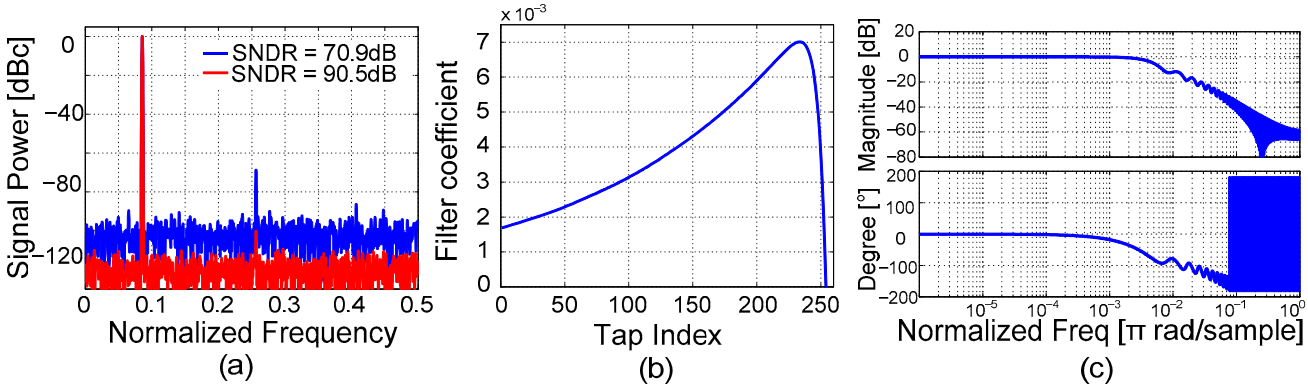

Figure 10. (**a**) Simulated output spectrum with the optimal filter (red) and the cascade-of-integrator (CoI) filter (blue) when oversampling ratio (OSR) = 256; (**b**) normalized coefficients of the filter, and (**c**) the magnitude and phase response of the filter.

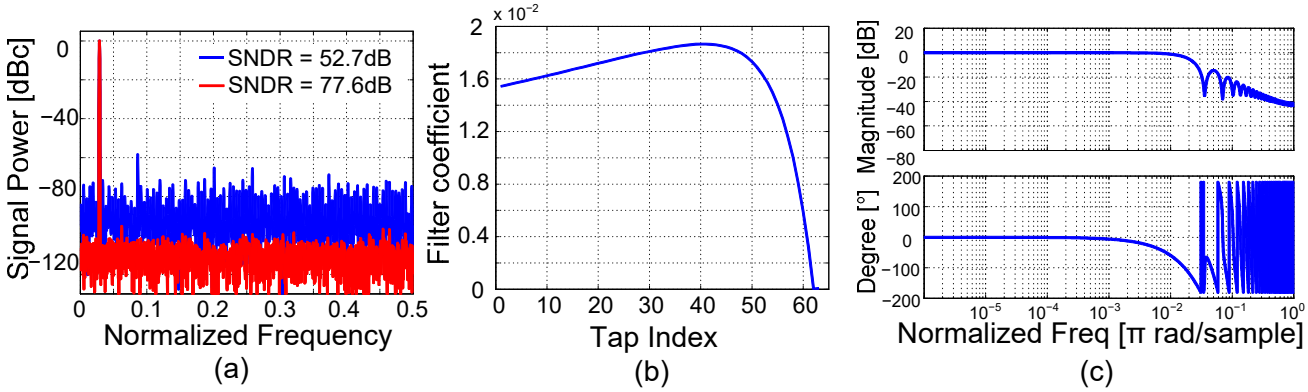

Figure 11. (**a**) Simulated output spectrum with the optimal filter (red) and the CoI filter (blue) when OSR = 65, (**b**) normalized coefficients of the filter, and (**c**) the magnitude and phase response of the filter.

It is also worth pointing out that when OSR is fixed, the optimal filter coefficients are invariant to the signal frequency used for the calibration. To experimentally prove our claim, Figure 12 shows a simulated output spectrum for three different signal frequencies (f_{sig} = 0.08F_S, 0.23F_S, and 0.34F_S) while using the same filter coefficients found from f_{sig} = 0.084F_s. The result shows that SNDR is universally enhanced above 90 dB, showing that the invariance of the optimal filter coefficient to the signal frequency.

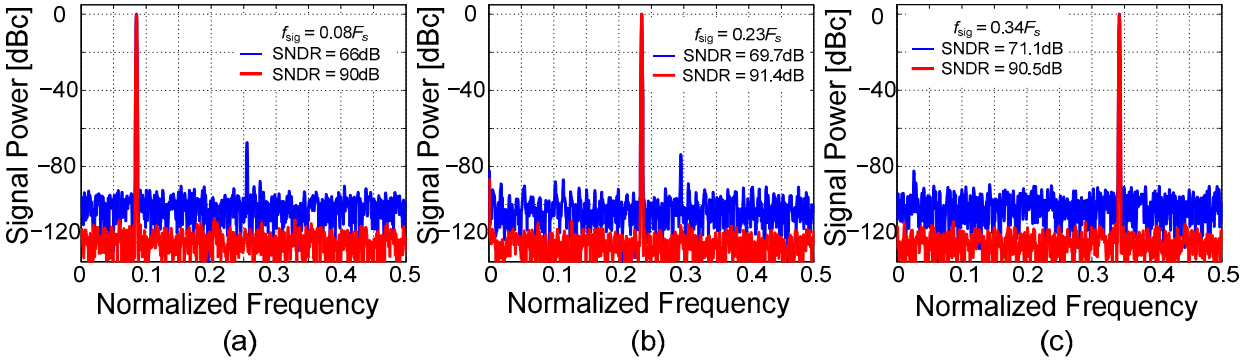

Figure 12. Simulated output spectrum when input signal frequencies are (**a**) f_{sig} = 0.08F_S; (**b**) f_{sig} = 0.23F_S, and (**c**) f_{sig} = 0.34F_S.

For extensive verification, we have performed 100 Monte-Carlo simulations for OSR = 256 with the capacitor mismatch and gain variation parameters in Table 3. The histogram in Figure 13 displays the distributions of SNDRs with the optimal filtering (shown in blue) and the CoI filtering (shown in red). The mean value of SNDR improves from 67 dB to 90 dB, demonstrating that the presented algorithm can enhance the SNDR of IDSM using a low-power passive integrator beyond 90 dB even under the presence of various component mismatches and amplifier gain uncertainty.

In addition, we have designed a full transistor-level proof-of-concept design of the proposed ADC in the 65 nm CMOS process, where the residual ADC in Figure 9 is implemented as synchronous 8-bit SAR ADC. Figure 14a shows the simulated output spectrum of the ADC after the optimal filtering. The result clearly proves that almost 20 dB of SNDR enhancement is attainable after the calibration in a full circuit simulation. In addition, the obtained weights of the decimation filter in Figure 14b are similar to those already shown in Figure 10b, indicating that the behavioral simulation matches well with transistor-level simulation. For the interest of readers, we also report that the power and area of this residual ADC is only 3% and 15% of the total power and area, respectively. Therefore, having this residual ADC does not incur substantial power and area costs.

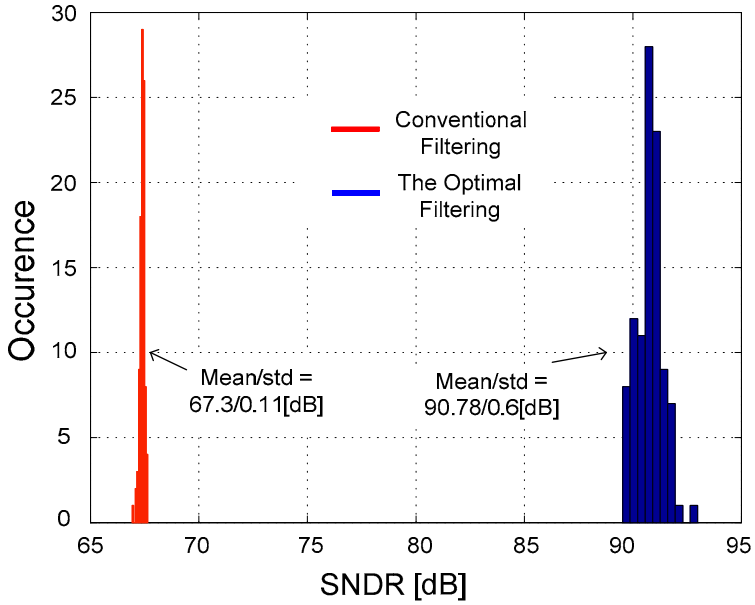

Figure 13. Histogram of the signal-to-noise and distortion ratio (SNDR) from 100 Monte-Carlo simulations.

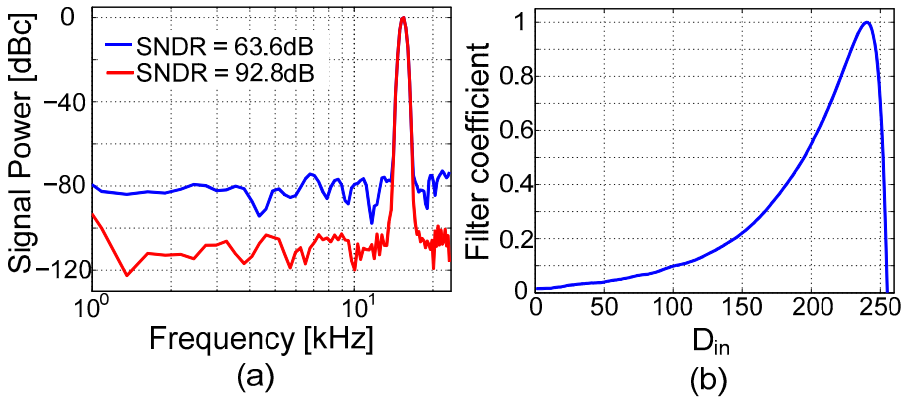

Figure 14. (**a**) Simulated output spectrum from transistor-level circuit simulation in 65 nm complementary metal-oxide-semiconductor (CMOS) model with the optimal filter (red) and the CoI filter (blue) when OSR = 256, and (**b**) the normalized coefficients of the optimal filter.

6. Conclusions

This paper presented an optimal digital filtering technique that enhances the SNDR of incremental DSMs based on leaky integrators. The main focus of this work is to come up with an algorithm that finds optimal digital filter parameters. The algorithm, based on convex optimization, provides a straightforward and predictable way of designing an optimal digital filter for IDSMs using a passive integrator and a low-gain amplifier. Based on a behavioral ADC model that captures fine details of transistor-level circuits such as gain nonlinearity and thermal noise, comprehensive behavioral simulations confirm that the proposed algorithm is quite effective in enhancing SNDR of the entire A/D conversion beyond 90 dB despite using a passive integrator. The technique presented in this work is highly digital in nature, and therefore can be a favorable approach when one wants to design high-resolution ultra-low-power sensor ADCs in highly scaled CMOS technology where designing high-gain op-amps are costly in terms of power and area.

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