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Hybrid Modulated DCDC Boost Converter for Wearable Devices

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Abstract: Wearable devices require power management systems to achieve high conversion efficiency over a wide range of load currents. Multi-mode mixed modulation can be used in DCDC converters to achieve high efficiency over a wide load current range. The DCDC boost converter proposed in this paper uses a hybrid modulation of DGM (Deep Green Control Mode), PCMC (Peak current mode control)-PFM (Pulse Frequency Modulation) and PCMC-PWM (Pulse Width Modulation). The converter switches smoothly from PCMC-PFM to PCMC-PWM mode under load-current-based conditions and without any mode selection module. The proposed DCDC boost converter is fabricated in a 0.18 μm CMOS process with a Die area of 1.24 × 0.78 μm^2. The input voltage range is 0.8–5 V, the output voltage is 5 V, and the load current range is 5–300 mA. Experimental results show that the boost converter can achieve 94.7% peak efficiency. Efficiency of more than 90% can be achieved in the load current range of 30–300 mA.

Keywords: boost converter; hybrid modulated; wearable devices; DGM; PCMC-PFM; PCMC-PWM; efficiency

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1. Introduction

The expected growth of wearable IoT devices in 2026 is shown in [1] to be approximately USD 110.8 billion and the industry is growing at a CAGR(Compound Annual Growth Rate) of 13.6%. Figure 1 [2] shows that there are three main categories of existing wearable products: accessories, e-textiles, and e-patches. Wearable devices have gained much attention for their unique connectivity characteristics [3], excellent data accuracy, and data efficiency [4]. Wearable devices also face many challenges, among which battery power supply efficiency and energy consumption are a concern [2,3].

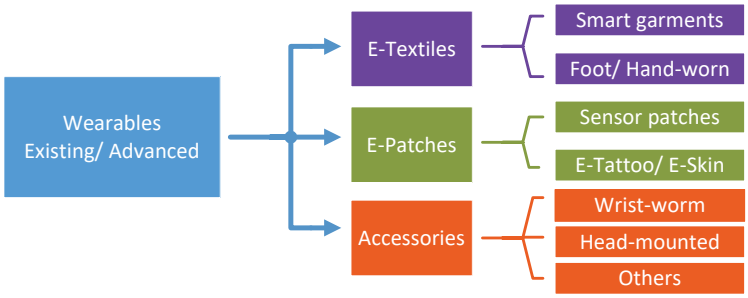

Figure 1. Main categories of existing wearable products.

Numerous types of batteries are used in wearable electronic devices, ranging from the early primary batteries represented by lithium batteries [5], and to the most widely

used secondary batteries today. The most recent cutting-edge research is the use of energy harvesting for autonomous power supply [2,6]. For example, the collection and use of mechanical, thermal, and solar energy proposed in [7,8] provides new research directions. A well-performing power management unit (PMU) will be the key module to improve the battery efficiency of wearable electronic devices for any energy supply method. Wearable electronic devices require PMU modules with high efficiency, wide input voltage range, and load current range to adapt to different operating scenarios [9], which is the same as typical IoT devices. For example, the current consumption in sensing mode is a few uA to tens of uA [10,11], the microprocessor is tens of mA [12,13], and the wireless link can be up to hundreds of mA [14,15]. The quiescent current of the device in sleep mode should also be reduced as much as possible to improve the overall efficiency [9,16,17].

Today there are two main categories of switching power supplies: capacitor-based [18,19] and inductor-based. Capacitor-based switching power supplies can only provide output voltages with discrete voltage ratios to the system [20], making them unsuitable for wearable electronics. On the contrary, inductor-based switching power supplies, especially DCDC boost converters, have consistent output voltage. It is necessary for battery-powered systems, or as a conversion interface for energy harvesting systems [21], to provide stable and reliable voltages to devices. Therefore, inductor-based switching power supplies are gradually becoming the preferred choice for wearable devices. The main control methods of DCDC boost converter are PWM mode, PFM mode, and PWM-PFM hybrid mode. PWM mode boost converter output voltage ripple is small and has a fast conversion speed, PFM mode has higher efficiency compared to PWM mode at light load, PWM-PFM mode combines the advantages of both but the circuit structure is complex and it is difficult to achieve smooth switching between the two modes. For devices in sleep mode for a long time, quiescent current loss severely affects the system efficiency [22,23]. To address this problem [9], a Deep Green Control Mode (DGM) with very low quiescent current is proposed which can significantly improve the system efficiency in ultra-light load or sleep mode. However, this method has only been successfully applied in buck converters and smooth switching between PWM-PFM modes is not taken into account.

The DCDC boost converter proposed in this paper uses a hybrid modulation technique of DGM-PFM-PWM automatic switching. The DGM mode will be used under ultra-light load conditions, which will reduce switching losses and quiescent current. The peak current-PFM control mode (PCMC-PFM) is used under light load conditions, during which the internal clock can generate a clock oscillation signal that is positively correlated with the load current, reducing switching losses while ensuring a high response rate and a small output voltage ripple. The peak current-PWM control mode (PCMC-PWM) with constant clock frequency is used to achieve high output efficiency under heavy load conditions. The internal VCO unit of the boost converter not only provides a reliable clock oscillation frequency for the boost converter, but also enables a smooth transition from PFM to PWM mode depending on the load current without adding an additional mode switching control unit.

The rest of this paper is organized as follows: in Section 2, the system-level architecture of the proposed DGM-PFM-PWM hybrid modulated DCDC boost converter is introduced, with emphasis on the DGM mode, the PFM operation mode, and the smooth transition from the PFM mode to the PWM mode. Section 3 presents the circuit implementation of the key modules and the simulation results they can achieve. The experimental results of the proposed DCDC boost converter will be given in Section 4. The conclusions will be discussed in Section 5.

2. Proposed DGM-PFM-PWM Hybrid Modulated DCDC Boost Converter

In order to achieve high efficiency over a wide load range this paper proposes a DGM-PFM-PWM hybrid modulated DCDC boost converter. The proposed system-level architecture of the boost converter and the DGM control method at ultra-light load will be introduced in Section 2.1. The PCMC-PFM control mode at light load is introduced in

Section 2.2. A novel technique for smooth switching from PCMC-PFM mode to PCMC-PWM is introduced in Section 2.3.

2.1. System Structure and DGM Operation Mode

The system-level architecture of the proposed boost converter is shown in Figure 2. The system mainly consists of power stages (N-MOS, P-MOS, and Gate Driver), reference voltage generation circuits (Bandgap), feedback circuits (R_{f1}, R_{f2}, and peak current detector), and control circuits, including DGM comparator (DGM-CMP), error comparator (EA) with high level clamp (H-clamp) and low level clamp (L-clamp), PWM comparator, PFM amplifier, VCO, pulse generation unit, slope compensation, digital logic control unit (Logic), and other modules. The system is controlled by a mixture of DGM, PCMC-PFM, and PCMC-PWM modes. In addition, the system also uses a dual-loop control combining voltage outer-loop and peak current inner-loop to enhance the response speed of the converter.

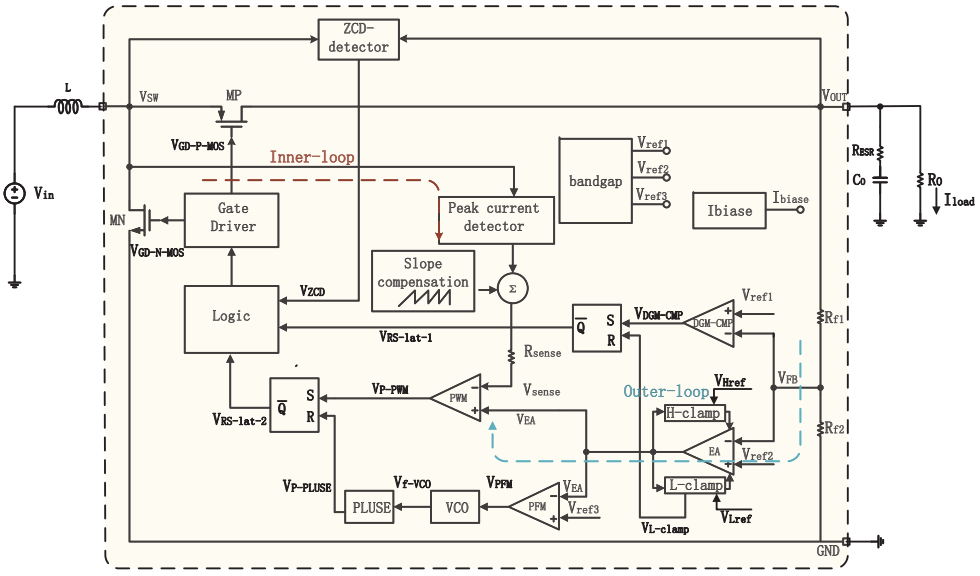

Figure 2. The system-level architecture of the proposed boost converter.

The magnitude of the load current directly determines the operating mode of the boost converter. The parasitic resistance R_{ESR} carried by this capacitor has a definite value when the off-chip C_O is fixed. The voltage V_{OUT} obtained from the load is fed into the error comparator via feedback and compared with the reference voltageV_{ref2} to obtain the V_{EA} as shown in (1).

$$V_{EA} = A_{EA}\left[V_{ref2} - \frac{R_{f2}}{R_{f1}+R_{f2}}(V_{CO} - R_{ESR}I_{load})\right] \tag{1}$$

In Equation (1), V_{EA} is the amplification of the error amplifier, R_{f1} and R_{f2} are the feedback resistors, V_{CO} is the voltage obtained on the output capacitor C_O, and I_{load} is the load current. The derivation of (1) yields (2).

$$\frac{\partial V_{EA}}{\partial I_{load}} = A_{EA}\frac{R_{f2}\times R_{ESR}}{R_{f1}+R_{f2}} > 0 \tag{2}$$

Equation (2) shows that V_{EA} is positively correlated with I_{load}, which means that V_{EA} increases (decreases) with the increase (decrease) in I_{load}. The effect of the clamp circuit makes $V_{EA} \in \left[V_{Lref}, V_{Href}\right]$, where V_{Lref} and V_{Href} are the reference voltages input to the

clamp circuit. The operating mode of the system will be closely related to the relationship between V_{EA} and I_{load}.

The system operates in DGM control mode when the boost converter has an ultra-low load current. From (3), it is clear that V_{FB} has relatively high value in this mode. The L-clamp contains a Schmitt trigger structure. In DGM mode, V_{FB} is compared with V_{ref1} by EA to obtain a lower output V_{EA}, and the Schmitt trigger will be triggered when $V_{EA} = V_{Lref}$ and the output $V_{L-clamp}$ is high.

$$V_{FB} = \frac{R_{f1}}{R_{f1} + R_{f2}} \times (V_{CO} - I_{load} R_{ESR}) \tag{3}$$

At the same time the output voltage of DGM-CMP VDGM-CMP is low. $V_{L-clamp}$ and VDGM-CMP obtain $V_{RS-lat-1}$ with a high level under the action of RS trigger (RS-latch-1), which will control PWM comparator and PFM comparator to stop operation and make the converter enter the ideal phase in DGM mode to improve system efficiency. The logical relationship between $V_{L-clamp}$, $V_{DGM-CMP}$, and $V_{RS-lat-1}$ is shown in Figure 3a. $V_{RS-lat-1}$ is also fed to the digital logic control unit to obtain the control signal which is used to turn off the N-MOS and P-MOS to reduce the switching losses of the system, and the V_{OUT} will be in a continuous state of reduction during this phase. $V_{RS-lat-1}$ is low when $V_{FB} < V_{ref2}$, while PWM, PFM, N-MOS, and P-MOS resume normal operation, and the output voltage V_{OUT} continues to rise until $V_{FB} > V_{ref2}$. After that, the system will start a new cycle of DGM control mode. During the DGM and PCMC-PFM control the P-MOS will have a long on time which results in $V_{SW} \leq V_{OUT}$. This will result in a backflow of current from V_{OUT} to V_{IN}, causing a large power loss.

A ZCD detector circuit is added to further improve the efficiency during the DGM and PCMC-PFM control modes. When $V_{SW} \leq V_{OUT}$, the ZCD detector circuit generates V_{ZCD} with high level, which is used to turn off the P-MOS by the Logic. The correspondence between V_{OUT}, $V_{RS-lat-1}$,V_{ZCD}, the driving signal $V_{GD-N-MOS}$ of MN and the driving signal $V_{GD-P-MOS}$ of MP is shown in Figure 3b.

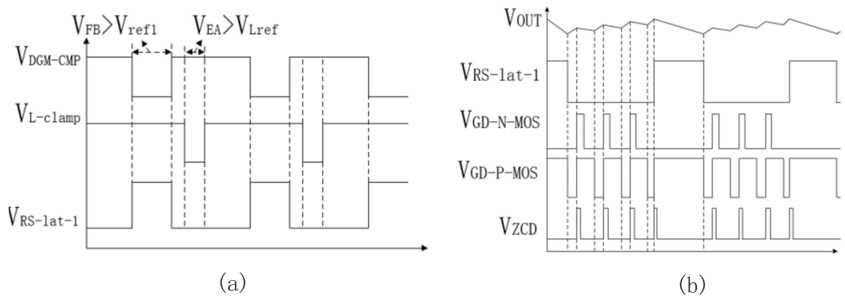

Figure 3. Main control signal timing logic. (**a**) The logical relationship between $V_{L-clamp}$, $V_{DGM-CMP}$ and $V_{RS-lat-1}$. (**b**) The correspondence between V_{OUT},$V_{RS-lat-1}$, V_{ZCD}, $V_{GD-N-MOS}$, and $V_{GD-P-MOS}$.

2.2. PCMC-PFM control mode

When the boost converter enters PCMC-PFM or PCMC-PWM control mode, the PWM comparator and PFM amplifier will be in continuous operation. From (2), it can be seen that V_{EA} is positively related to I_{load}. PCMC-PFM operation mode will directly use this relationship to regulate the operating frequency of the system. The input reference voltage V_{ref3} of the PFM amplifier is deterministic and $V_{L-clamp} < V_{ref3} < V_{H-clamp}$. When $V_{L-clamp} < V_{EA} < V_{ref3}$, the output V_{PFM} of the PFM amplifier will decrease with the increase in load current. V_{PFM} is fed to the voltage-controlled oscillation unit VCO, which will generate an oscillation signal V_{f-VCO} with an oscillation frequency negatively related to V_{PFM}, and it can be seen that the oscillation frequency of V_{f-VCO} increases with the increase in I_{load} in the PCMC-PFM control mode. The narrow pulse signal V_{PLUSE} with

the same frequency as V_{f-VCO} is obtained after feeding V_{f-VCO} into the PLUSE. The correspondence between I_{load}, V_{EA}, V_{PFM}, V_{f-VCO}, and V_{PLUSE} in PCMC-PFM mode is shown in Figure 4a. The compensated peak current information I_{sense} is converted into the feedback signal V_{sense} of the current inner loop. V_{sense} and V_{EA} are compared by PWM module to generate pulse signal V_{P-PWM}. The $V_{RS-lat-2}$ is fed to the Logic to obtain control signals to control the drive circuit to generate the corresponding drive signals $V_{GD-N-MOS}$ and $V_{GD-P-MOS}$. Figure 4b shows the logical relationships between V_{P-PWM}, V_{PLUSE}, $V_{RS-lat-2}$, $V_{GD-N-MOS}$, and $V_{GD-P-MOS}$.

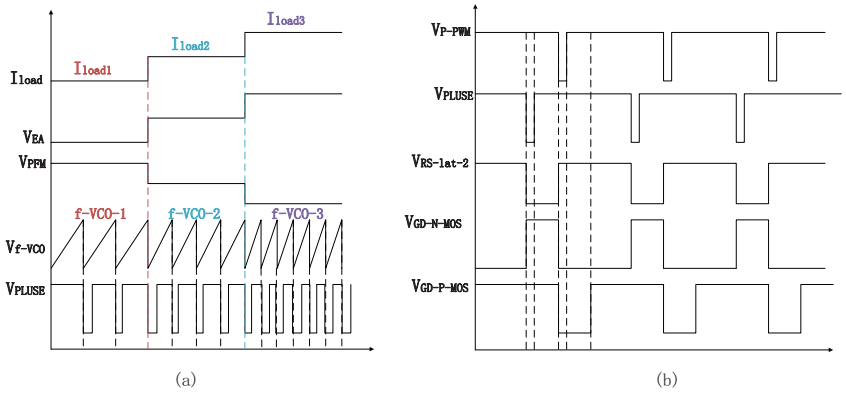

Figure 4. Main signal timing relationship in PFM mode. (**a**) Correspondence between Iload, V_{EA}, V_{PFM}, V_{f-VCO}, and V_{PLUSE} in PCMC-PFM mode. (**b**) The logical relationships between V_{P-PWM}, V_{PLUSE}, $V_{RS-lat-2}$, $V_{GD-N-MOS}$, and $V_{GD-P-MOS}$.

2.3. Smooth switching from PCMC-PFM mode to PCMC-PWM mode

When $V_{L-clamp} < V_{EA} < V_{ref3}$, the system operates in PCMC-PFM mode and the oscillation frequency of the system increases with the increase in I_{load}. The output of the PFM amplifier$V_{PFM} < V_{N-th}$, where V_{N-th} is the threshold voltage of the control MOS equipment in the VCO module. At this time, the oscillation signal V_{f-VCO} oscillation frequency generated by VCO reaches saturation and no longer follows V_{EA} and I_{load} changes, the system automatically smoothly enters the PCMC-PWM control mode with constant frequency. Figure 5 shows the correspondence curves between V_{EA}, V_{PFM}, and V_{PLUSE} when the system is smoothly switched from PCMC-PFM mode to PCMC-PWM mode. It can be seen that the system is completely self-regulated by Iload during this phase of mode switching without adding any mode switching module which greatly reduces the complexity of the system design.

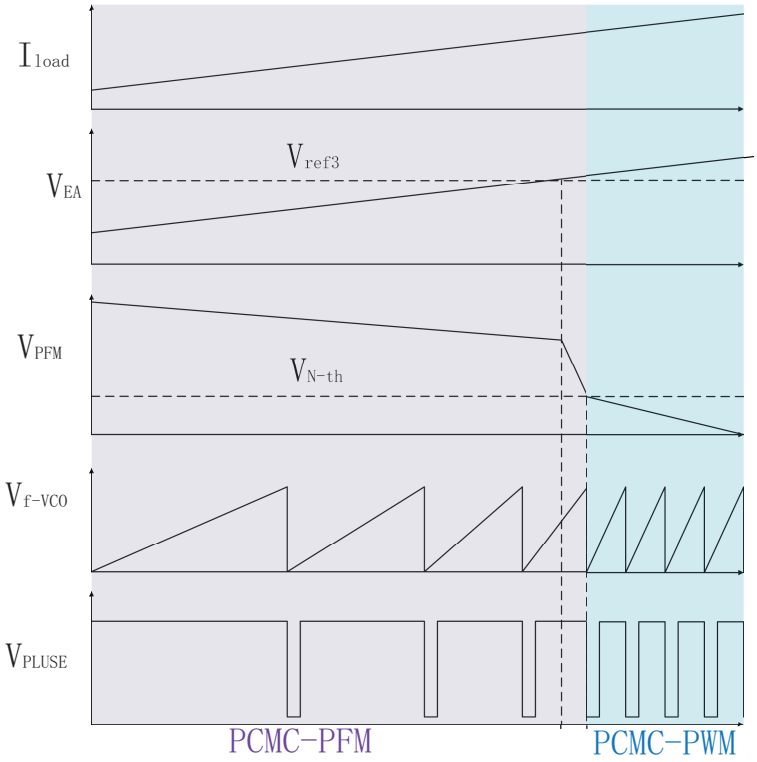

Figure 5. The correspondence curves between V_{EA}, V_{PFM} and V_{PLUSE} when the system is smoothly switched from PCMC-PFM mode to PCMC-PWM mode.

3. Implementation of Key Circuits

The error amplifier structure with H-clamp and L-clamp is introduced in Section 3.1. Section 3.2 introduces the oscillation unit consisting of PFM, VCO, and Pluse generator.

3.1. EA with H-Clamp and L-Clamp

Figure 6 shows the structure of the error amplifier containing H-clamp and L-clamp. where the main structure of the error amplifier EA is a symmetrical OTA structure. The gain of this amplifier is shown in (4), where g_{m1} is the equivalent transconductance of M_1. R_{n4} is the output resistance of node 4, and B is the current factor in the amplifier [24]. From [25] it is known that the DCDC boost converter has a right half-plane zero as shown in (5) (D is the on–off duty cycle of MN in Figure 1) it can cause system instability and requires the inclusion of a compensation circuit. The proposed boost converter system will incorporate a compensation structure in the error amplifier as shown in Figure 6.

$$A_V = g_{M1} B R_{n4} = g_{M1} \frac{W_{M5}/L_{M5}}{W_{M3}/L_{M3}} R_{n4} \tag{4}$$

$$f_{ZRHP} = \frac{V_{OUT}(1-D)^2}{2\pi I_{load} L} \tag{5}$$

V_{EA} is closely related to the ripple size of the output voltage V_{OUT} of the boost converter. V_{EA} needs to be limited otherwise too high V_{EA} will directly lead to high ripple in V_{OUT}. The size of V_{EA} also directly affects the operating mode of the boost converter. The clamp circuit shown in Figure 6 is added to the error amplifier so that the output $V_{EA} \in \left[V_{Lref}, V_{Href}\right]$. When $V_{EA} = V_{Lref}$, the Schmitt trigger flip-flop output $V_{L-clamp}$ in L-clamp is high to control the boost converter into DGM mode. The simulation result of the frequency response of the error amplifier shown in Figure 7a shows that the DC amplification gain of the error amplifier is 69.88 dB. The phase margin is 78°. The bandwidth

is 2.348 MHz. The simulation results of V_{EA} for the boost converter at different load currents are shown in Figure 7b. When I_{load} gradually increases, it will produce a decrease in V_{OUT} and eventually lead to an increase in the stable value of V_{EA} which is consistent with the theoretical derivation.

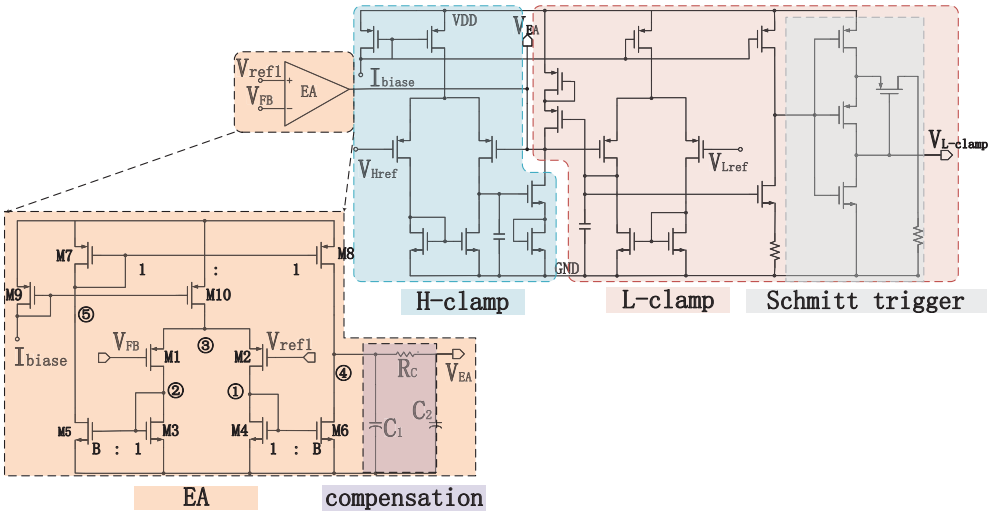

Figure 6. The structure of the error amplifier containing H-clamp and L-clamp.

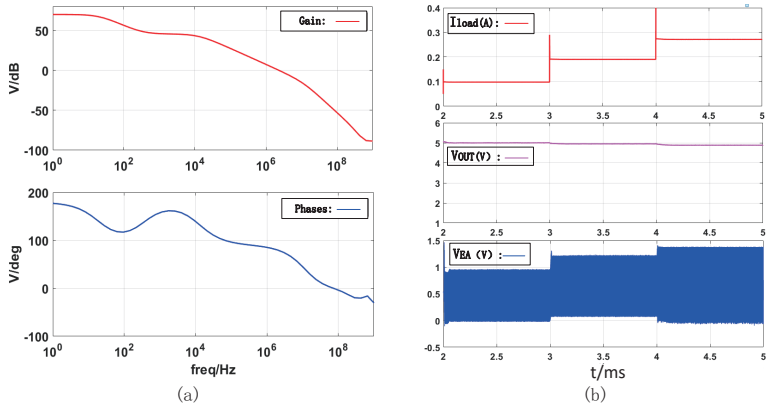

Figure 7. The simulation results of EA. (**a**) The frequency response of EA. (**b**) The correspondence of I_{load}, V_{OUT}, and V_{EA}.

3.2. Oscillation Unit

Figure 8 shows the structure of the oscillation unit composed of PFM amplifier, VCO, and PLUSE. This is where $V_{Lref} < V_{ref3} < V_{Href}$, and V_{ref3} is a fixed value to ensure M3 works in the saturation zone. The V_{ref3} with a high level during the ideal phase of the DGM mode can be used to turn off the oscillator unit to reduce the switching losses of the boost converter, where $\bar{V}_{RS-lat-1}$ is the inverse signal of $V_{RS-lat-1}$. To increase the gain of the PFM amplifier a diode connected M7 is connected at the output. $W_{M8}/L_{M8} = 1$ in the VCO structure, so M8 has a high threshold voltage V_{th-M8}. The output V_{PFM} of the PFM amplifier when $V_{Lref} < V_{EA} < V_{ref3}$ is shown in (6). At this point, it is guaranteed that $V_{PFM} > V_{th-M8}$ and M8 operates in the saturation region with an operating current as shown in (7).

$$V_{PFM} = g_{M3}\frac{1}{g_{M7}}(V_{ref3} - V_{EA}) \tag{6}$$

$$I_{DS-M8} = \frac{1}{2}\mu_n C_{OX}\frac{W_{M8}}{L_{M8}}(V_{PFM} - V_{th-M8})^2 \tag{7}$$

The current flowing through M11 charges the capacitor C_{VCO} to obtain a gradually increasing V_{f-VCO}. When $V_{f-VCO} > V_{ref4}$, V_{CMP-1} will change from low to high, this voltage is acted upon by the PLUSE to generate a high potential pulse V_{P-M12} and a low potential pulse V_{PLUSE}, where M_{12} conducts under the action of V_{P-M12} causing C_{VCO} to discharge. To ensure that C_{VCO} is fully discharged the pulse width of V_{P-M12} cannot be too small, and the pulse width can be adjusted by adjusting the resistor R_{PLUSE} and capacitor C_{PLUSE} in PLUSE. After the discharge is completed, there will be $V_{f-VCO} = 0$, then V_{P-M12} goes low and C_{VCO} starts charging again cyclically to generate a sawtooth oscillation signal. The frequency f_{VCO} of V_{f-VCO} is shown in (8a) When $V_{ref3} < V_{EA}$, $V_{PFM} < V_{th-M8}$, M_8 is turned off and the f_{VCO} is a fixed value as shown in (8b). The simulation results are shown in Figure 9.

$$f_{VCO} = \begin{cases} \frac{NI_{biase} - I_{DS-M8}}{CV_{ref4}} & (V_{Lref} < V_{EA} < V_{ref3}) \quad (8a) \\ \frac{NI_{biase}}{CV_{ref4}} & (V_{ref3} < V_{EA} < V_{Href}) \quad (8b) \end{cases} \tag{8}$$

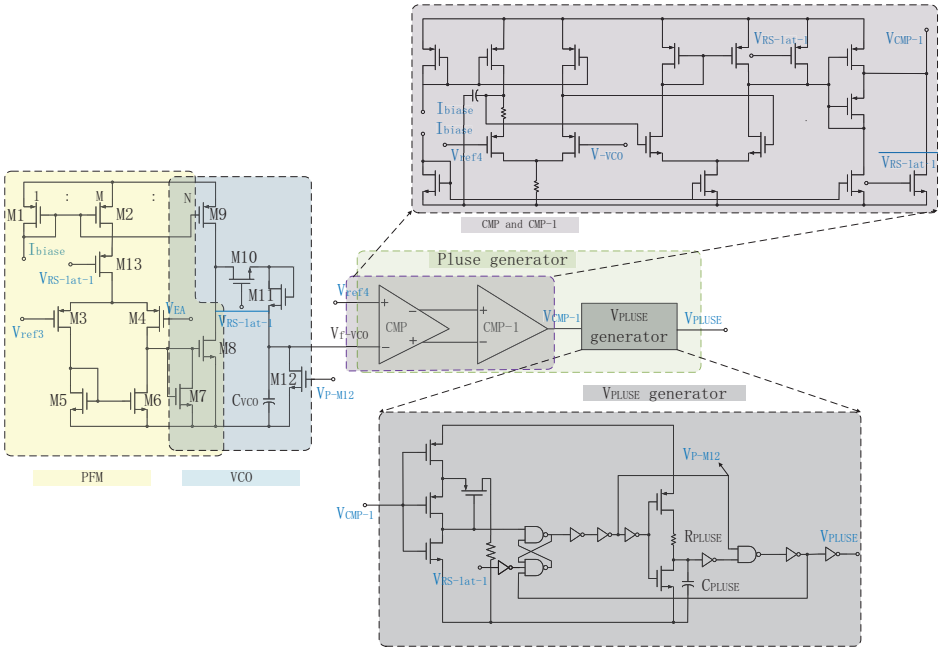

Figure 8. The structure of the oscillation unit composed of PFM amplifier, VCO, and Pluse generator.

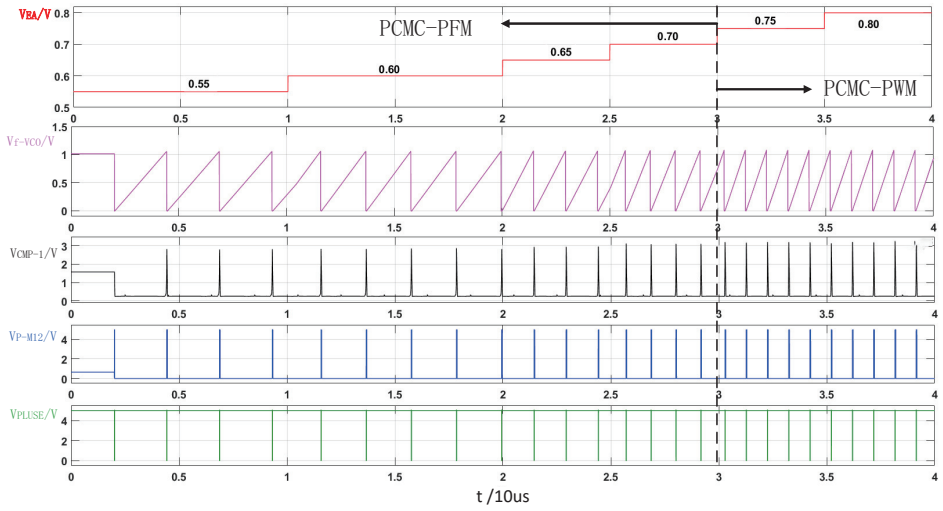

Figure 9. The simulation results of V_{EA}, $V_{(f-VCO)}$,$V_{(CMP-1)}$,$V_{(P-M12)}$, and V_{PLUSE}.

4. Measurement Results

The chip is fabricated by using 0.18 µm CMOS process and the area of the chip is 1240 µm × 780 µm as shown in Figure 10a. A 2.2 µH off-chip inductor and a 2.2 µF off-chip capacitor are used by this boost converter as shown in Figure 10b.

Figure 11a,b show test results of V_{OUT}, V_{SW} and I_{SW} in DGM operating mode of the proposed DCDC Boost converter. The load currents in Figure 11a,b are 5 mA and 20 mA, respectively. The boost converter operates in DGM mode under both load conditions. In this mode, a complete DGM cycle consists of two stages: the first stage is the inductor continuously charging and discharging for two switching cycles, at which the output voltage shows an overall rising trend; the other stage is the inductor current continues to be zero and enters the ideal stage in the DGM mode, at which the output voltage continues to decrease until the arrival of the next DGM cycle. The period of DGM is 14.9 µs with 5 mA load current and 2.3 µs with 20 mA.

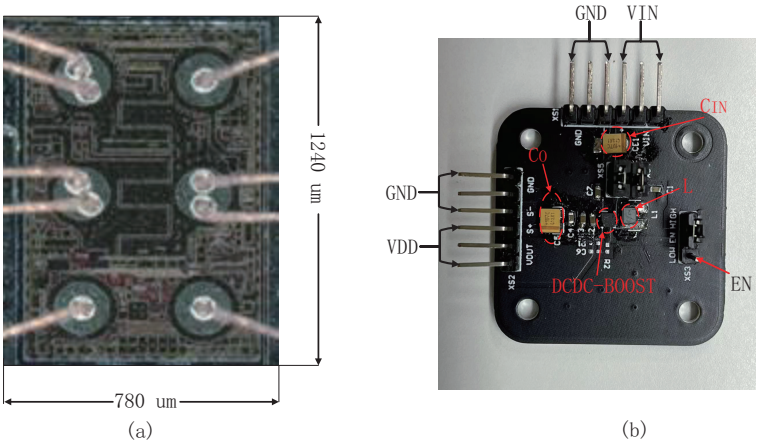

Figure 10. Microphotograph and Measurement board of the proposed DCDC Boost converter. (**a**) Microphotograph of the proposed DCDC Boost converter. (**b**) Measurement board of the proposed DCDC Boost converter.

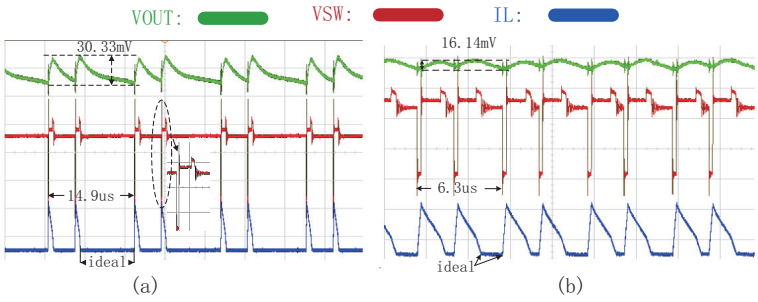

Figure 11. Test results of V_{OUT}, V_{SW}, I_{SW} in DGM operating mode of the proposed DCDC Boost converter. (**a**) When the I_{load} is 5 mA. (**b**) When the I_{load} is 20 mA.

Figure 12a,b show test results of V_{OUT}, V_{SW}, and I_{SW} in PCMC-PFM operating mode of the proposed DCDC Boost converter. The load currents in Figure 12a,b are 50 mA and 100 mA, respectively, and the boost converter operates in PCMC-PFM mode for both load conditions. It has a continuous switching frequency of 479 K Hz at 50 mA load current and 799 K Hz at 100 mA. Figure 13a,b show test results of V_{OUT}, V_{SW} and I_{SW} in PCMC-PWM operating mode of the proposed DCDC Boost converter. The load currents in Figure 13a,b are 200 mA and 250 mA, respectively. The boost converters in both load conditions operate in PWM mode with a fixed and continuous switching frequency of 1.45 M Hz.

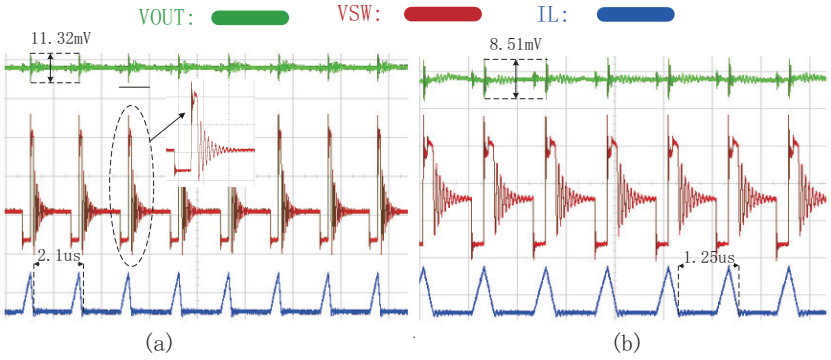

Figure 12. Test results of V_{OUT}, V_{SW}, I_{SW} in PCMC-PFM operating mode of the proposed DCDC Boost converter. (**a**) When the I_{load} is 50 mA. (**b**) When the I_{load} is 100 mA.

Figure 14a–d show the results of the load conversion response test results of the boost converter. In Figure 14a, the load is switched from 10 mA to 50 mA and the converter is switched from DGM mode to PFM mode with a response time of 30.3 µs. The switching within the PFM mode is shown in Figure 14b, where the load is switched from 50 mA to 100 mA with a response time of 28.1 µs. The test results shown in Figure 14c,d are for switching from PFM mode to PWM mode. In Figure 14c, the load current is switched from 100 mA to 200 mA with a response time of 18.5 µs. In Figure 14d, the load current is switched from 50 mA to 250 mA with a response time of 40.8 µs.

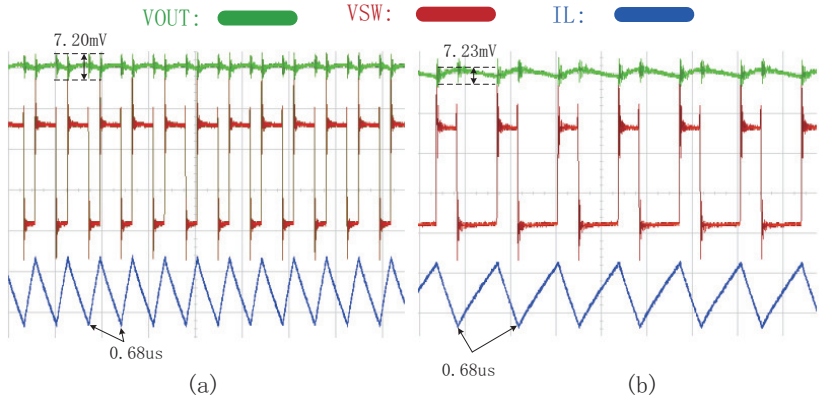

Figure 13. Test results of V_{OUT}, V_{SW}, I_{SW} in PCMC-PWM operating mode of the proposed DCDC Boost converter. (**a**) When the I_{load} is 200 mA. (**b**) When the I_{load} is 250 mA.

Figure 15 shows the efficiency of the boost converter for different load currents at an input voltage of 3.6 V. A peak efficiency of 94.7% can be achieved at a load current of 198 mA, and the efficiency is greater than 90% for $I_{load} \in$ [30 mA, 300 mA].

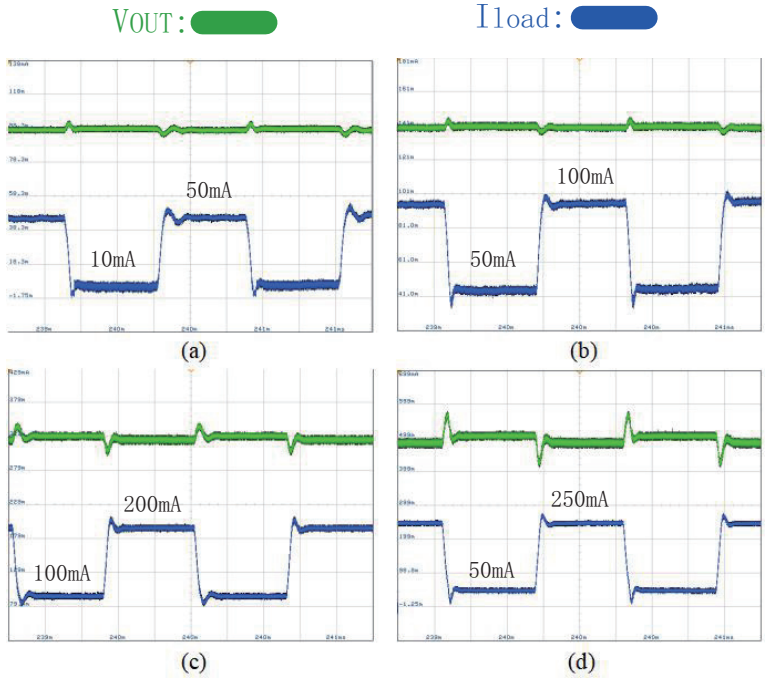

Figure 14. The test results of the load conversion response. (**a**) The load is switched from 10 mA to 50 mA. (**b**) The load is switched from 50 mA to 100 mA. (**c**) The load is switched from 100 mA to 200 mA. (**d**) The load is switched from 50 mA to 250 mA.

The proposed boost converter allows a maximum load current of 50 mA at an input voltage of 0.8 V. With this input voltage, the boost converter cannot operate properly when the load current is greater than 50 mA. Therefore, the linear and load regulation analysis of the proposed boost converter should be divided into two cases. The two cases for linear regulation rate analysis are: the load current is 50 mA and the load current is the maximum load current of the system which is 300 mA. Figure 16a,b shows the test results of output voltage variation with input voltage for load currents of 50 mA and 300 mA, respectively. Figure 16a shows an output voltage of 4.75 V at an input voltage of 0.8 V and an output voltage of 5.00 V at an input voltage of 5 V; Figure 16b shows an output voltage of 4.84 V at an input voltage of 2.4 V and 4.99 V at an input voltage of 5 V. Then, the linear adjustment rate of the boost converter is 0.238%/V for a load current of 50 mA and 1.156%/V for a load current of 300 mA from (9).

$$line - reg = 100\frac{\Delta V_{out}/V_{out}}{\Delta V_{in}}(\%/V) \tag{9}$$

The two cases for load regulation rate analysis are 0.8 V and 3.6 V for the input voltage. Figure 17a,b shows the test results of output voltage variation with load current when the input voltage is 0.8 V and 3.6 V, respectively. Figure 17a shows an output voltage of 4.99 V at a load current of 0 and 4.75 V at a load current of 50 mA; Figure 17b shows an output voltage of 5.00 V at a load current of 0 and 4.86 V at a load current of 300 mA. The load regulation of the boost converter is 0.096%/mA for an input voltage of 0.8 V and 9.33×10^{-3}%/mA for an input voltage of 3.6 V from (10).

$$load - reg = 100\frac{\Delta V_{out}/V_{out}}{\Delta I_{load}}(\%/V) \tag{10}$$

Table 1 shows the performance comparison of the proposed DGM/PCMC-PFM/PCMC-PWM hybrid modulation mode boost converter compared with the hybrid modulation converter proposed in the published works. The proposed boost converter in this paper can achieve a higher efficiency of 94.7% for the same process with similar Die Area. The

proposed boost converter in this paper has a larger input voltage range of 0.8–5 V and a larger load current range of 5–300 mA.

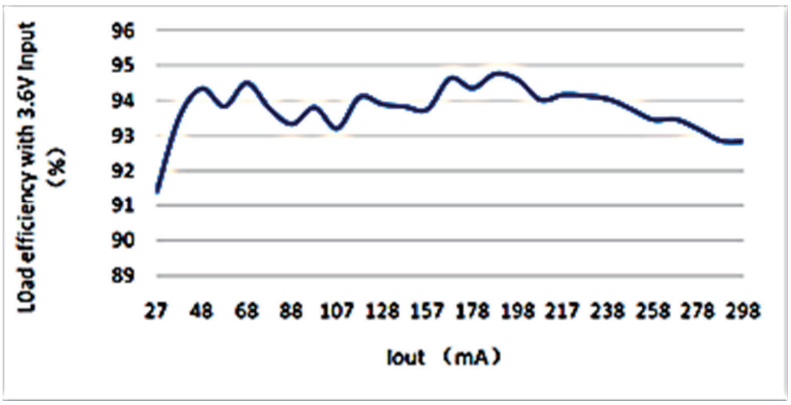

Figure 15. The efficiency of the proposed boost converter.

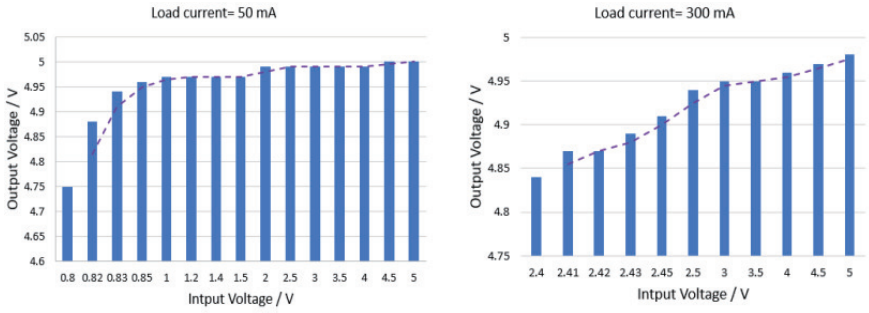

Figure 16. The test results of output voltage variation with input voltage when the load currents is identified. (**a**) The load current is 50 mA. (**b**)The load current is 300 mA.

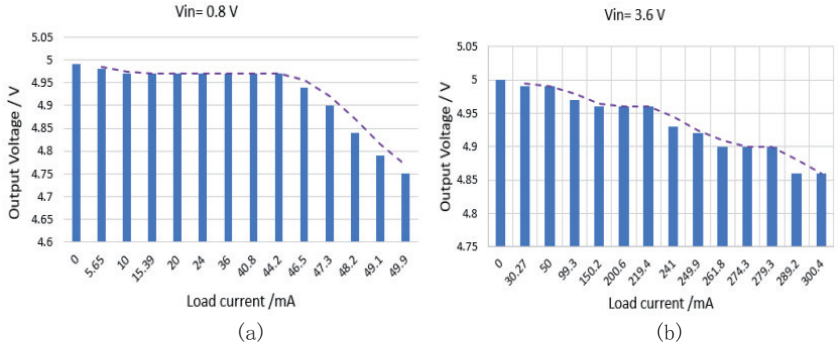

Figure 17. The the test results of output voltage variation with load current when the input voltage is identified. (**a**) The input voltage is 0.8 V. (**b**) The input voltage is 3.6 V.

Table 1. Performance comparison with prior works.

	[26]	[27]	[16]	[9]	[28]	**This Work**
Technology (um)	0.18	0.13	0.18	0.18	0.18	0.18
Switching freq. (MHz)	1.65	2.5	7.4	4	1.7	1.65
Input Voltage (V)	0.55–1	2.2–3.3	2.0–3.3	2.7–4.7	2.2–5.0	0.8–5.0
Onput Voltage (V)	0.35–0.5	1.7	1.2	1.6	1.8	5.0
Mode	PWM/PFM/AM [1]	PWM/PFM/SSCG [2]	MSPWM [3]/PFM/PWM	PWM/PFM/DGM	On–time–based	PCMC–PFM/PCMC–PWM/DGM
Load current (mA)	0.1–20	0.01–20	200	0.001–100	0.2–100	5–300
Peak efficiency (%)	92	92.4	91	92.1	94	94.7
Die Area (mm^2)	1.2 × 1.2	0.82 × 0.8	0.97 × 0.88	1.0 × 0.55	1.35 × 1.2	1.24 × 0.78
Inductor (uH)	4.7	3.0	1	4.7	4.7	2.2
Capacitor (uF)	–	3.0	2.2	4.7	1	20

[1] AM: Asynchronous mode. [2] SSCG: Retention Compensated. [3] MSPWM: Multiple-sawtooth PWM.

5. Conclusions

This paper introduces a DCDC boost converter for wearable devices. A hybrid DGM/PCMC-PFM/PCMC-PWM modulation technique is used to achieve high conversion efficiency over a wide load range. Frequency modulation in PCMC-PFM mode is implemented under load current-based conditions. Smooth switching from PCMC-PFM to PCMC-PWM mode without adding any additional control module. The boost converter is fabricated in a 0.18 µm CMOS process and the test results show that the peak efficiency of the boost converter can reach 94.7%. A wide input voltage range of 0.8–5 V and a wide load current range of 5–300 mA can be achieved. At 3.6 V input voltage, the conversion efficiency of more than 90% can be achieved in the load current range of 30–300 mA.

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References

1. IMARC Group. Available online: https://www.imarcgroup.com/global-wearable-technology-market/ (accessed on 19 September 2022)
2. Seneviratne, S.; Hu, Y.; Nguyen, T.; Lan, G.; Khalifa, S.; Thilakarathna, K.; Hassan, M.; Seneviratne, A. A Survey of Wearable Devices and Challenges. *IEEE Commun. Surv. Tutor.* **2017**, *19*, 2573–2620. [CrossRef]
3. Motti; V ,G. *Introduction to Wearable Computers*; Wearable Interaction; Springer: Cham, Switzerland, 2020; pp. 1–39.
4. Jain, N.; Chaudhary, A.; Sindhwani, N.; Rana, A. Applications of Wearable devices in IoT. In Proceedings of the 2021 9th International Conference on Reliability, Infocom Technologies and Optimization (Trends and Future Directions) (ICRITO), Noida, India, 3–4 September 2021.
5. ReadWrite. Available online: http://readwrite.com/2015/08/14/battery-innovation-needed/ (accessed on 8 November 2016)
6. Ballo, A.; Grasso, A. D.; Palumbo, G. A Subthreshold Cross-Coupled Hybrid Charge Pump for 50-mV Cold-Start. *IEEE Access* **2020**, *8*, 188959–188969. [CrossRef]
7. Im, J. P.; Wang, S. W.; Ryu, S. T.; Cho, G. H. A 40 mV transformer reuse self-startup boost converter with MPPT control for thermoelectric energy harvesting. *IEEE J. Solid-State Circuits* **2012**, *47*, 3055–3067. [CrossRef]
8. Chen, P. H.; Fan, P. Y. An 83.4% peak efficiency single-inductor multiple-output based adaptive gate biasing DC-DC converter for thermoelectric energy harvesting. *IEEE Trans. Circuits Syst.* **2015**, *62*, 405–412. [CrossRef]

9. Zhao, M.; Li, M.; Song, S.; Hu, Y.; Yao, Y.; Bai, X.; Hu, R.; Wu, X.; Tan, Z. An Ultra-Low Quiescent Current Tri-Mode DC-DC Buck Converter With 92.1% Peak Efficiency for IoT Applications. *IEEE Trans. Circuits Syst.* **2022**, *69*, 428–439. [CrossRef]
10. Jiang, H.; Y. Guo Y.; Wu, Z.; Zhang, C.; Jia, W.; Wang, Z. Implantable Wireless Intracranial Pressure Monitoring Based on Air Pressure Sensing. *IEEE Trans. Biomed. Circuits Syst.* **2018**, *12*, 1076–1087. [CrossRef]
11. 10. Tang, Z.; Fang,Y.; Shi, Z.; Yu, X.; Tan, N. N.; Pan, W. A 1770-um^2 leakage-based digital temperature sensor with supply sensitivity suppression in 55-nm CMOS. *IEEE-Solid-State Circuits* **2020**, *55*, 781–793. [CrossRef]
12. Van den Steen, S.; Eyerman, S.; De Pestel, S.; Mechri, M.; Carlson, T. E.; Black-Schaffer, D.; Hagersten, E.; Eeckhout, L. Analytical Processor Performance and Power Modeling Using Micro-Architecture Independent Characteristics. *IEEE Trans. Comput.* **2016**, *65*, 1557–9956. [CrossRef]
13. Walravens, C.; Dehaene, W. Low-power digital signal processor architecture for wireless sensor nodes. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2014**, *22*, 313–321. [CrossRef]
14. Ma,S.; Wu, T.; Zhang, J.; Ren, J. A 5G wireless event-driven sensor chip for online power-line disturbances detecting network in 0.25 um GaAs process. *IEEE Trans. Ind. Electron.* **2021**, *68*, 5271–5280. [CrossRef]
15. Seth, S.; Kwon, D. H.; Venugopalan, S.; Son, S. W.; Zuo, Y.; Bhagavatula, V.; Lim, J.; Oh, D.; Cho, T. B. A Dynamically Biased Multiband 2G/3G/4G Cellular Transmitter in 28 nm CMOS. *IEEE J. -Solid-State Circuits* **2016**, *51*, 1096–1108. [CrossRef]
16. Hong, W.; Lee, M.; A 7.4-MHz tri-mode DC-DC buck converter with load current prediction scheme and seamless mode transition for IoT applications. *IEEE Trans. Circuits Syst.* **2020**, *67*, 4544–4555. [CrossRef]
17. Zeng, W. L.; Ren, Y.; Lam, C. S.; Sin, S. W.; Che, W. K.; Ding, R.; Martins, R. P. A 470-nA Quiescent Current and 92.7%/94.7% Efficiency DCT/PWM Control Buck Converter With Seamless Mode Selection for IoT Application. *IEEE Trans. Circuits Syst.* **2020**, *67*, 4085–4098. [CrossRef]
18. Ballo, A.; Grasso, A.D.; Palumbo, G. A Review of Charge Pump Topologies for the Power Management of IoT Nodes. *Electronics* **2019**, *8*, 480. [CrossRef]
19. Ballo, A.; Grasso, A. D.; Palumbo, G. Current-mode body-biased switch to increase performance of linear charge pumps. *Int. J. Circuit Theory Appl.* **2020**, *48*, 1864–1872. [CrossRef]
20. Ming, D. L.; Lee, Y. H.; Chen, K. H. A high efficiency adaptive frequency hopping controlled 1/3× step-down switch capacitor DC-DC converter with deep-green mode operation. In Proceedings of the 2012 IEEE International Symposium on Circuits and Systems (ISCAS), Seoul, Korea, 20–23 May 2012.
21. Lee Li, M. C;. C. H.; Yang, X. X. Implementation of DC-DC PFM Boost Power Converter for Low-power Energy Harvesting Applications. In Proceedings of the 2021 11th International Conference on Power, Energy and Electrical Engineering (CPEEE), Shiga, Japan, 26–28 February 2021.
22. Zhang, S.; Zhao, M.; Wu, X.; Zhang, H. Dual-phase DC–DC buck converter with light-load performance enhancement for portable applications. *IET Power Electron.* **2018**, *11*, 719–726 [CrossRef]
23. Chen, P.H.; Cheng, H.C.; Ai, Y.A.; Chung, W.T. Automatic modeselected energy harvesting interface with >80% power efficiency over 200 nW to 10 mW. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2018**, *26*, 2898–2906. [CrossRef]
24. Sansen, W.M.C. *Analog Design Essentials*; Tsinghua University Press: Beijing, China, 2022; pp. 144–151.
25. Yu-Chien Hsu, Dan Chen, Sheng-Fu Hsiao, Chun-Shih Huang and Hung-Yu Cheng, Modeling of the control behavior of current-mode constant on-time boost converters. In Proceedings of the 2015 IEEE 2nd International Future Energy Electronics Conference (IFEEC), Taipei, Taiwan, 1–4 November 2015.
26. Chen, P. H.; Shiang, C.; Lin, K. C. A 50 nW to 10 mW output power tri-mode digital buck converter with self-tracking zero current detection for photovoltaic energy harvesting. *IEEE J. Solid-State Circuits* **2016**, *51*, 523–532.
27. Park, Y. J.; Park, J. H.; Kim, H. J.; Ryu, H.; Kim, S.; Pu, Y.; Hwang, K. C.; Yang, Y.; Lee, M.; Y. Lee, K. A Design of a 92.4% Efficiency Triple Mode Control DC–DC Buck Converter With Low Power Retention Mode and Adaptive Zero Current Detector for IoT/Wearable Applications. *IEEE Trans. Power Electron.* **2017**, *32*, 6946–6960. [CrossRef]
28. Park, W. Namgoong, G.; Choi, E.; Lee, B.; Park, H.; Ma, H.; Bien, F. A 94% Peak Efficiency Dual Mode Buck Converter with Fully Integrated On-time-based Mode Control for Implantable Medical Devices. *IEEE Trans. Circuits Syst. II Express Briefs* **2022**, 1. [CrossRef]