

Communication

HfO_x/Ge RRAM with High ON/OFF Ratio and Good Endurance

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Abstract: A trade-off between the memory window and the endurance exists for transition-metal-oxide RRAM. In this work, we demonstrated that HfO_x/Ge-based metal-insulator-semiconductor RRAM devices possess both a larger memory window and longer endurance compared with metal-insulator-metal (MIM) RRAM devices. Under DC cycling, HfO_x/Ge devices exhibit a 100× larger memory window compared to HfO_x MIM devices, and a DC sweep of up to 20,000 cycles was achieved with the devices. The devices also realize low static power down to 1 nW as FPGA's pull-up/pull-down resistors. Thus, HfO_x/Ge devices act as a promising candidates for various applications such as FPGA or compute-in-memory, in which both a high ON/OFF ratio and decent endurance are required.

Keywords: Germanium; HfO_x RRAM; MIGe; endurance; memory window

1. Introduction

Resistive random access memory (RRAM) has been intensively investigated for its diversified applications, including embedded memory, storage class memory, FPGA, and in-memory computation of neural networks [1–3]. Metal Oxide (i.e., HfO_x, TaO_x, NiO, and TiO₂) is commonly applied as the switching layer sandwiched between two metal electrodes to build a metal-insulator-metal (MIM) structure. Among various switching layer materials, hafnium oxide (HfO_x) stands out owing to its technical maturity, fab-friendliness, and decent device performance [4–6]. The choice of metal electrodes affects the behavior of HfO_x-based RRAM a lot. Normally, when noble metal (i.e., Pt and Ru) is constructed as the top and bottom electrodes [7–9], the devices have unipolar switching because the conductive filament (CF) is annihilated by thermal diffusion. However, the switching behavior of unipolar RRAM is unstable, and the current during the annihilation of CF is too large for the applications of embedded memory, FPGA, and in-memory computation. As for bipolar RRAM, the materials of the top electrode are usually Ti, W, Al, and TiN [4,10–15]. Table 1 shows the benchmark of bipolar HfO_x-based RRAM with different electrodes. It is reported that the endurance is 10⁶–10⁷ in reference [11,14], but the memory window (i.e., the ratio between high and low resistance states) is ~10. Reference [12] improved endurance to 10¹⁰ by utilizing oxygen plasma treatment within Ti/HfO₂/TiN structured RRAM, while the memory window is 10² and the operation voltage is larger than 3 V. Moreover, reference [10] realized a larger memory window up to 10⁵ as the thickness of HfO₂ is 24.7 nm. It is observed that endurance can be improved by increasing the extra available oxygen ions in HfO₂, and the memory window can be enlarged using a thicker HfO₂ film. Nevertheless, both a large memory window and long endurance achieved in one RRAM device are difficult when the HfO₂ film is less than 10 nm. In other words, there is generally a trade-off between the memory window and the endurance of MIM RRAM [16].



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Table 1. Benchmark of bipolar HfO_x-based RRAM.

Ref.	Structure	Window	Retention	Endurance	V _F /V _{SET} /V _{RESET}	I _{CC}
[10]	TiN/HfO ₂ /Pt	10 ⁵	10 ⁴ s	NS ¹	FF ² /−4.3/6 V	NS
[11]	W/Zr/HfO ₂ /TiN	>10	NS	>10 ⁶	2/0.5/−1.25 V	50 μA
[12]	Ti/HfO ₂ /TiN	10 ²	10 ⁴ s	10 ¹⁰	NS/3/−3.5 V	1 mA
[13]	Al/HfO _x /Al	10 ⁴	NS	NS	1/1.8/0.8 V	1 μA–1 mA
[14]	Ti/HfO ₂ /TiN	>10	10 ⁴ s	>10 ⁷	FF/0.5/−0.5 V	NS
[4]	TiN(Ti)/HfO _x /W	~10	NS	>10 ⁴	2.5/0.5/−1 V	500 μA
[15]	Ti/HfO _x /Pt	40	>10 ⁵	>10 ³	2.5/0.5/−0.7 V	1 mA

¹ Not Specified. ² Forming Free.

As of today, MIM-based HfO_x RRAM is gradually entering the market at 40 nm technology nodes and beyond in embedded or standalone memory applications [17,18]. For advanced applications such as FPGA's pull-up/pull-down resistors [19], or compute-in-memory (CIM) [20], both a low leakage in the high resistance state (HRS) and a large memory window are required to achieve good energy efficiency. Since MIM RRAMs with the HfO_x switching layer often exhibit modest memory windows, an alternative stack with a higher ON/OFF ratio is highly desired. In this work, we experimentally studied the metal-insulator-semiconductor (MIS) RRAM devices with the HfO_x switching layer and Ge or Si bottom electrodes in order to achieve a higher memory window with good endurance. In particular, a memory window over 10⁵ was achieved with Pd/HfO_x/p-Ge RRAM devices, and the conductance mechanism was analyzed in detail. Furthermore, stable DC cycles with a large memory window were demonstrated for Pd/HfO_x/p-Ge devices up to 20,000 DC sweep cycles. Compared with TiN/HfO_x/Pt devices and Pd/HfO_x/p⁺-Si devices, Pd/HfO_x/p-Ge devices possess better DC endurance under the same test condition. These results suggest HfO_x/Ge RRAM device is a promising candidate for FPGA and CIM applications.

2. Materials and Methods

Two types of devices were fabricated, including MIS and MIM devices. For MIS devices, Pd/HfO_x/p-Ge devices and Pd/HfO_x/p⁺-Si devices were fabricated. The process flow is depicted in Figure 1a. After the wafer cleaning, 7 nm HfO_x was deposited on Ge or Si substrates by Atomic Layer Deposition (ALD). The ozone post oxidation (OPO) is not processed here in contrast with the process of previous HfO_x/Ge RRAM [21,22]. It is not only because the interface is vital for previous RRAM stack used in MOSFET, but the stack variable here needs to be the same as the one in MIM devices. Subsequently, the lithography process and Pd deposition were carried out, and a lift-off process was utilized to form the top electrode. Al was finally deposited using thermal evaporation as a contact metal to Ge or Si substrates. To distinguish the Ge-based and Si-based devices, hereinafter MIGe is used to refer Pd/HfO_x/p-Ge devices, and MISi is used to refer Pd/HfO_x/p⁺-Si devices. For MIM devices, a typical TiN/HfO_x/Pt device was fabricated by the following process flow. First, back electrode Pt was sputtered on a SiO₂ substrate. Next, 7 nm HfO_x as the switching layer and 15 nm TiN as the top electrode were sequentially deposited by ALD. Afterward, the contact metal W was deposited by sputtering and patterned by lithography. Lastly, a W/TiN/HfO_x stack was etched layer by layer using Inductive Coupled Plasma (ICP) tool to expose the bottom electrode.

The DC I-V characterizations were carried out by Agilent B1500A semiconductor parameter analyzer. SET and RESET operations were achieved by sweeping from a non-zero voltage V_{start} to a larger voltage V_{end}, where V_{end} was large enough to trigger the switching event. During the SET operation, current compliance (CC) was exerted by B1500A on MIGe/MISi devices (CC = 50 μA) and MIM devices (CC = 1 mA). The READ operations were achieved by applying single-point voltage on the device and measuring the currents for resistance calculation.

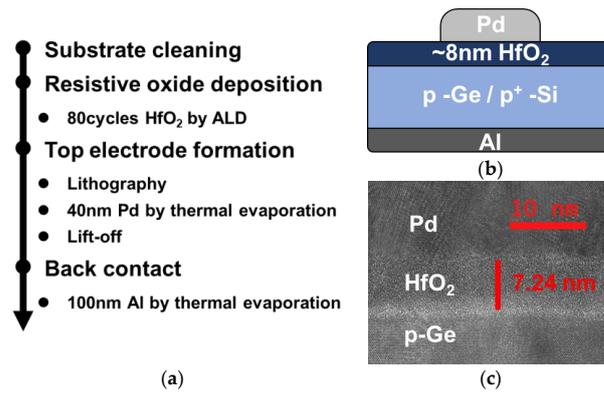


Figure 1. MIGe RRAM devices' (a) process flow, (b) structure schematic and (c) TEM graph.

3. Results and Discussion

Typical DC I-V characteristics were measured for Pd/HfO_x/p-Ge and TiN/HfO_x/Pt devices, as shown in Figure 2. For MIM devices, stable low resistance states (LRS) can be achieved by 1 mA CC, and the resistance of high resistance states (HRS) is roughly 10⁴ times the virgin-state resistance. The memory window of MIM devices is around 10³, while a larger memory window of over 10⁵ is realized in MIGe devices. It is worth noting that the HRS current of MIGe devices is approximately equal to the current of virgin states, implying a complete annihilation of the conductive filament (CF). Furthermore, the low operation current of MIGe (CC = 50 μA) leads to the advantage of low operating power. The RESET current of MIM devices is around several mA while that of MIGe devices is around 100 μA, in line with the SET current compliance. Thus, the write power of MIGe devices is estimated to be dozens of times smaller than that of MIM devices. For MIM devices, if a lower CC is applied to reduce the operation power, the memory window will also shrink significantly.

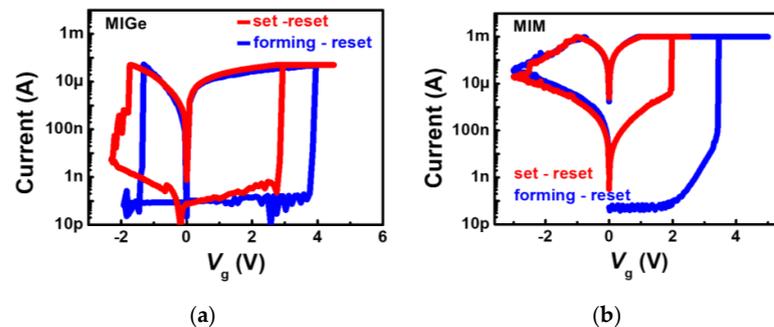


Figure 2. DC I-V_g curves of (a) Pd/HfO_x/p-Ge devices and (b) TiN/HfO_x/Pt devices.

It is worth pointing out that the effective voltage drops on the oxide stack (V_{ox}) of MIGe devices are less than the voltage applied on the gate/top electrode (V_g). There are two situations: (a) The MIGe device works like a MOS when it is at HRS due to the negligible CF; (b) When the MIGe device works at LRS, the CF is conductive, so the device is not equivalent to a MOS. In the case of HRS, the voltage on the gate contributes to a series of oxide capacitance (C_{ox}) and substrate capacitance (C_s). The total capacitance (C_{tot}) is approximate to oxide capacitance at negative bias; thus, the voltage drop on the oxide stack is equal to V_g . While the device is positively biased, the surface potential, which is equal to the voltage dropped on the substrate (V_s), is extracted using a quasi-static technique [23,24]. The surface potential is expressed as Equation (1):

$$\varphi_s(V_g) = \int_{V_{acc}}^{V_g} \left[1 - \frac{C(V_g)}{C_{ox}} \right] dV_g + \Delta \tag{1}$$

where, Δ is correction factor and expressed as:

$$\Delta = \int_{V_{acc}}^{V_{FB}} \left[1 - \frac{C(V_g)}{C_{ox}} \right] dV_g \quad (2)$$

To obtain V_{FB} , C_{FB} needs to be calculated firstly using Equation (3):

$$C_{FB} = \frac{1}{\frac{1}{C_{ox}} + \frac{1}{C_s}}, \quad C_s = \frac{\epsilon_s \epsilon_0}{D_{deby}} = \frac{\epsilon_s \epsilon_0}{\sqrt{kT \epsilon_s \epsilon_0 / q^2 NA}} \quad (3)$$

NA is $5 \times 10^{16} / \text{cm}^3$, and ϵ_s is the relative permittivity of Germanium. Derived from Equation (1), the voltage across the RRAM stack and substrate varies with the gate voltage, as plotted in Figure 3. It is indicated that the practical voltage across the RRAM stack is the same as what is in MIM RRAM. Moreover, the substrate doping concentration does not affect the switching behavior except for the operation voltage due to the partial voltage on the substrate. Hence, the scalability will not be affected by the substrate doping concentration. As for the LRS state, the voltage across the RRAM stack and the substrate will be discussed further in this paper.

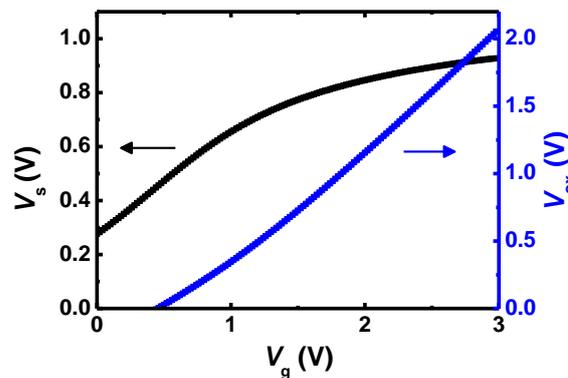


Figure 3. The voltage drops across the RRAM stack (V_{ox} , the curve in blue) and substrate (V_s , the curve in black) when the device is positively biased.

To further understand the conduction mechanisms of MIGe devices, double logarithmic J - E curves in LRS were plotted. As shown in Figure 4a, the fitting results suggest that two different conductive mechanisms exist for MIGe devices. When the applied voltage on the top electrode (TE) is less than V_1 , the conduction behavior is ohmic because $\ln(J)$ is proportional to $\ln(E)$, and the slope is around 1. When the voltage on the TE increases above V_1 , the slope of the curve reduces to smaller than 1. The current density vs. electric field data fits well with the Schottky emission equation in which $\ln(J) \propto E^{1/2}$ [25]. Based on the Schottky emission equation, the barrier height Φ_B is calculated to be 0.35 eV, while the electron effective mass in HfO_x is approximated to be about $0.11 m_0$ [26]. The conductive current through CF is contributed by electrons, which are the minority carriers for MIGe devices. A comparatively low current through CF, especially at the moment of CF forming, could help limit the overgrowth of the CF region [27]. For MIM devices, the J - E curve is symmetric, as shown in Figure 4b, and the slopes are both around 1. Plenty of free electrons are available from the two metal electrodes leading to a high operating current.

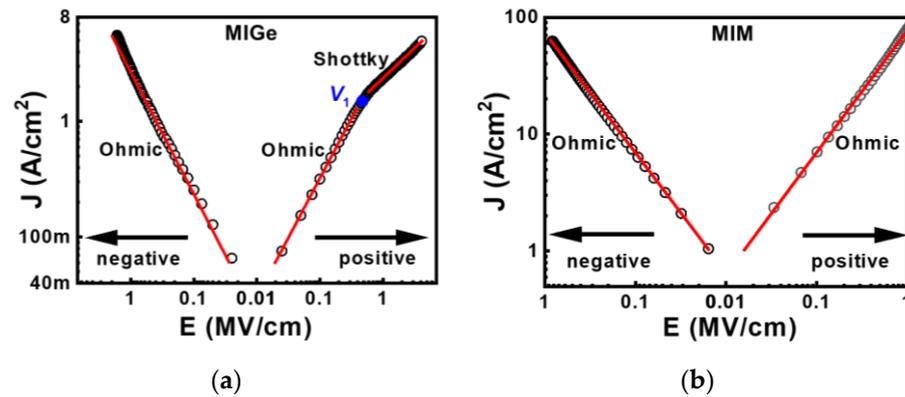


Figure 4. J - E curves of (a) Pd/HfO_x/p-Ge devices and (b) TiN/HfO_x/Pt devices in low resistance state.

Figure 5 exhibits the energy band diagram for the illustration of electronic transport mechanisms when the MIGe device works at HRS. As shown in Figure 5d, the voltage drop, V_g , is divided between the oxide switching layer and Ge substrate. When negatively biased, the resistance of the Ge substrate is negligible, and the resistance of CF (R_{CF}) can be extracted from I - V_g . Then the voltage dropped on the Ge substrate (V_s) could be derived as $V_g - I \cdot R_{CF}$, where $I \cdot R_{CF}$ is approximately the voltage on the switching oxide (V_{ox}). Therefore, V_g is almost equal to V_{ox} when the device is negatively biased ($V_g < 0$). On the other hand, when $V_g > V_1$, V_g is mostly distributed to V_s . As depicted in Figure 5b, the conductive filament consists of abundant oxygen vacancies (V_O), which can gather to form a quasi-continuous defect energy band in the bandgap of HfO_x [28]. In this case, the filament consisting of V_O can be treated as a metallic conducting path between the TE and Ge substrate at negative biases (Figure 5a). However, when the V_g is positive and larger than V_1 , the electrons from the Ge substrate need to overcome an energy barrier of 0.35 eV to reach the defect levels of the CF (Figure 5c). From the experimental data, it is estimated that the energy level of CF is close to the conduction band minimum (CBM) of Ge and roughly 1.75 eV below the CBM of HfO₂. This energy level is consistent with previous studies, which identified V_O levels to be ranging from 1.2 to 2.1 eV below the CBM of HfO₂ [29–31].

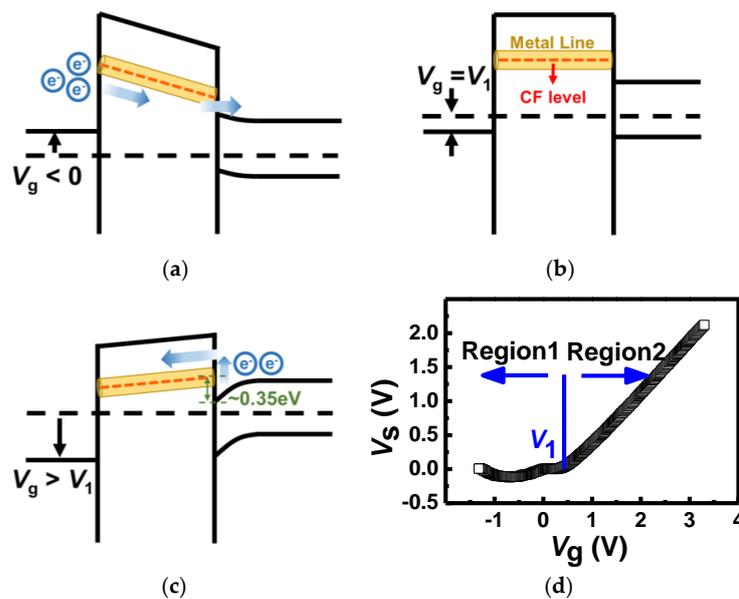


Figure 5. Energy band diagram of current transmission at (a) region 1, (b) region 2, (c) $V_g = V_1$. (d) V_s - V_g curve. (V_s : the voltage dropped on Ge substrate; V_g : the voltage applied on the gate.)

Furthermore, the DC endurance was characterized for Pd/HfO_x/p-Ge, Pd/HfO_x/p⁺-Si, and TiN/HfO_x/Pt devices. The sequence of SET-READ-RESET-READ cycles was used, and devices with the same dimension (40 μm × 40 μm) were characterized. The cycling results of MIGe and MIM devices were plotted in Figure 6, which suggests different endurance failure phenomena of MIGe and MIM devices. For MIM devices, it can be observed that a sudden hard breakdown happened during the RESET, as shown in Figure 6d. Its endurance failure behavior is similar to those that originated from the depletion of O²⁻ which induced the RESET difficulty and increased vacancy concentrations [19,32]. In contrast, the MIGe devices maintained a stable endurance window of 100× or more but failed when the HRS and LRS converged into an intermediate state, as shown in Figure 6a,b. Although the distribution of HRS appears to be wide on account of the randomness of oxygen ion movement, pulse programming is an effective approach to improve the uniformity of HRS [10]. Pulse characterizations were implemented further for MIGe and MIM devices (data not shown here). The results of pulse endurance are in correspondence with the results of DC endurance. The MIGe device is still functional after 10⁵ fully successful switching cycles, whereas the MIM device broke down after 10⁴ pulse switching cycles. The effective operation cycles of the MIGe device (>10⁵) are sufficient for CIM [33] since the SET/RESET operations will not be executed frequently.

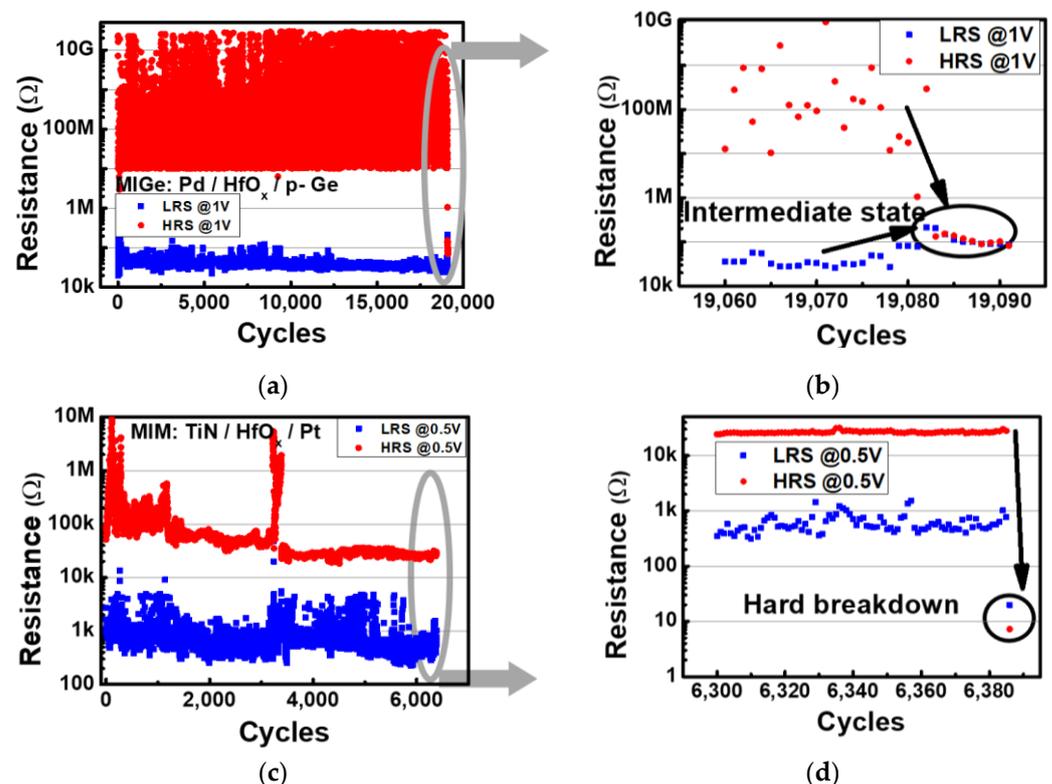


Figure 6. DC endurance cycles of (a) Pd/HfO_x/p-Ge devices (10 MΩ for minimum of HRS and 500 kΩ for maximum of LRS in test code) and (c) TiN/HfO_x/Pt devices (50 kΩ for minimum of HRS and 5 kΩ for maximum of LRS in test code); DC endurance failure of (b) Pd/HfO_x/p-Ge devices and (d) TiN/HfO_x/Pt devices.

In addition to the larger and more stable memory window achieved by MIGe devices, it is also demonstrated that the devices have superior endurance over the other two types of devices. To further confirm the superior endurance performance of MIGe devices compared to MISi and MIM, DC endurance tests were further carried out for multiple devices of each sample. Figure 7a summarizes the mean DC endurance of MIGe, MISi, and MIM devices. The mean DC endurance of MIGe devices is around 10⁴, while that of MIM devices is ten times smaller. Moreover, the static power of FPGA's pull-up/pull-down resistors when

implemented with RRAM was calculated [2]. For FPGA's configuration memory, the 1T2R structure was widely investigated. In these two resistors, usually one is ON, and the other is OFF. Therefore, the static power mainly depends on the OFF state resistor. Figure 7b compares the static powers of MIGe, MISi, and MIM devices at a 1.8 V supply. The results suggest that MIGe RRAM is a promising candidate for FPGA's pull-up/pull-down resistors.

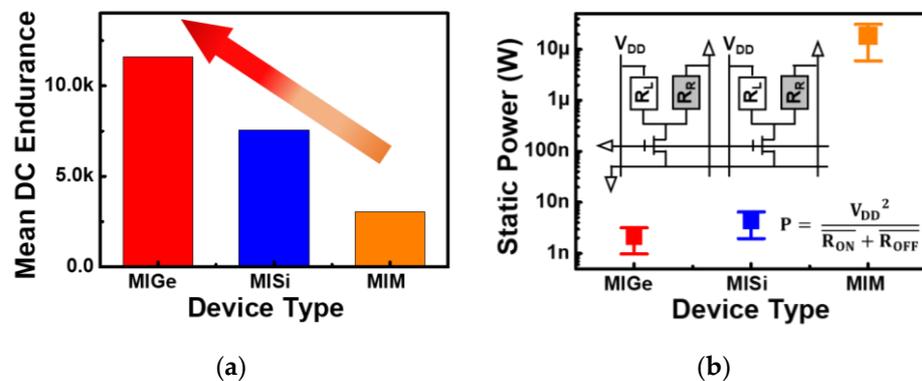


Figure 7. MIGe, MISi and MIM devices' (a) mean DC endurance and (b) static power ($V_{dd} = 1.8$ V) of FPGA's pull-up/pull-down resistors.

4. Conclusions

In conclusion, a large memory window of over 10^5 was demonstrated for Pd/HfO_x/p-Ge RRAM devices. Furthermore, the devices have been proven to have better endurance and a more stable memory window than MISi and MIM RRAM devices. Moreover, a low static power down to 1 nW was observed in MIGe devices as FPGA's pull-up/pull-down resistors. Therefore, HfO_x/p-Ge-based RRAM is a promising candidate for FPGA applications.

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