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Threshold Voltage Recovery Time Measurement Technique Post V_{TH} Instability in Normally-Off p-Gate GaN High Electron Mobility Transistors

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Abstract: In this study, we propose a simple measurement technique to quantitatively measure the time taken by threshold voltage of normally-off p-GaN AlGaN/GaN HEMTs to recover from a nominal operational gate stress-induced instability. The proposed technique eliminates the requirement to perform a full transfer characteristic sweep post-stress, thereby eliminating the measurement-induced instability effect, often colluding precise recovery time measurement. The rate of recovery and extracted recovery times hold significance in empirically correlating the location of traps in the p-GaN or AlGaN barrier region causing V_{TH} instability. The gate of the HEMT is stressed at nominal operational drive voltages 1.5 V, 2 V, and 4 V for various time intervals from 500 µs to 100 s, and the time taken for the drain current to recover to prestress levels measured at near-threshold voltage (~1.1 V_{TH}) is measured as the threshold voltage recovery time. With increasing gate stress voltages, 2DEG gets trapped at relatively deeper trap energy levels at the AlGaN/GaN interface requiring more emission time during the process of recovery, mandating larger recovery times. At higher stress voltage of 4 V, the Schottky gate leakage current is high enough enabling injected holes to cross the AlGaN barrier and counter-compensate for the deeply trapped 2DEG, requiring relatively the same recovery times as lower stress voltages where the gate leakage is negligibly small. With increasing stress time, the amount of 2DEG trapped increases, requiring more recovery time to de-trap and beyond a certain time, saturation of the trap density occurs causing the recovery time to plateau.

Keywords: normally-off p-GaN HEMT; threshold voltage instability; 2DEG capture time; emission time; recovery time

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1. Introduction

Gallium Nitride (GaN) wide bandgap semiconductors, with their superior properties, enable power conversion systems with higher efficiency, smaller form factor and lighter weight. Spontaneous and piezoelectric polarization potential, along with its ability to form heterostructures, enables high-mobility, high-density 2-dimensional electron gas (2DEG) at the heterointerface (AlGaN/GaN), which makes GaN suitable for making High Electron Mobility Transistors (HEMT) for power applications. Normally, these devices are on; however, to reduce the static power dissipation and for safety purposes, normally-off devices are preferred. p-GaN gate AlGaN/GaN-on-Si is the leading normally-off transistor architecture with significant commercial traction. Threshold voltage (V_{TH}) instability is reported in these devices during nominal operational OFF state stress [1,2], ON state stress [3–7], and V_{TH} measurements [8–11]. V_{TH} instability is often attributed to the dynamic charge conditions created in the gate stack during operation. For instance, trapping of 2DEG electrons in the AlGaN barrier cause a positive V_{TH} shift and an accumulation or depletion of holes in the p-GaN gate region, cause a negative or positive V_{TH} shift, respectively. Threshold voltage instability remains a serious concern, as a negative V_{TH} shift could lead to a faulty turn-on of the device, and a positive V_{TH} shift could mandate

higher gate drive voltages, alongside causing an increase in reverse conduction voltages, adding to the switching dead time losses. Thus, it is essential to observe whether threshold voltage recovers after an event of V_{TH} instability and understand its recovery dynamics to foresee the aforementioned reliability issues. The reported V_{TH} recovery time measurement methods [10] typically involve a stress pulse at the gate terminal or the drain terminal, followed by a threshold voltage measurement by a full transfer characteristic (I_D-V_G) sweep. However, in these measurement techniques, the additional V_{TH} shift caused by the V_{TH} measurement itself [8] due to the I_D-V_G sweep is not decoupled, making the recovery time measured cumulatively inaccurate. Also, the p-GaN gate HEMT's gate stacks across manufacturers have design variations in gate contact (Ohmic or Schottky) and process variations in terms of active Mg doping (p-GaN doping). These variations across manufacturers induce variations in the trapping/de-trapping processes in the gate stack associated with the V_{TH} shift caused during the I_D-V_G sweep [9]. Thus, the recovery time estimated by the existing techniques involving an I_D-V_G sweep will embed additional V_{TH} shift variations due to the I_D-V_G sweep, and this additional shift varies across manufacturers. Hence, a measurement technique to precisely measure recovery time, eliminating the inconsistencies arising due to the measurement technique, is required. In this work, a V_{TH} recovery time estimation technique based on sensing the channel current prestress and post-stress at a single gate voltage at an optimum time interval is proposed. This technique eliminates the V_{TH} shift caused by the transfer characteristic sweep, which is typically present in the nominal measurement schemes. The ON state-induced V_{TH} instability recovery time is estimated by utilizing this technique, and the effect of stress voltage and stress time on recovery dynamics is understood. Based on the time taken to recover post-instability and the slope of the recovery characteristics, the technique is further used to empirically ascertain the trap location.

2. Experimental Methods

Normally-off lateral AlGaN/GaN-on-Si HEMT devices (650 V, 15 A) based on p-gate technology with a threshold voltage of 1.3 V were used in this study. The devices used are based on TSMC technology [12] with a 60–80 nm thick Mg-doped p-GaN layer, 15–25 nm AlGaN layer, and ~5 um GaN epitaxy layer grown on silicon substrate with an intermediate transition layer (Figure 1). The devices under investigation had a Schottky gate with a threshold voltage of 1.3 V, which, upon gate stress (1–4 V), showed a positive threshold voltage shift, as measured by a double pulse test [7]. The proposed recovery time measurement voltage technique (Figure 2) involves a 'stress pulse' where the gate stress (V_G_stress) and the stress time (T_stress) can be defined. The gate stress is followed by a 'measurement pulse,' which is fixed at a gate voltage (V_G_measure) 10% greater than a V_{TH} with a fixed pulse width (T_meas). T_meas of the 'measurement pulse' is selected to ensure that I_D is sampled precisely without the influence of measurement-induced stress. To estimate T_meas, the drain current (I_D) is sampled over time at a V_G bias of 1.1 $V_{TH,}$ and the time period in which the I_D sampled is stable is chosen as T_meas [8,9]. For the samples under investigation, it was observed that at a V_G bias of 1.1 V_{TH}, I_D reached a stable phase between 100 and 500 µs, interpreted as $I_D$stable-Tzone (Figure 3), beyond which I_D decayed rapidly. Thus, a T_meas of 200 µs was chosen for these samples in this analysis hereafter. The drain terminal (V_D bias) was maintained at 50 mV throughout the course of measurements. The I_D measured post-stress by the measurement pulse after a delay of T_stable is termed 'I_D_recovery'. The I_D measured with no stress pulse by the measurement pulse after a delay of T_stable is termed 'I_D_reference'(Figure 2). The time interval between stress pulse and measurement pulse when I_D_recovery matched I_D_reference was estimated as the recovery time. The time interval was iteratively varied through various times to estimate the recovery time for a given condition. In all the measurements, I_D_recovery was sampled after 100 µs with a measurement pulse of width 200 µs. Keysight B2912A high resolution SMUs were used to realize the measurement schematic involving variable V_G_stress (1.5/2/4 V) levels and fixed V_G_measure (1.1 V_{TH}) pulses. Due to hardware

programming interface limitations, a single SMU cannot be used to generate the stress and recovery pulse at different voltage levels. To overcome this, two Keysight B2912A high-resolution SMUs with a protection Zener diode [13], as shown in Figure 4, were used to realize the recovery measurement setup. The 2 SMUS were synchronized by a N1294A-032 I/O trigger cable and switched as required. The gate terminal was stressed at (V_G stress) 1.5 V–4 V for various time intervals (T_stress) from 500 µs to 100 s by SMU1. The time taken for the depleted 2DEG channel to recover to prestress levels was sensed by I_D sampled in the measurement pulse by SMU2, as shown in Figure 2. Post-stress, depending on the extent of positive (+ve) V_{TH} shift, a drop in I_D (2DEG density in the channel) sampled at V_G_measure by the measurement pulse relative to prestress levels was seen. The V_G_measure was chosen at optimum levels (1.1V_{TH}) to ensure that it was close to V_{TH}.

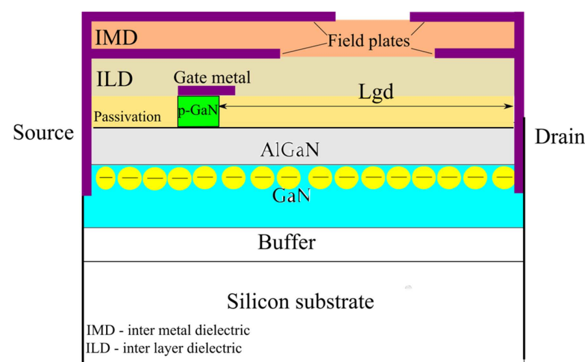


Figure 1. Schematic of the normally-off p-GaN gate AlGaN/GaN-on-Si HEMT.

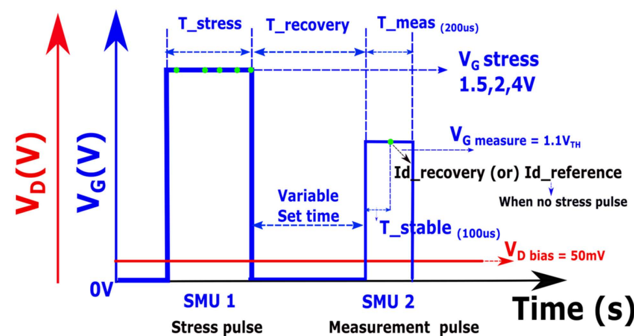


Figure 2. Illustrious gate and drain terminal voltage waveforms demonstrating the threshold voltage recovery time measurement technique.

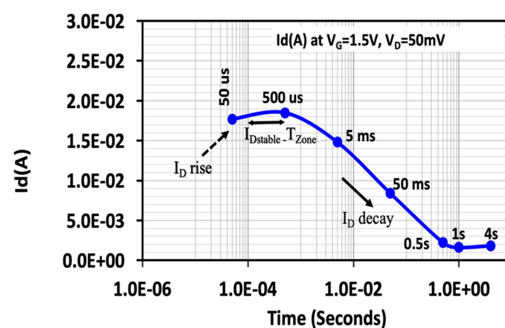


Figure 3. I_D sampling at constant V_G of 1.5 V showing the $I_D$stable-Tzone 100–500 µs where I_D is stable pre-falling I_D and post-rising I_D.

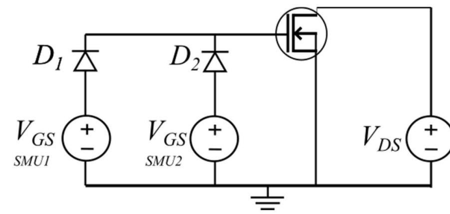


Figure 4. Schematic of the measurement setup where SMU1 and SMU2 are alternatively switched, corresponding to the V_{GS} test waveform shown in Figure 1.

If V_{G}_measure is >> 1.1 $V_{TH,}$ there exists a possibility that the 2DEG channel density is too high relative to the 2DEG changes caused by gate stress, thus making the I_D measured insensitive to stress and recovery. In other words, the I_D sensed would be from the constant regime of I_D-V_G transfer characteristics, as shown in Figure 5, missing the dynamic component caused by stress. Post-stress $I_{D,}$ thus measured by measurement pulse after a recovery time (iteratively changed), is plotted as % normalized with respect to I_D_reference (prestress channel currents measured at V_{GS} = 1.1 V_{TH}, V_{DS} = 50 mV), as shown in Figure 6a–c. For example, after a 2 V, 500 µs stress pulse was administered, followed by a recovery time of 0.05 s; the I_D measured in the measurement pulse was 35% of I_D_reference, as shown in the encircled in Figure 6b. I_D_reference is shown as 100%, and the % recovered with respect to various recovery times is plotted to observe the recovery dynamics. The time when % I_D recovered reaches 100% is representative of the time taken for the V_{TH} to recover post-stress, corresponding to the stress voltage/time. By employing this technique of using a short measurement pulse instead of a complete transfer characteristic sweep, the effect of measurement-induced V_{TH} instability was removed, providing an actual estimate of the recovery time. This recovery time measurement approach, post V_{TH} instability, can be an apt representative replacement for the existing methods. The effect of stress time and stress voltage on V_{TH} recovery dynamics and recovery time are shown in Figure 6a–c, Figure 7, Figure 8a–f, and Figure 9, respectively.

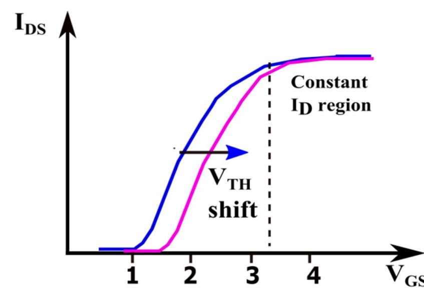


Figure 5. Transfer characteristic showing constant I_D region insensitive to V_{TH} shift caused by V_G stress.

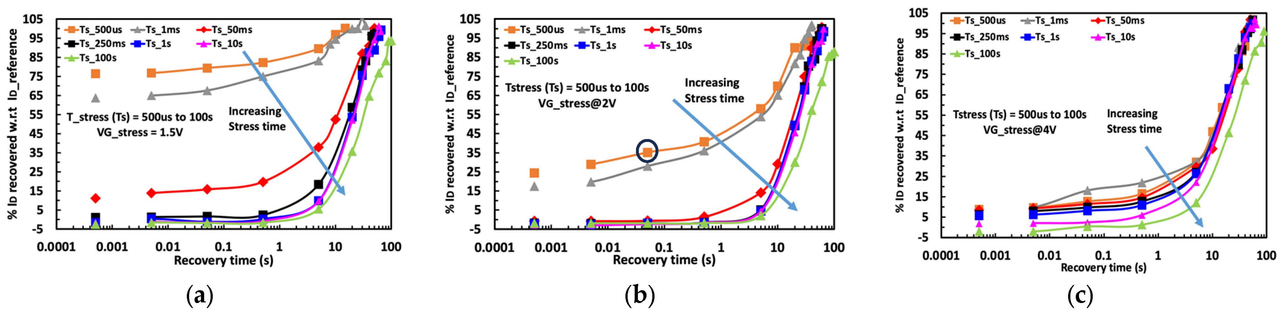


Figure 6. Dynamics of V_{TH} recovery measured by time taken for I_D to recover to prestress levels (I_D-reference) across varying stress times (500 µs to 100 s) for different V_G_stress values of 1.5 V (**a**), 2 V (**b**), and 4 V (**c**).

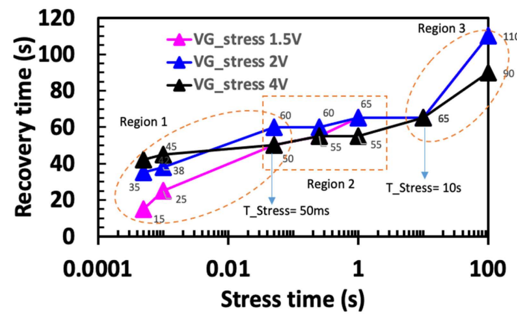
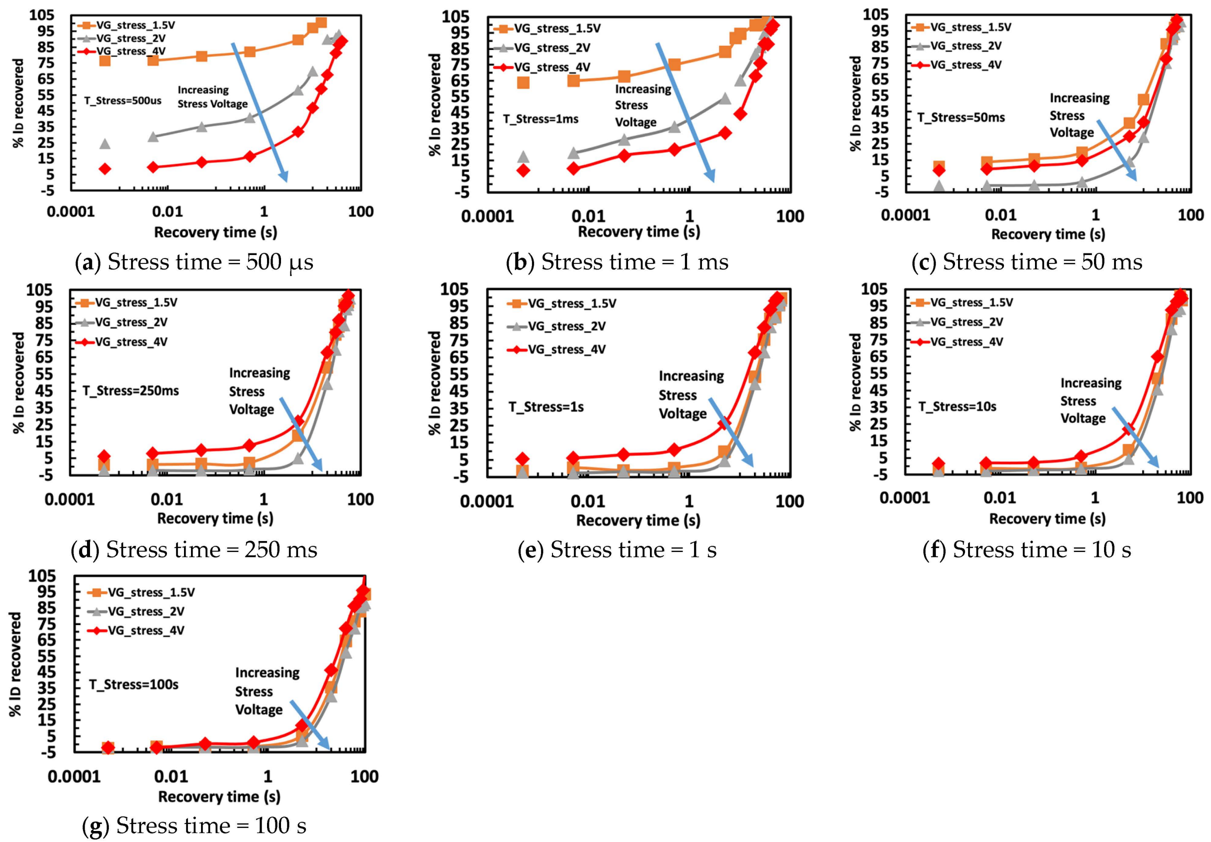


Figure 7. Effect of V_G stress time on the recovery time extracted by the proposed technique illustrating the recovery trends.



(**a**) Stress time = 500 µs (**b**) Stress time = 1 ms (**c**) Stress time = 50 ms

(**d**) Stress time = 250 ms (**e**) Stress time = 1 s (**f**) Stress time = 10 s

(**g**) Stress time = 100 s

Figure 8. Dynamics of V_{TH} recovery measured by time taken for I_D post-stress to recover to prestress levels (I_D-reference, equivalent to 100% I_D recovered in the Y axis) across varying stress voltages (1.5/2/4 V) at various stress times (500 µs—(**a**); 1 ms—(**b**); 50 ms—(**c**); 250 ms—(**d**); 1 s—(**e**); 10 s—(**f**); 100 s—(**g**)).

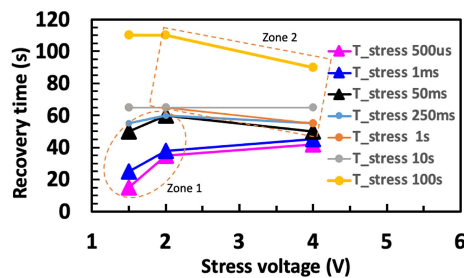


Figure 9. Effect of V_G stress voltage on the recovery time extracted by the proposed technique illustrating the recovery trends.

3. Results and Discussion

3.1. Effect of Stress Time and Stress Voltage on Recovery Time

As stress time increases, a larger decrease in the I_D is observed; this decrease is attributed to the depletion of electrons in 2DEG. With increasing stress time from 500 µs to 50 ms at a V_G_stress of 1.5 V/2 V, the I_D sampled at 1.1 V_{TH} post-stress shows a decreasing trend, and for stress times > 50 ms, the decrease in I_D reaches saturation with no further decrease, as seen in Figure 6a,b. At a higher V_G_stress of 4 V (Figure 6c), even a short stress time of 500 µs causes a strong 2DEG depletion (sensed by I_D sampled at 1.1 V_{TH} post-stress), and with further increasing stress times, the 2DEG depletion saturates. The time taken by the drain current to recover to 100% of its prestress current levels, extracted at 1.1 $V_{TH,}$ is defined as the recovery time (Tr). The recovery process is nonexistent to negligibly small until 0.5s and strongly kickstarts after 5s, and the relative rate of recovery of trapped 2DEG electrons for different stress voltages and stress times is similar, as observed from the slope of recovery curves in Figure 6a–c. With increasing T_stress from 500 µs to 50 ms, the recovery time (Tr) extracted shows an increasing trend, as observed in region 1 of Figure 7. When T_stress is increased from 50 ms to 10 s, the Tr extracted plateaus, and when T_stress is increased from 10 s to 100 s, the Tr extracted shows a strong increasing trend, as observed in regions 2 and 3, respectively (Figure 7). These observed trends agree with the 2DEG depletion trends observed in Figure 6a–c.

As stress voltage increases, a larger decrease in the I_D is observed, revealing the depletion of electrons in 2DEG, as observed in Figure 8a–g. With increasing V_G_stress from 1.5 V to 4 V, for stress times of 500 µs and 1 ms, the I_D sampled at 1.1 V_{TH} post-stress shows an evidently decreasing trend (Figure 8a,b). At a V_G_stress of 1.5 V and 2 V, with stress times ranging from 50 ms to 100 s, it is observed that the I_D sampled at 1.1 V_{TH} post-stress decreases marginally. Upon further increase of V_G_stress to 4 V, with stress times ranging from 50 ms to 100 s, the decrease in I_D starts to saturate and gradually reverse, as seen in Figure 8c–g. At lower stress times of 500 µs and 1 ms, the recovery time increases with stress voltage (Figure 9). At stress times beyond 50 ms, the recovery time is similar for stress voltages of 1.5 V and 2 V and marginally decreases at 4 V (zone 2 of Figure 9). It is to be noted that at a V_G_stress of 4 V, the I_D change due to 2DEG trapping is negligibly small compared to the high channel current, as the device operates in the constant I_D regime of the transfer characteristic (Figure 5). Also, in instances when the I_D has collapsed fully to off-current levels, either by increasing time/voltage to high levels, it does not mean the V_{TH} shift has stopped at that respective stress time and voltage. In summary:

- As stress time increases, recovery time also increases until reaching a critical stress time of 50 ms, beyond which recovery time plateaus until a stress time of 10 s.
- The effect of increasing stress time on recovery time is subdued while the gate is stressed at a higher voltage (4 V).
- As stress voltage increases, recovery time also increases until a critical stress voltage (2 V), beyond which recovery time plateaus.
- The effect of increasing stress voltage on recovery time is subdued while the gate is stressed beyond higher stress times (50 ms).

Thus, based on the trends observed above, there are three T_stress zones: (a) 500 µs to 50 ms, (b) 50 ms to 10 s, and (c) 100 s (marked as region 3 in Figure 7). There are also two V_G_stress groups: (a) V_G_stress = 1.5 V and 2 V, and (b) 4 V (marked as zone 2 in Figure 9).

3.2. Process of 2DEG Trapping and Recovery

The 2DEG depletion causing the positive V_{TH} shift can be explained by the trapping of the 2DEG electrons during the positive gate bias. At the positive gate bias, a vertical field pull can cause trapping of 2DEG electrons at four possible locations/regions: (a) the pGaN/AlGaN interface, (b) the AlGaN bulk, (c) the AlGaN/GaN interface, and (d) the AlGaN/GaN interface and borderline region (some nanometers inside the AlGaN region from the AlGaN/GaN interface is referred as the borderline region). Various capture processes are in play depending on the trapping location, as depicted in Figure 10. For ex-

ample, direct tunneling (DT), trap-assisted tunneling (TAT), and phonon-assisted tunneling (PAT) are processes associated with 2DEG trapping at the AlGaN bulk. Thermal transition and thermionic emission are the capture processes associated with 2DEG trapping at the p-GaN/AlGaN interface. Direct capture, direct capture together with borderline hopping, are the processes associated with 2DEG gettting trapped at the AlGaN/GaN interface and borderline region. The capture time varies depending on the location of traps and the respective processes involved. The stress time or the stress voltage can effectively control how many 2DEG electrons are trapped and the location where they are trapped. However, the trap energy levels, trap density, and their distribution are fixed irrespective of the stress voltage (operational levels) and time. Hence, the recovery time is solely dependent on the emission. The emission time [14] is given by Equation (1)

$$\tau_e = \frac{\exp(E_c - E_T)/\mathrm{KT}}{\sigma_n * v_{th} * N_c} \tag{1}$$

where τ_e is the emission time of the electron, E_c is the conduction band minimum energy level, E_T is the trap energy level, K is the Boltzmann constant, T is the temperature, σ_n is the electron capture cross-section of the trap, v_{th} is the electron thermal velocity, and N_c is the effective density of states in the conduction band. With exponential dependence on trap electron energy level position, the recovery time has a direct exponential dependence on the difference in energy levels between trap energy level, conduction band minimum, and inverse linear dependence on capture cross section and effective density of states. Thus, recovery time and its dynamics can be an effective indication of the trap characteristics.

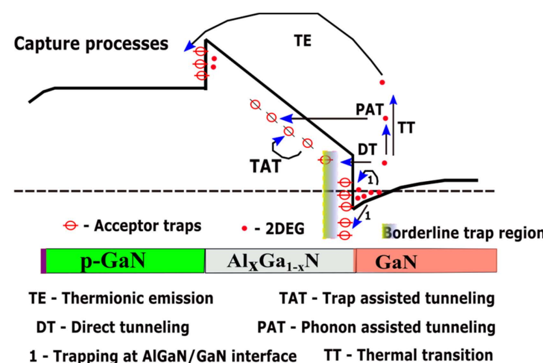


Figure 10. Illustrative viable capture processes by which 2DEG could be trapped due to vertical field pull by +ve gate bias.

3.3. Hypothesis on Trap Location and Recovery Processes

Based on the recovery dynamic shown in Figures 6a–c and 8a–g, it is observed that 90% of the I_D recovery post-stress for all stress times and voltages happens between 5 s and its respective Tr. The recovery process has predominantly similar rates of recovery (slope) in most cases where trap occupation levels are not negligibly small (for stress times > 1 ms), implying similar emission processes. For similar emission processes with similar rates of emission irrespective of V_G_stress voltages and times, the trapping or capture processes should be a simplistic, repetitive process and not significantly altered by voltage/time changes. On the other hand, if trapping/emission processes involve crossing barriers such as AlGaN or tunneling through barriers, they might be affected by stress voltage and times, affecting barrier shape and height. Thus, it is hypothesized that 2DEG getting trapped at the AlGaN/GaN interface is the dominant process relative to the other processes highlighted in Figure 10.

Having empirically hypothesized the trapping location, the trapping processes during stress and emission processes post-stress at the AlGaN/GaN interface, represented in terms of band diagram, are graphically illustrated for V_G_stress values = 1.5 V and 2.0 V. Prestress, the conduction band minima (EC_min) is above the GaN buffer electron

fermi level (eEf_GaN), signifying the normally-off operation; the difference between the EC_reference and the EC_min is the conduction band discontinuity (Ecbd), which remains constant irrespective of stress voltage/time. On application of +ve gate voltage (Time = 0), EC_min moves below eEf_GaN, forming a 2-dimensional quantum confined space holding the 2-dimensional electron gas (2DEG). Over time (stress phase), the 2DEG starts to get trapped at the shallow acceptor traps (ET_shallow) at the AlGaN/GaN interface due to the field pull (processes 1.0 and 1.1, respectively, in Figure 13).

When the stress time increases:

- The number of 2DEG electrons becoming trapped in the ET_shallow level increases until trap levels are fully filled or 2DEG is fully depleted and I_D decays correspondingly, as shown in Figure 11 and in Figure 12 at constant gate bias (1.5/2 V).
- The acceptor trap, after trapping an electron, becomes negatively charged, generating a net negative charge in the AlGaN region, causing EC_min to move up relative to the fermi energy level, representing rapid 2DEG depletion (stress phase in Figure 13).
- When the gate stress voltage increases, 2DEG density increases, and the 2DEG electrons become trapped at the deeper (ET_deep) acceptor trap energy levels (process 1.2 in Figure 13 for V_G_stress values of 2 V; process 1.3 in Figure 14 for V_G_stress values of 4 V).

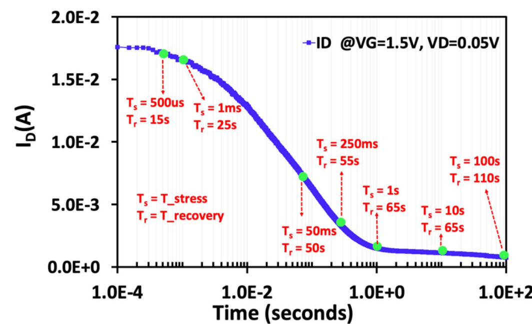


Figure 11. I_D sampled at V_G bias of 1.5 V over various stress times (Ts) and respective recovery times (Tr) extracted by this technique.

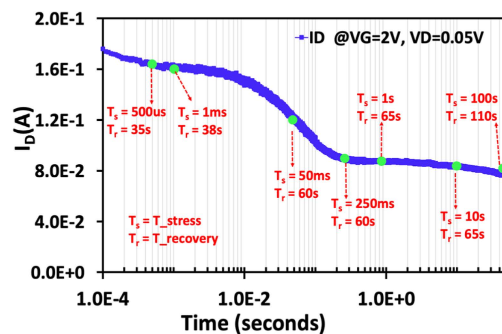


Figure 12. I_D sampled at V_G bias of 2 V over various stress times (Ts) and respective recovery times (Tr) extracted by this technique.

The traps are termed deep/shallow based on their relative position with respect to Ec_min. During the stress phase, 2DEG electrons get trapped at the AlGaN/GaN interface, causing the conduction band maxima at the interface to move up relatively, correlating with the extent of trapping. Once the stress is removed (post-stress at V_G = 0 V), the number of 2DEG electrons trapped during the stress phase determines the extent by which conduction band maxima at the interface moves up relative to Ec_reference, measured as ΔEc. Because of increased 2DEG electron trapping with increasing stress time, $\Delta Ec1(for\ Tstress\ 500\ us) < \Delta Ec2\ (for\ Tstress\ 50\ ms)$, and $\Delta Ec3 < \Delta Ec4$, as shown in Figure 13. During this period, the devices are allowed to relax at room temperature, and

the trapped electrons are emitted from ET_shallow or ET_deep to the triangular quantum well by thermal energy.

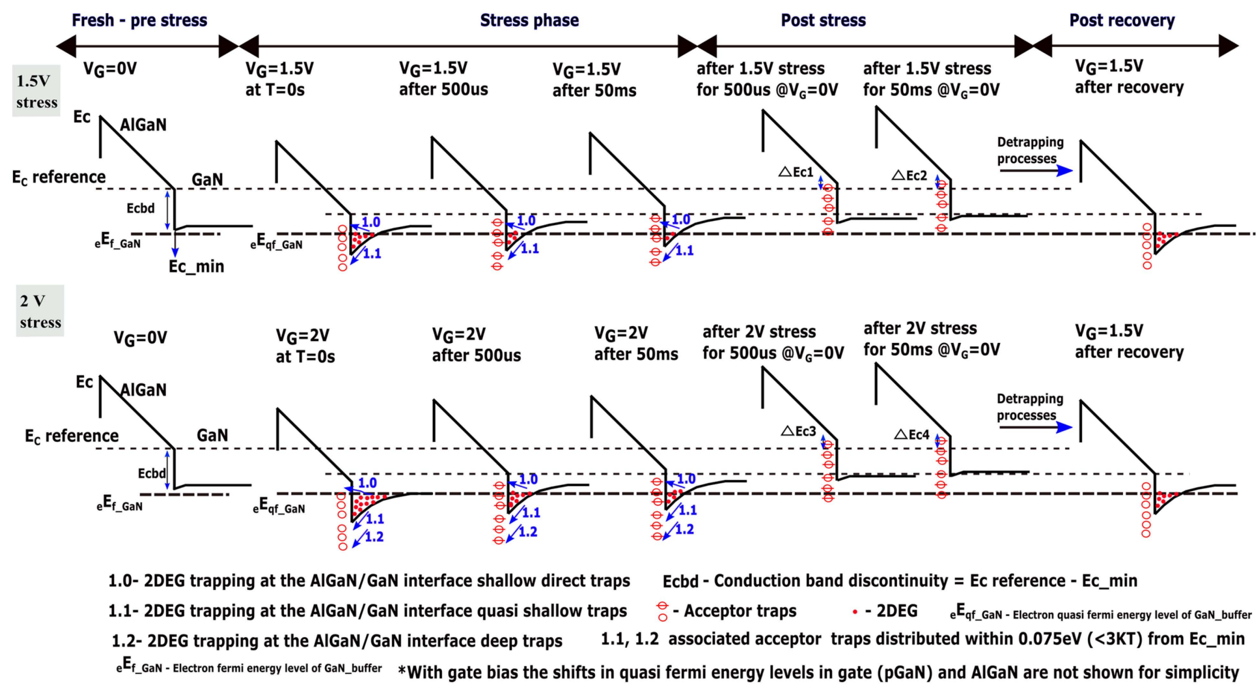


Figure 13. Illustrative schematic showing the AlGaN/GaN interface's conduction band movement relative to prestress Fermi energy level, with increasing durations of stress, post-stress, and post-recovery following a relaxation time of 1.5 V and 2 V stress.

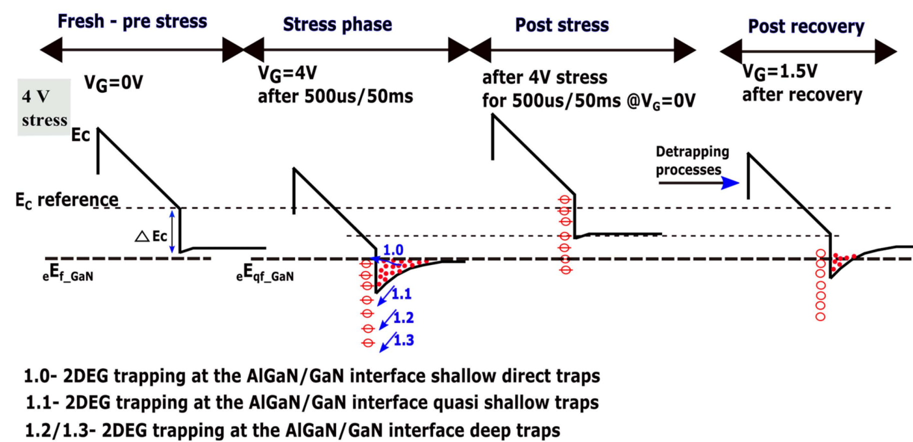


Figure 14. Illustrative schematic showing the AlGaN/GaN interface's conduction band movement relative to the Fermi energy level during prestress, with increasing durations of stress, post-stress, and post-recovery following a relaxation time of 4 V stress.

As the emission time has an exponential dependence on ET-EC, those trapped at ET_deep will take more time to emit, explaining the increase in recovery time with higher stress voltages (zone 1 of Figure 9). However, at higher stress voltages of 4 V, the gate leakage current becomes higher [15], and the injected holes cross the AlGaN barrier by thermionic emission and tunneling (Figure 15), setting a potential counter compensation for the 2DEG trapping, causing net reduced 2DEG trapping explaining the relatively same or slightly shorter recovery times as in V_G_stress of 4 V (zone 2 of Figure 9). It is to be noted that, unlike 1.5/2 V V_G_stress instances, the 2DEG density during 4 V stress, with increasing times, shows negligible change as the I_D at V_G 4 V is in the saturation regime and is not

affected by the V_{TH} shift, as explained earlier in Figure 5. As stress time increases beyond 50 ms (until 10 s), the trap density at the AlGaN/GaN interface, within the thermodynamic reach of 2DEG, starts becoming saturated by trapped electrons, causing constant recovery times (region 2 of Figure 7). At a high-stress time of 100 s, the 2DEG electrons, post-saturating the AlGaN/GaN interfaces, hop to the borderline region traps (2–3 nm from the interface) of AlGaN, leading to higher emission times and thus higher recovery times (as shown in region 3 of Figure 7). Thus, from the dynamic recovery trends and times, we could ascertain that the AlGaN/GaN interface is the predominant trapping site. This recovery time measurement could be extended to understand OFF-state stress-induced 2DEG trapping, as well. Deep Level Transient Spectroscopy (DLTS) in depth profiling mode could be used to determine the traps' exact energy levels and concentration, as well as the traps' density [16,17]. With DLTS, alongside temperature-dependent Arrhenius analysis, the trap location ascertained by the proposed recovery time measurement technique could be verified, which will be a part of future work.

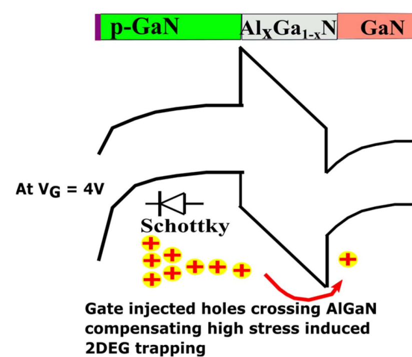


Figure 15. Illustrative band diagram at V_G = 4 V across the gate stack showing gate-injected holes crossing the AlGaN barrier.

4. Conclusions

We have proposed a methodology to measure the recovery time reliably, post gate stress induced threshold voltage instability by decoupling the cumulative effect of measurement induced instability. The effect of stress time and stress voltage on recovery time is studied, and based on the recovery dynamics, the trap location is indicatively ascertained. The dynamics of the trapping process, the subsequent recovery process with changes in stress time, voltage is observed and the correlation to the recovery time trends is made. Further temperature-dependent measurements and TCAD models are being developed as a part of future work.

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