electronics

MDPI

Article

Nonlinear Dynamics in HfO_2/SiO_2-Based Interface Dipole Modulation Field-Effect Transistors for Synaptic Applications

Noriyuki Miyata

National Institute of Advanced Industrial Science and Technology (AIST), Tsukuba 305-8565, Ibaraki, Japan; nori.miyata@aist.go.jp

Abstract: In the pursuit of energy-efficient spiking neural network (SNN) hardware, synaptic devices leveraging emerging memory technologies hold significant promise. This study investigates the application of the recently proposed HfO_2/SiO_2-based interface dipole modulation (IDM) memory for synaptic spike timing-dependent plasticity (STDP) learning. Firstly, through pulse measurements of IDM metal–oxide–semiconductor (MOS) capacitors, we demonstrate that IDM exhibits an inherently nonlinear and near-symmetric response. Secondly, we discuss the drain current response of a field-effect transistor (FET) incorporating a multi-stack IDM structure, revealing its nonlinear and asymmetric pulse response, and suggest that the degree of the asymmetry depends on the modulation current ratio. Thirdly, to emulate synaptic STDP behavior, we implement double-pulse-controlled drain current modulation of IDMFET using a simple bipolar rectangular pulse. Additionally, we propose a double-pulse-controlled synaptic depression that is valuable for optimizing STDP-based unsupervised learning. Integrating the pulse response characteristics of IDMFETs into a two-layer SNN system for synaptic weight updates, we assess training and classification performance on handwritten digits. Our results demonstrate that IDMFET-based synaptic devices can achieve classification accuracy comparable to previously reported simulation-based results.

Keywords: MOSFET; gate dielectrics; interface dipole; neuromorphic; spiking neural network

Citation: Miyata, N. Nonlinear Dynamics in HfO_2/SiO_2-Based Interface Dipole Modulation Field-Effect Transistors for Synaptic Applications. *Electronics* **2024**, *13*, 726. https://doi.org/10.3390/electronics13040726

Academic Editors: Elias Stathatos, Jae-Hyung Jang, Tao Wang, Frédérique Ducroquet, Yi Gu and Hongtao Li

Received: 31 December 2023
Revised: 2 February 2024
Accepted: 7 February 2024
Published: 10 February 2024

1. Introduction

Research on solid/solid interfaces is intricately connected to the evolution of semiconductor devices. Throughout the extensive history of semiconductor devices, substantial progress has been made in understanding the various interfaces that constitute these devices, such as metal/semiconductor, semiconductor/semiconductor, and oxide/semiconductor interfaces. In the development of MOSFETs, the fundamental building blocks of Si large integrated circuits, the interfacial electronic states, especially at the oxide/Si interface in the gate stack structure, are crucial elements influencing device operation and performance. Historically, the discovery of high-quality SiO_2/Si interfaces formed by the thermal oxidation of silicon substrates in around 1960 paved the way for the mass production manufacturing of CMOS integrated circuits [1,2]. In the 2000s, research institutions worldwide actively pursued the development of high-*k* gate dielectrics, accumulating knowledge about gate stacks containing various metal oxides [3,4]. The adoption of HfO_2-based dielectrics in current state-of-the-art MOSFETs is a technological fruition of these research and development efforts [5]. In the 2010s, research on non-volatile memories based on MOSFETs incorporating high-*k* dielectrics experienced a significant surge [6,7]. Ferroelectric field-effect transistor (FeFET) memory, integrating ferroelectric materials into the gate stack, and conventional flash memory with high-*k* dielectrics garnered considerable attention [8,9]. The discovery of ferroelectric HfO_2 in 2021 captured researchers' interest due to its excellent material compatibility with silicon semiconductor technology [10], driving continued active research and development for memory applications [11–14]. A notable

recent research trend in FeFETs, similar to the purpose of this study, is the development of analog memories for neuromorphic applications [15,16].

Research on the dipole layers induced at dielectric/dielectric interfaces has primarily advanced for the purpose of controlling the threshold voltage of high-*k* MOSFETs [17,18]. It has been reported that a small dipole layer is formed at the HfO_2/SiO_2 interface used in this study [19,20]. Interfacial dipole modulation (IDM) memory was conceived based on the studies of such high-*k* gate stack structures, with the objective of inducing MOS threshold voltage shifts similar to FeFETs. The first reported IDM results were observed in a HfO_2/SiO_2 stack structure incorporating a 1 monolayer (ML) of TiO_2, as depicted in Figure 1a [21]. A MOS capacitor with such a stack structure exhibits a high-frequency C-V curve with small hysteresis, as illustrated in Figure 1b. This phenomenon was elucidated by the alteration in the bonding state around the Ti atoms at the SiO_2/HfO_2 interface, causing a change in the potential difference (interfacial dipole) between SiO_2 and HfO_2. Subsequently, hard X-ray photoelectron spectroscopy studies of IDM metal–insulator–metal structures have revealed changes in the Ti oxidation states synchronized with memory operation, supporting the notion that the origin of IDM is the structural change around the interfacial Ti atoms [22]. As IDM operates at amorphous dielectric/dielectric interfaces, it does not necessitate high-temperature crystallization annealing, in contrast to ferroelectric HfO_2, and has been verified even with low-temperature annealing at around 300 °C [23]. Furthermore, as shown in Figure 1c, the modulation operation exhibits a gradual change with respect to the applied voltage. This feature is also thought to originate from atomic-scale disorder at the amorphous dielectric/dielectric interface. The gradual threshold change is anticipated to be beneficial for analog operation in synaptic devices, as discussed later. On the other hand, the modulation range of HfO_2/SiO_2-based IDM is relatively small, up to about 0.33 V [21,23]. To extend the modulation range, a multilayered HfO_2/SiO_2 structure has been proposed. For example, an FET incorporating a multilayered IDM with six TiO_2 modulation layers achieves a threshold voltage shift of over 1 V and a current change of over six orders of magnitude [21]. The pulse response characteristics of IDMFETs have been investigated, demonstrating stable and repetitive modulation. The authors believe that these characteristics make it suitable for use as a synaptic device in spiking neural networks and have conducted detailed measurements. This report presents the pulse response measurement of IDMMOS capacitors, explains the physical origin of their characteristics, and describes the current modulation of IDMFETs to verify their potential as synaptic devices in spiking neural networks.

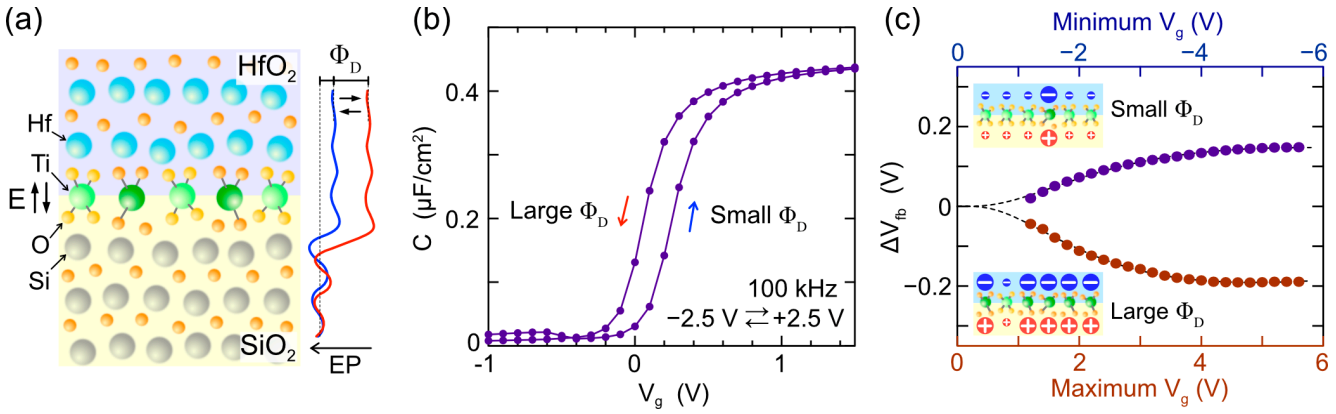

Figure 1. Basis of the interface dipole modulation (IDM) mechanism and MOS capacitor characteristics. (**a**) Proposed IDM mechanism for the HfO_2/SiO_2 interface with an atomically thin TiO_2 modulation layer. (**b**) High-frequency C-V curve of the HfO_2/SiO_2/n-Si IDMMOS capacitor displaying counterclockwise hysteresis. (**c**) Relationship between V_{fb} shift from the initial V_{fb} and the maximum and minimum V_g in C-V measurements.

Energy-efficient neuromorphic computing hardware is a recent hot topic in the electronic memory device research field, and a variety of emerging-memory-based technologies have been proposed [24–26]. In particular, research on analog memory aimed at emulating biological synapses is active, and the realization of highly integrated synaptic devices is expected. One criterion for evaluating synaptic devices is the linearity of synaptic weight update characteristics. For example, in the current mainstream of deep neural networks, good linearity in weight updates is preferred and increased nonlinearity leads to poor learning and inference performance [27,28]. Also, regarding the next generation AI technology, spiking neural networks (SNNs), most studies show that linear weight updates are advantageous [29,30]. However, there is also the possibility of intentionally introducing nonlinear update dynamics to improve the performance of unsupervised SNN learning [31–33]. In SNN systems, as illustrated in Figure 2a, spikes transmitted from presynaptic neurons undergo weighting through synapses before being input into the postsynaptic neuron [34,35]. In post-synaptic neurons, input spikes contribute to the rise in membrane potential, leading to output spikes when the membrane potential reaches a specific threshold according to leaky integrate-and-fire (LIF) dynamics. Spike timing-dependent plasticity (STDP) serves as a fundamental synaptic learning rule, updating synaptic weights based on the temporal difference between pre-synaptic and post-synaptic spikes. Numerous studies have explored STDP learning employing emerging memory devices, with a predominant focus on two-terminal resistive-switching memory due to its benefits in high-density integration [36,37]. Meanwhile, three-terminal memory devices like FET-type memory have garnered attention as synaptic devices capable of achieving concurrent STDP learning within a single device [38–40]. This study aims to achieve concurrent STDP in IDMFETs utilizing a straightforward spike waveform and operation approach. We apply the experimentally observed STDP-like responses of IDMFET to a simple SNN network and assess its suitability for unsupervised SNN learning.

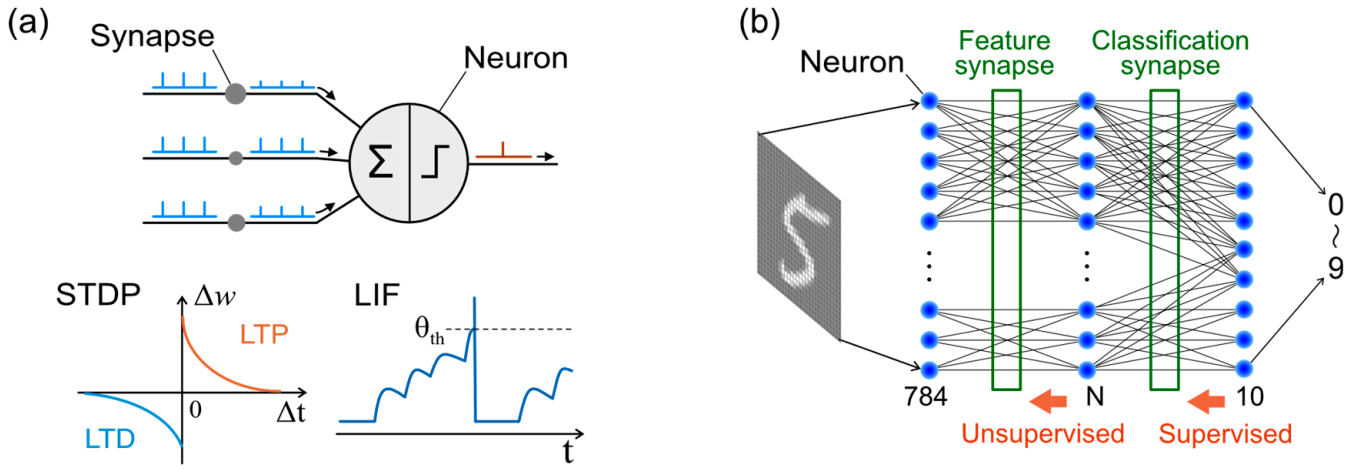

Figure 2. Illustration of the spiking neuron model and network architecture for pattern recognition examined in this study. (**a**) Spike-based neuron model with leaky integrate-and-fire (LIF) dynamics and spike-timing-dependent plasticity (STDP) synaptic learning. (**b**) Network architecture where feature synapses are trained through an unsupervised learning based on the experimentally observed pulse responses of IDMFET.

2. Materials and Methods

2.1. Oxide Deposition and Device Fabrication

The HfO_2, TiO_2, and SiO_2 constituting the IDM stack structure were deposited in the same chamber via the high-vacuum electron-beam (EB) evaporation method [41]. The thicknesses of the HfO_2 and SiO_2 were estimated from the calibrated deposition rates using transmission electron microscopy (TEM) and in situ X-ray photoelectron spectroscopy (XPS, Vacuum Science Instruments, Bad Schwalbach, Germany). The modulation layer of 1-ML

TiO_2 was determined based on in situ XPS measurements of TiO_2 deposition on the Si surface. Following the oxide deposition of the IDM stack, a post-deposition annealing (PDA) process was performed at 400 °C for 30 min in an O_2/Ar (~20%) atmosphere. Subsequently, a 50 nm-thick Ir layer was deposited onto the sample surface to serve as the gate electrode, using an EB deposition method.

A 2-IDMMOS capacitor containing two TiO_2 modulation layers was prepared for pulse response characterization. Using the high-vacuum EB evaporation method, the IDM oxide stack, comprising a 3.5 nm-thick top HfO_2 layer, a 1.8 nm-thick inner SiO_2 layer, a 1.8 nm-thick inner HfO_2 layer, and two TiO_2 modulation layers, was formed on an n-type Si(100) substrate covered with a thermally grown SiO_2 layer approximately 5 nm thick. After the above PDA, Ir gate electrodes with a diameter of 200 μm were fabricated using a stencil mask method.

The IDMFET was fabricated through the following steps [42]. Initially, n^+ source/drain (S/D) regions were formed on a p-type Si(100) substrate using the ion implantation method, followed by the formation of an approximately 10 nm-thick thermally grown SiO_2 layer. After etching the SiO_2 layer to 5 nm using diluted hydrofluoric acid, a multilayered HfO_2/SiO_2 IDM stack, comprising 6 TiO_2 modulation layers, was deposited using the high-vacuum EB evaporation method. This 6-IDM stack is composed of a 3.5 nm-thick top HfO_2 layer, 1.8 nm-thick inner SiO_2 layers, 1.8 nm-thick inner HfO_2 layers, and six TiO_2 modulation layers. After the above PDA, a 50 nm-thick Ir layer was deposited and, subsequently, gate electrode patterns with a gate length of 1 μm and a gate width of 100 μm were formed using lithography and reactive-ion etching.

2.2. Pulse Response Measurements of IDM Devices

The pulse response characteristics of the IDMMOS capacitor were observed through a repeated sequence of a voltage pulse stimulus and a C-V measurement at 1 MHz. Negative voltage pulses to the gate electrode in this experiment failed to generate adequate minority carriers (holes) to create an inversion layer on the Si surface. Consequently, we could not obtain a sufficient oxide electric field compared to positive voltage pulses. To address this limitation, we intentionally generated holes near the Si surface by exposing the sample surface to light [21,23]. In such cases, it becomes imperative to maintain a relatively wide pulse width, considering the hole diffusion process from the electrode-uncovered Si region to the Si region beneath the gate electrodes. In this experiment, a pulse width of 20 msec was employed.

The pulse response measurement of the IDMFET was conducted using a repeated sequence of a voltage pulse stimulus and drain current (I_d) measurements with V_{ds} = 50 mV [21]. For comparison, the DC drain current–gate voltage (I_d-V_g) curves were also measured with V_{ds} = 50 mV. Furthermore, to emulate the synaptic STDP behavior, two voltage waveforms with a time difference were applied to the gate and drain electrodes of the IDMFET. A repeated sequence of this double-pulse-controlled stimulus and I_d measurement was performed. The details of the voltage waveforms are described below.

2.3. SNN Architecture for Pattern Recognition

A simple two-layer feedforward network with 784 neurons in the input layer, N neurons in the hidden layer (where N is a variable), and 10 neurons in the output layer was utilized to perform training and classification tasks on the MNIST handwritten digits dataset [43], as shown in Figure 2b. Spike-based temporal processing optimized for the experimentally observed responses of the IDMFETs was implemented, referencing a computationally efficient simplified model proposed by Iakymchuk et al. [44]. In the input neurons, 28 × 28 pixels with 256 gray levels were transformed into 784 spike trains with a frequency range from 200 Hz to 1.25 kHz. These spikes were then transmitted to the hidden neurons through feature synapses, thereby raising the membrane potentials of the neurons. The hidden neurons operate on a LIF model with dynamic threshold adjustments and a 10 msec refractory period, generating output spikes when their membrane potential

exceeds a certain threshold. Additionally, a winner-take-all (WTA) competitive algorithm was implemented through lateral inhibition in the hidden layer neurons.

The STDP weight update of the feature synapse was performed based on the time difference between the pre-synaptic spike and the post-synaptic spike, with the time delay from post-synaptic spike firing to reaching the synapse set to 80 µs. Furthermore, to stabilize unsupervised learning, an additional weight depression function, independent of the input neuron's frequency and referred to as frequency-independent depression (FID), was introduced for all synapses undergoing STDP. This FID operation simply produces the effect of reducing the synaptic weight distribution. Through the above procedure, the feature synapses acquire characteristics of the input images through unsupervised learning. Additionally, the classification synapses update weights through supervised learning based on STDP to associate the hidden neurons with the output neurons. These synaptic learning processes enable the entire network to function as a pattern classifier. A total of 60,000 MNIST images were used for training feature and classification synapses, and 10,000 images were used for the performance test.

3. Results and Discussion

3.1. Pulse Response of IDM MOS Capacitors

The pulse response characteristic of the IDMMOS capacitor (illustrated in Figure 3a) indicates that the flat-band voltage (V_{fb}) undergoes stable positive and negative shifts in response to the voltage polarity switch every 50 pulses. Here, the V_{fb} shift from the initial V_{fb} (ΔV_{fb}) were plotted. Both positive and negative V_{fb} shifts display obvious nonlinear responses, exhibiting substantial changes immediately after the polarity switch and gradual suppression in the amount of change as the pulse count increases. Utilizing the approximation formula for nonlinear characteristics [45,46], the estimated nonlinear parameter ν for both positive and negative V_{fb} shifts is approximately six, indicating a nearly symmetrical response. The pulse voltage (V_p) dependence illustrated in Figure 3b indicates an increase in modulation amplitude and ν with the rise in V_p, as depicted in Figure 3c. As a result, IDMs exhibit inherently nonlinear and near-symmetric responses and the degree of nonlinearity varies depending on the operating conditions, making it necessary to consider these specific characteristics in synaptic applications.

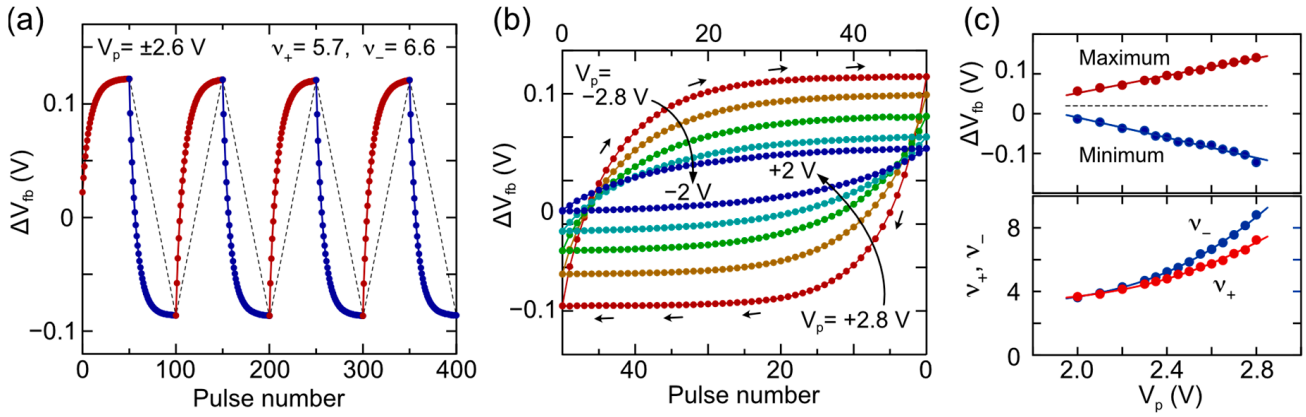

Figure 3. Pulse response of an IDMMOS capacitor with two TiO_2 modulation layers. (**a**) Cyclic characteristics of flat-band voltage (V_{fb}) shifts, showing stable modulation amplitude and nonlinear characteristics. (**b**) Dependence of V_{fb} modulation characteristics on pulse voltage (V_p). (**c**) Impact of V_p on modulated V_{fb} shifts and nonlinear parameters (ν_+ and ν_-).

Next, we delve into the reasons behind the nonlinear response. The V_p-dependent V_{fb} shift in Figure 3b incorporates information about both the interface dipole state and response characteristics, which is useful for analyzing their relationship. ΔV_{fb} on the y-axis corresponds to the strength of the interface dipoles, as shown in Figure 1a. Here, we assumed that the unit dipole switches between two states: large and small. In this scenario,

the maximum V_{fb} shift occurs when all the unit dipoles at the HfO_2/SiO_2 interface switch due to the electric field; under the opposite electric field, the opposite maximum V_{fb} shift occurs when all the unit dipoles switch to the opposite state. Additionally, the maximum modulation width of the 2-IDM structure is 0.66 V, as previously reported. In this context, the ratio of un-switched unit dipoles, that is, switchable unit dipoles, is defined as θ_D. In the following discussion, θ_D was estimated from the experimentally obtained ΔV_{fb} based on the above assumptions. On the other hand, the modulation rate, dV_{fb}/dt (V/sec), can be estimated from the ΔV_{fb} shift per pulse and the oxide electric field E_{ox} (V/cm) can be estimated from the relationship between the ideal C-V curve of the MOS structure and V_p [47]. Consequently, we can establish the relationship between dV_{fb}/dt and E_{ox} as shown in Figure 4a. It is essential to note that even if the switching rate of the unit dipole is constant, the modulation rate varies depending on θ_D. For instance, a change in θ_D from $\theta_D = 0.5$ to $\theta_D = 0.65$ or $\theta_D = 0.35$ predicts the characteristics (I) and (II) in Figure 4a. However, the experimental results indicate more significant changes that cannot be explained by a simple θ_D difference.

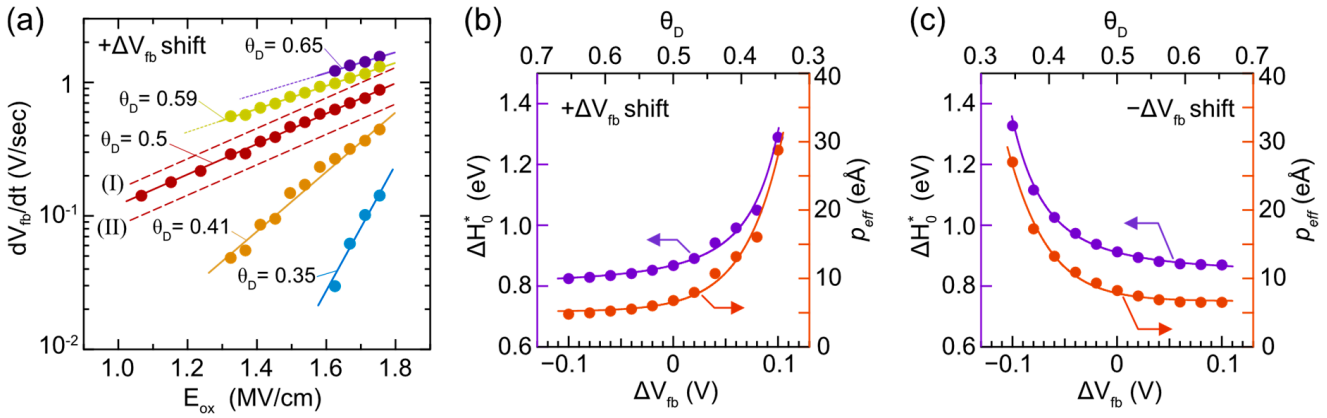

Figure 4. Pulse response characteristics and IDMMOS capacitor and origin of nonlinear response. (**a**) Dependence of the rate of V_{fb} shifts (dV_{fb}/dt) on the ratio of switchable unit dipoles (θ_D) observed for positive V_{fb} shifts. (I) and (II) depict the estimated ideal dV_{fb}/dt for $\theta_D = 0.65$ and 0.35, respectively. (**b**,**c**) θ_D dependence of zero-field effective activation energy (ΔH_0^*) and effective dipole moment (p_{eff}) for positive and negative V_{fb} shifts, respectively.

The experimentally obtained dV_{fb}/dt is considered to be proportional to the number of switchable unit dipoles. Therefore, the following relationship can be predicted: $dV/dt = \Delta V_{max} \cdot k \cdot \theta_D$, where ΔV_{max} is the maximum V_{fb} modulation of 0.66 V and k (s^{-1}) represents the reaction rate associated with the structural change responsible for dipole modulation. As mentioned earlier, IDM originates from alterations in the chemical bond state around the Ti atom. Previous studies have indicated that this phenomenon can be elucidated by the electric-field-induced chemical bond breakage model [21]. In our study, we continue to employ the following equation, based on the bond-breaking model:

$$k = v_0 exp\left(-\frac{\Delta H_0^* - p_{eff}E}{k_B T}\right) \quad (1)$$

where v_0 is the molecular vibrational frequency, typically on the order of ~10^{13} (s^{-1}), and T and k_B are the temperature (K) and Boltzmann's constant, respectively. From these relationships and the experimentally obtained E_{ox} dependence, we can estimate the zero-field activation energy ΔH_0^* (eV) and the effective dipole moment p_{eff} (eÅ) for each θ_D. The θ_D dependence of ΔH_0^* and p_{eff} for positive ΔV_{fb} shifts is summarized in Figure 4b, and the results estimated by the same analysis for negative ΔV_{fb} shifts are shown in Figure 4c. We can find that, for both cases, both ΔH_0^* and p_{eff} increase when θ_D falls below 0.5. Studies on the dielectric breakdown of gate dielectrics have reported that ΔH_0^* and p_{eff} are sensitive

to local bonding configuration [48,49]. In addition, in the previous report on the IDM response, it has been suggested that the observed ΔH_0^* of about 0.7 eV for large θ_D is close to the breakage of the Ti-O bond [21]. Namely, the observed θ_D dependence in this study likely exhibits that the Ti bonding configuration contributing to IDM varies depending on θ_D. Since IDM occurs at an amorphous oxide interface, it is natural that there are variations in the bond length and bond angle in the chemical bonds of interfacial Ti atoms. Therefore, it is reasonable to assume that the initial structural change starts from the bonding with low ΔH_0^*. In addition, there is a possibility that the structural change itself affects approximate bonding, that is, IDM itself leads to structural variations with higher ΔH_0^* values. From the above experimental results and considerations, we conclude that the nonlinearity in the IDM response is an unavoidable feature caused by the amorphous oxide interface.

3.2. Pulse Response of IDMFETs

We can easily predict that converting the threshold voltage (V_{th}) shift induced by the IDM into a change in the channel current of the FET will result in a response characteristic that is different from the IDM response, since the channel current–gate voltage relationship of the FET is not ideally linear, i.e., general I_d-V_g characteristics include at least a linear region and a sub-threshold region [50]. Before describing the synaptic characteristics of the IDMFET, we will briefly discuss the fundamental DC I_d-V_g curve and pulse-induced I_d change. The DC I_d-V_g curves shown in Figure 5a indicate that approximately 1 V hysteresis takes place with a sweeping voltage range of ±4.5 V. To convert the IDM-induced V_{th} shift into I_d change, it is suitable to use the read V_g within this hysteresis range. Here, the sub-threshold swing was estimated to be approximately 100 mV/decade, suggesting that the I_d change caused by a 0.1-V V_{th} shift is expected to be an order of magnitude current change.

The amplitudes of the I_d modulations marked as (I), (II), and (III) in Figure 5a represent the pulse-induced I_d changes observed under different readout V_g voltages and the same pulse conditions. Here, the pulse voltage (V_p) and pulse width (t_p) were set to ±5.4 V and 800 µs, respectively, and the V_p polarity was switched every 300 pulses. The changes in the pulse response characteristics (I), (II), and (III) shown in Figure 5b indicate that the I_d increase and decrease exhibit opposite behavior regarding nonlinearity. As for the I_d increase, (I) exhibits a nonlinear response, (II) approaches a linear response, and (III) shows an inverted nonlinear response, exhibiting that the nonlinear coefficient (ν_+) changes from positive to negative. Regarding the I_d decrease, the nonlinear coefficient (ν_-) is always positive and the nonlinearity becomes stronger in the order of (I), (II), and (III). On the other hand, even with the same read V_g, the nonlinearity changes significantly depending on the pulse voltage V_p (Figure 5c,d). In the lower graph of Figure 5d, we present the ratio of the nonlinear parameters for I_d increase and decrease (ν_+/ν_-) as an indicator of asymmetry. Here, ν_+/ν_- values approaching 1 indicate proximity to symmetric response and smaller V_p values have better symmetry. In summary, the nonlinearity and asymmetry of the IDMFET exhibit complex behavior dependent on the read and pulse conditions. A summary of the ν_+/ν_- ratios measured under various conditions (Figure 5e) shows that the general tendency is that the asymmetry becomes stronger when aiming for a large current ratio (I_{max}/I_{min}). This implies that, simultaneously, the nonlinearity of the I_d decrease becomes stronger.

The above behavior regarding the nonlinearity and asymmetric response can be roughly understood in terms of basic FET operation as follows. We can easily understand that when the I_d modulation is in the linear region or sub-threshold region with a sufficiently small I_{max}/I_{min} ratio, the nonlinear and near-symmetric IDM characteristics are directly reflected in the I_d response, as the I_d dynamics of (I) in Figure 5b show. On the other hand, when I_{max}/I_{min} is large and the device is operating in the sub-threshold region, even if the V_{th} shift is constant, the smaller the current, the smaller the absolute I_d change will be exponentially. In other words, in the characteristic of the I_d increase, the current is insensitive to V_{th} shifts in the initial stage and gradually becomes sensitive, so the nonlinear

characteristics are weakened. Conversely, in the characteristic of the I_d decrease, the current is sensitive to V_{th} shifts in the initial stage and gradually becomes insensitive, so the nonlinearity of FET operation is further superimposed on the nonlinear IDM response. It is easy to predict that a similar effect will occur even when I_{max}/I_{min} is large and the I_d modulation straddles the linear and sub-threshold regions. This emphasized asymmetry can be found in the I_d dynamics in (II) of Figure 5b. As I_{max}/I_{min} increases further, the current becomes more insensitive to V_{th} shifts during the initial stage of I_d increase, resulting in an opposite nonlinear response. This can be seen in the I_d dynamics in (III) of Figure 5b. The ultimate goal of this study is to verify whether the nonlinear and asymmetric IDMFET response can be applied to STDP learning.

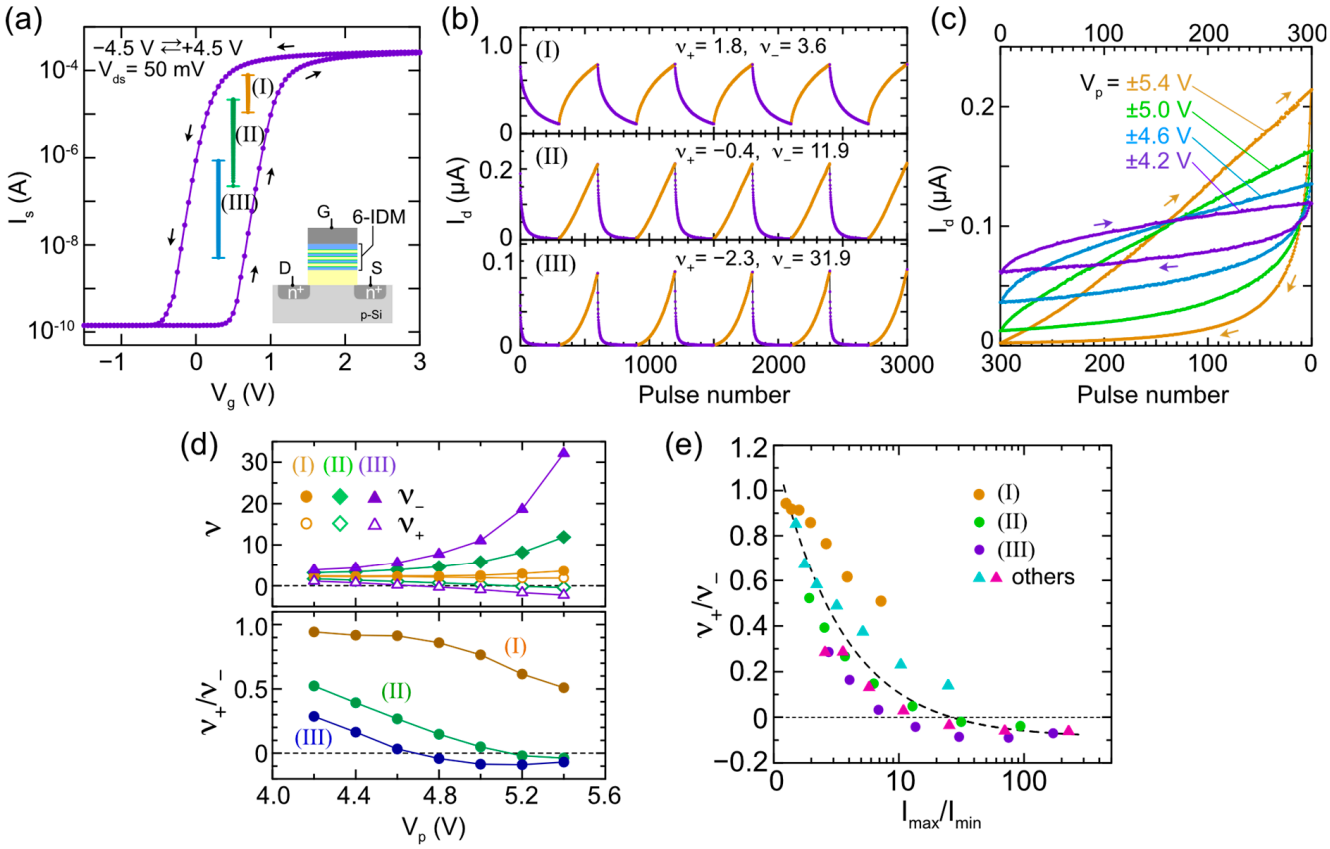

Figure 5. Pulse-induced drain current (I_d) change of IDMFET. (**a**) DC I_d–V_g hysteresis curve and I_d modulation amplitude measured under various read gate voltage conditions (I)–(III). (**b**) Pulse-induced I_d changes with a pulse voltage (V_p) of ±5.4 V. Estimated nonlinear parameters for I_d increase (ν_+) and I_d decrease (ν_-) are shown. (**c**) Impact of V_p on nonlinear asymmetric I_d responses observed under read conditions (II) in (**a**). (**d**) V_p dependence of ν_+, ν_-, and the ratio of ν_+/ν_- under various read conditions. (**e**) Correlation between asymmetric characteristics, ν_+/ν_-, and the ratio of maximum to minimum drain current (I_{max}/I_{min}).

3.3. Double-Pulse-Controlled Synaptic Operation of IDMFETs

To update the I_d of IDMFETs based on the time difference between pre- and post-synaptic spikes, akin to synaptic weight (w) updates in biological STDPs, it is crucial to carefully choose the pre-spike and post-spike waveforms. However, for compatibility with the digital circuits responsible for neuron information processing, it is preferable to avoid complex waveforms as much as possible. We adopted a simple bipolar rectangular waveform, as shown in Figure 6a. Pre- and post-synaptic spikes have waveforms of the same voltages (V_{STDP}) and pulse widths (t_{STDP}) with a time difference Δt. Assuming that a superimposed waveform of pre-synaptic and post-synaptic spikes is applied to the gate stack structure, I_d modulation is expected to depend on Δt, because the period during

which a voltage twice V_{STDP} is applied coincides with Δt. Here, the application period of V_{STDP} also changes, but since IDM has an exponential response to E_{ox}, it is expected that it can be ignored by setting an appropriate V_{STDP}. Figure 6b shows the measurement results in which the sign of Δt alternates every 500 spikes. An increase in I_d is observed at +Δt and a decrease in I_d is observed at −Δt, indicating the expected STDP-like response. This means that synaptic potentiation occurs when a post spike is input after a pre spike is input and synaptic depression occurs at the opposite timing. Furthermore, as Δt approaches 200 μs of t_{STDP}, the amplitude of the I_d modulation increases, which is a characteristic predicted from the above waveform superposition. On the other hand, we also find that STDP operation exhibits obvious nonlinear and asymmetric potentiation/depression properties. For example, at Δt = ±200 μs, the ν_+/ν_- ratio was estimated to be 0.2, showing similar asymmetry to the previously discussed single-pulse IDMFET response.

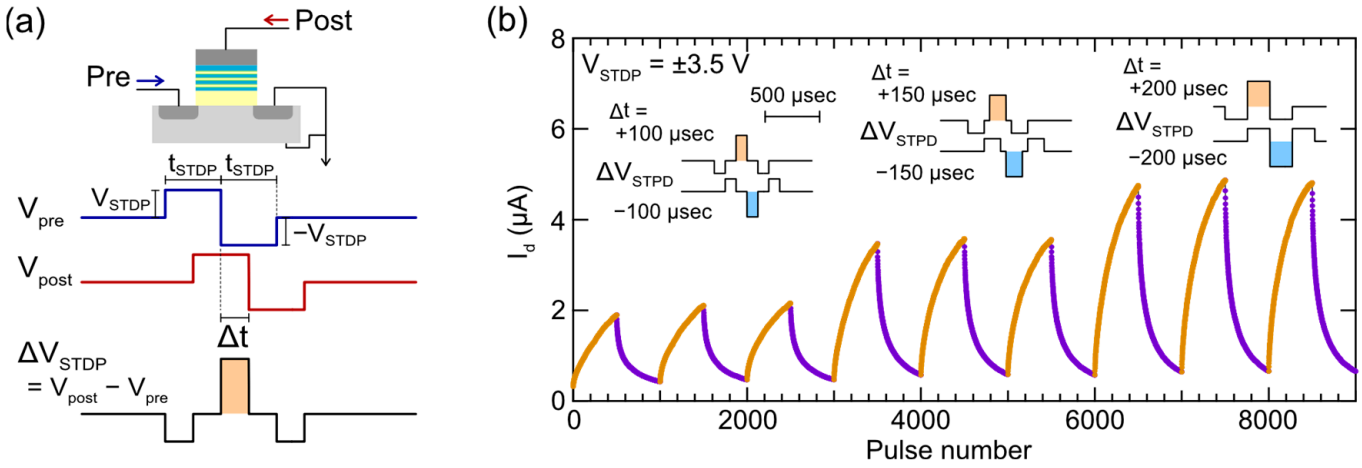

Figure 6. Double-pulse-controlled STDP operation with a bipolar rectangular waveform. (**a**) Concurrent STDP drain current (I_d) modulation scheme of IDMFET based on the interaction of pre- and post-synaptic waveforms. (**b**) Demonstration of STDP-like I_d modulation. I_d changes depend on the spike timing difference (Δt), and nonlinear characteristics persist even during STDP operation. ΔV_{STDP} waveforms, estimated from the difference between the pre- and post-synaptic waveforms for set Δt conditions, are shown as insets.

In order to determine whether the pulse-timing-dependent I_d modulation obtained from the IDMFET can be applied to STDP learning, we need to investigate the different Δt responses acquired within the same I_d range. Therefore, we performed a similar double-pulse measurement that restricted the I_d range, where the sign of Δt is reversed and when I_d exceeds the range of 0.8 to 3.0 μA. Figure 7a presents the comparison of response characteristics for Δt = ±200 μs and ±100 μs. We can see that for the latter, more pulses are required for Δt sign reversal compared to the former. Both results exhibit asymmetric response characteristics and Δt does not approximately affect the ν_+/ν_- ratio. The $\Delta I_d - I_d$ characteristics in Figure 7b can be obtained by converting the measured pulse-induced I_d change into an I_d change for each pulse (ΔI_d). Here, we can find the impact of the asymmetry response. Regarding an I_d increase, a slight ΔI_d value persists even as I_d approaches 3 μA. However, in the case of an I_d decrease, ΔI_d approaches zero more closely as I_d approaches 0.8 μA. The experimentally obtained $\Delta I_d - I_d$ data were fitted with an approximate equation: $\Delta I_d = \alpha(I_d - I_0) + \beta(I_d - I_0)\gamma$, where α, β, γ, and I_0 are constants. In the simulation study described later, the approximate equation of $\Delta I_d - I_d$ data was converted to the synaptic weight, w, in the w range of 0–0.8. The $\Delta w - \Delta t$ characteristics of STDP shown in Figure 7c are the result converted from the experimentally obtained $\Delta I_d - I_d$ data. Here, in the double pulse scheme shown in Figure 6a, when Δt is ±200 μs, which is equal to the pulse width, the time during which the voltage of $\pm 2 \times V_p$ is applied is maximum of 200 μs, and if it deviates from this, the application time becomes shorter

by the maximum one. If it is outside the ±400 µs range or 0 sec, the application time is expected to be zero. The $\Delta w-\Delta t$ characteristics of the experimental results show the expected characteristics, with the maximum modulation at 200 µs and the minimum modulation at −200 µs. On the other hand, the effects of IDMFET nonlinearity and asymmetry are manifested as w-dependent potentiation/depression asymmetry. Under conditions where w is close to zero, potentiation is larger than depression, reaching an equilibrium of potentiation/depression around w = 0.4. As w increases further, depression becomes more prominent. In the following simulations, these nonlinear and asymmetric STDP characteristics are applied to unsupervised pattern learning.

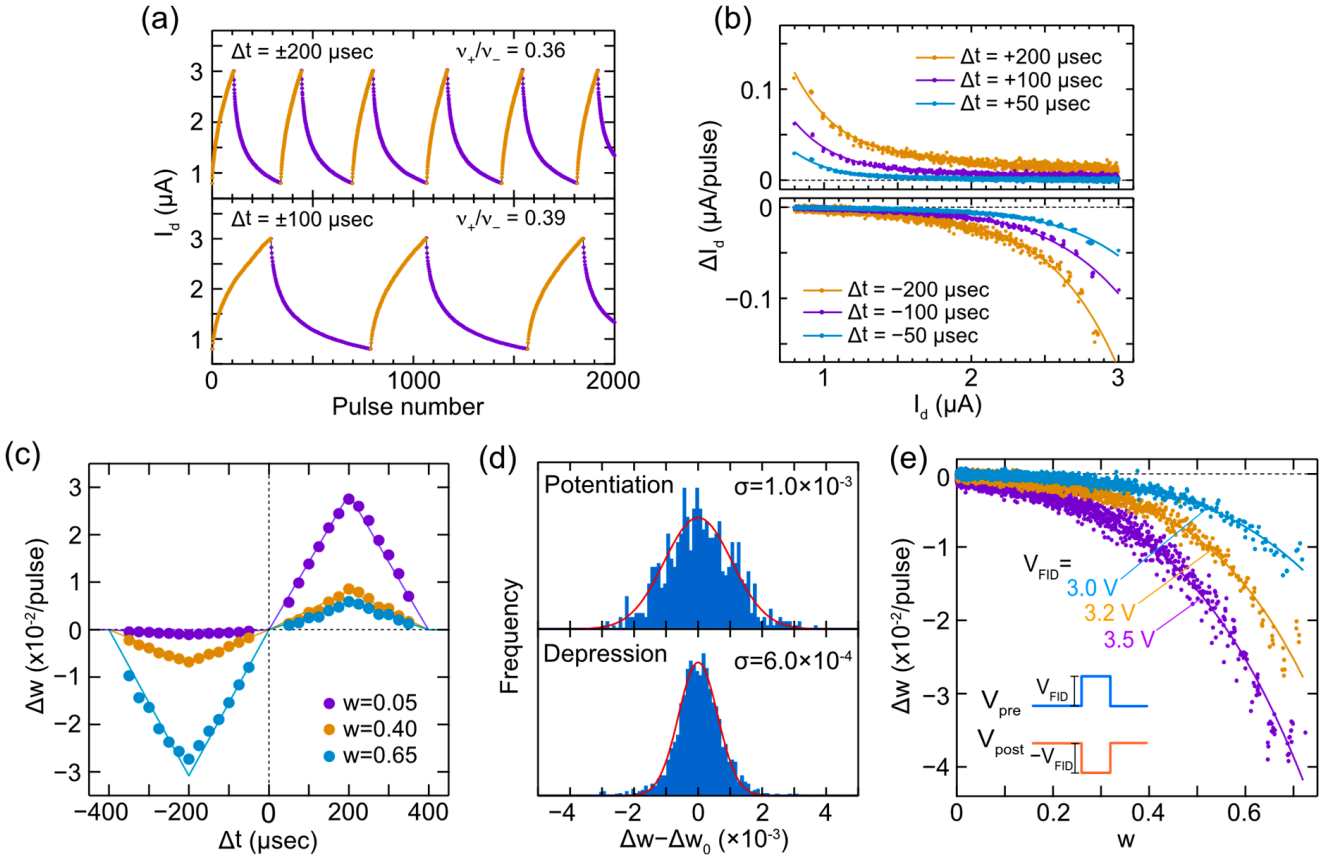

Figure 7. Double-pulse-induced I_d modulation observed within a current range limited to 3.0–0.8 µA. (**a**) Characteristics of STDP I_d modulation observed for Δt = ±200 µs and Δt = ±100 µs. (**b**) ΔI_d-I_d characteristics derived from STDP I_d modulation data, with solid lines representing fitting curves. (**c**) $\Delta w-\Delta t$ characteristics converted from measured ΔI_d-I_d showing nonlinear and asymmetric STDP responses of IDMFET. (**d**) Variation of Δw for STDP response of IDMFET with Δt = ±200 µs from fitting curves (Δw_0). (**e**) $\Delta w-w$ characteristics derived from double-pulse-induced I_d response with unipolar rectangular waveforms, which were utilized as a frequency-independent depression (FID) synaptic update.

On the other hand, an obvious variation is observed in the experimental ΔI_d-I_d data in Figure 7b. Figure 7d illustrates the difference between the approximation curve and measured data across the entire I_d range for the Δt = ±200 µs measurement. The origin of this variation contains the fluctuations of the IDM device itself and measurement system noise. Regarding the former, the fluctuation of the IDM response itself and other V_{th} fluctuations such as the oxide carrier trap may contribute. In the subsequent simulations, STDP incorporating the distribution of observed variations is applied.

In general, SNN learning requires an additional w update function that differs from STDP, for example, to set initial w values and to optimize and adjust the synaptic learning conditions. In this study, an additional w update of FID is applied to adjust the STDP-

based unsupervised learning, as described above. We propose a two-pulse-controlled modulation, as shown in the inset of Figure 7e, which is highly compatible with our STDP operation. Positive and negative voltage pulses, serving as pre- and post-synaptic spikes, are inputted into the IDMFET, inducing the w depression as shown in Figure 7e. The depression effect becomes stronger with the increase in pulse voltage (V_{FID}) across all w ranges. This depression characteristic is incorporated into SNN simulations using the same approximate equation as the STDP characteristics.

3.4. Unsupervised Synaptic Learning Based on IDMFET Characteristics

First, let us examine how unsupervised learning, combining STDP and FID, operates using a network with N = 100 as an example. In this simulation, when a hidden layer neuron fires, the synapses connected to it are updated by STDP and, subsequently, FID is applied to all synapses that underwent STDP (100% FID). For STDP, we utilized the approximate curve obtained from measurements at V_{STDP} = 3.5 V, and for FID, the approximate curve with V_{FID} varied in the range of 3.15 to 3.5 V was employed. Random variations from the distributions estimated by the measurements were incorporated into both STDP and FID. The training dynamics in Figure 8a show the average test accuracy over 10 training/classification cycles, with the shaded area indicating the spread between the maximum and minimum values. In comparison to the result at V_{FID} = 3.2 V, a higher V_{FID} of 3.5 V reaches maximum accuracy faster but subsequently experiences more significant accuracy degradation and fluctuates. Here, the number of training images required to reach 90% of the maximum average accuracy is defined as learning efficiency (η). Although V_{FID} does not significantly affect the maximum accuracy (Figure 8b), a noticeably larger V_{FID} is advantageous for learning efficiency (Figure 8c). This is presumed to be due to a larger V_{FID} enhancing the WTA effect, suppressing the probability of overlapping different digit patterns. However, as V_{FID} increases, the robustness deteriorates after reaching the maximum accuracy, as shown in Figure 8a, suggesting that a large V_{FID} degrades the information of the pattern once learned. Based on the characteristics of the IDMFET obtained in this experiment, a V_{FID} of around 3.2 V is considered a balanced and favorable condition.

From the perspective of reducing calculation costs, it is advantageous to minimize the number of FIDs. Figure 8a illustrates the training dynamics of randomly inducing FID pulses with a 50% probability, demonstrating that both the maximum accuracy and learning efficiency are degraded compared to those of the 100% FID. As depicted in Figure 8b,c, no clear benefit was found from the results of V_{FID} dependence either. We also investigated various FID probabilities and concluded that FID is always required after STDP. This result suggests that FID is effective for properly operating WTA and accumulating training pattern information in appropriate synapses. It is worth mentioning that previously reported studies on STDP-based unsupervised learning did not incorporate additional pulses such as FID [31–33,36–40]. This difference is presumed to be due to the difference in spike waveforms. Generally, more complex spike waveforms are employed to balance potentiation and depression during STDP, for example, spike waveforms include triangle waves and different positive/negative shapes, voltages, and widths. In this study, emphasis was placed on the simplicity of spike waveforms and concurrent STDP learning. An important result of this study is that we were able to achieve efficient unsupervised learning by combining additional FIDs within these constraints.

Next, we briefly mention the impact of the variation of IDMFETs. The training and classification calculation without the variation was also performed, but there are no significant differences in classification accuracy and learning efficiency (Figure 8b,c). We performed similar calculations with a wider distribution than the experimentally observed variation of IDMFETs and found a decline in learning performance. For example, if the variation is 10 times wider than that of the IDMFETs, the maximum accuracy drops to 70%. This means that whereas the current level of variation is acceptable, devices with excessive variation should be treated with caution.

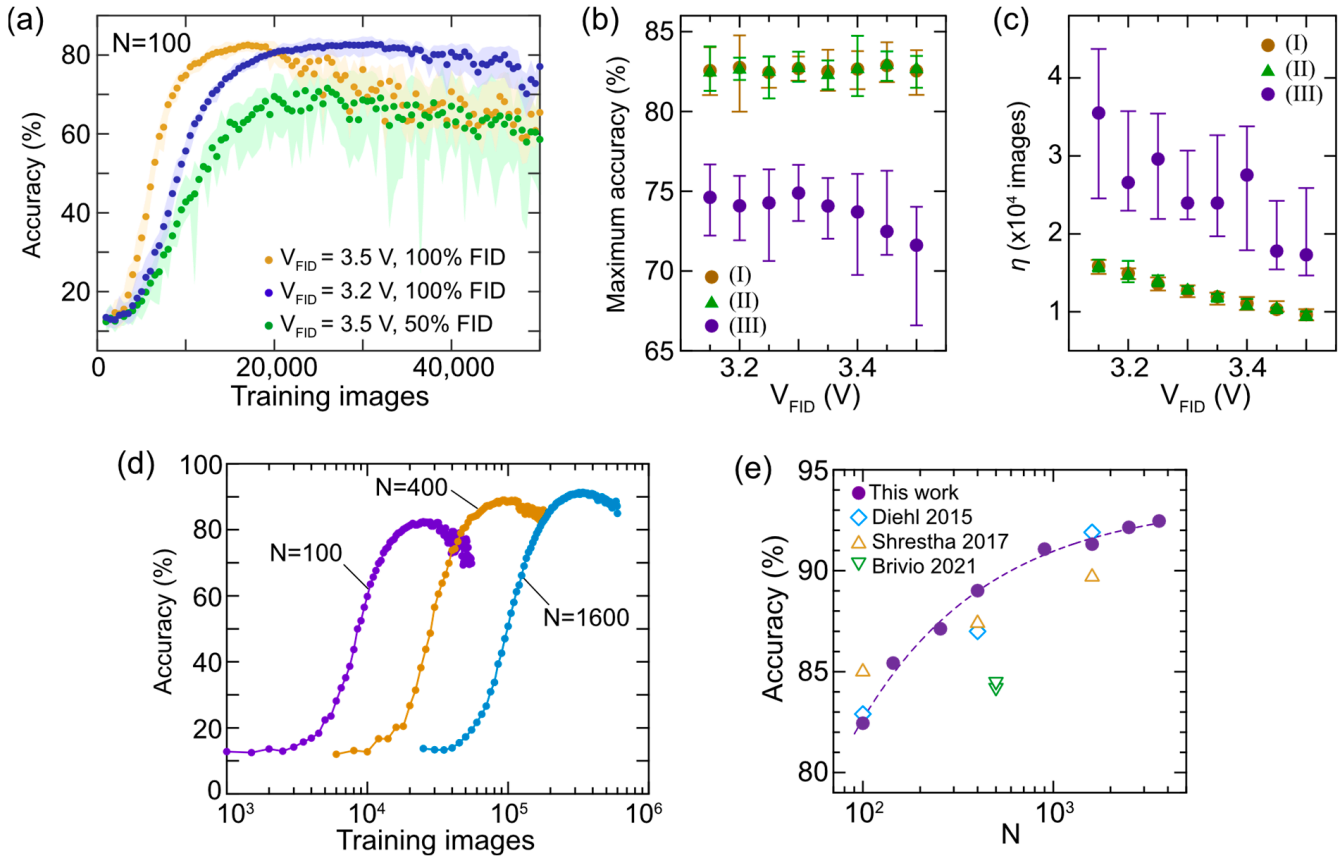

Figure 8. Demonstration of SNN pattern recognition using IDMFET-based STDP and FID synaptic updates. (**a**) Simulated training dynamics for N = 100 hidden neurons. Comparison of 100% FID spike probability conditions with V_{FID} = 3.5 V and 3.2 V. Additionally, the 50% FID spike probability condition with V_{FID} = 3.5 V is presented. (**b**) Impact of V_{FID} on maximum accuracy. (I) and (II) show the results for the 100% FID spike probability condition with and without variations in the IDMFET response, respectively, and (III) shows the results for the 50% FID spike probability condition. (**c**) V_{FID} dependence of learning efficiency (η), where η is defined as the number of training images reaching 90% of the maximum accuracy. (**d**) Training dynamics performed for different *n* networks. (**e**) Dependence of accuracy on *n*, including relevant references (refs. [31–33]) for comparison.

Finally, let us discuss the impact of the feature neuron size. Figure 8e illustrates the training dynamics for different values of *n*, calculated at V_{FID} = 3.25 V. Increasing *n* results in a decrease in learning efficiency due to the increased number of synapses to be learned, where we found a proportional relationship of $\eta = 68 \times n$. On the other hand, increasing *n* can improve classification accuracy, as shown in Figure 8e, in which the previously reported accuracy data deduced by similar networks with STDP-based unsupervised learning were compared [31–33]. It is important to note that previous studies were not related to the device characteristics or are not based on the actual device dynamics. It is evident that even with the STDP characteristics of the IDMFET, introducing suitable FID operations can achieve accuracy equivalent to conventional SNN. Based on these results, IDMFET is considered a promising candidate as a synaptic device for unsupervised SNN learning. Particularly noteworthy is the fact that, in typical SNN systems, the number of synapses is orders of magnitude larger than that of neurons; therefore, the implementation of high-density synaptic devices using IDMFETs is expected to be highly effective. Additionally, it is expected that not only IDMFETs but also other three-terminal devices with similar nonlinear response characteristics can be applicable to unsupervised SNN learning; for example, ferroelectric HfO_2 FeFETs and flash memory devices are promising candidates [15,16,38]. Achieving high-performance integrated synaptic devices based on these Si-based FETs,

including IDMFETs, requires a meticulous investigation of the effects of device scaling, endurance, and reliability during STDP operation, among other considerations. Furthermore, nonlinear responses are frequently observed in non-Si-based three-terminal memory devices, including two-dimensional materials, organic materials, and so on [39,40,51,52]. We expect that such emerging devices can be extended to unsupervised learning, following a similar approach to the one adopted in this study.

4. Conclusions

The pulse response characteristics of HfO_2/SiO_2-based IDM devices were investigated in detail, with the aim of applying them to synaptic STDP learning in SNN systems. The pulse measurements of IDM MOS capacitors reveal that IDM has an essentially nonlinear and near-symmetric response. The cause of the nonlinearity was presumed to be due to a variety of Ti-O chemical bonding states at the HfO_2/SiO_2 interface. The IDMFETs exhibit nonlinear and asymmetric dynamics of pulse-induced I_d modulation that are associated with the superimposition of an inherent nonlinear and near-symmetric IDM response and FET operation characteristics. STDP-like spike-timing-dependent double-pulse-controlled I_d modulation of IDMFETs can be demonstrated, showing nonlinear and asymmetric weight update dynamics. We propose a timing-independent double-pulse-controlled I_d depression of IDMFETs as an additional FID weight update for SNN to optimize unsupervised STDP learning. The training and classification of handwritten digits with a two-layer SNN, leveraging the experimentally observed STDP and FID characteristics, reveals the effectiveness of IDMFET synaptic devices for unsupervised learning in SNNs.

Funding: This work was supported by JSPS KAKENHI, grant numbers 16H02335 and 19H02178.

Data Availability Statement: Data are contained within the article.

Acknowledgments: Part of the device fabrication was conducted at the AIST Nano-Processing Facility (AIST-NPF). The author would like to thank the members of the ULVAC-AIST joint research project for valuable discussions and H. Nohira of Tokyo City University for hard X-ray photoelectron spectroscopy measurements.

Conflicts of Interest: The author declares no conflicts of interest.

References

1. Kahng, D.; Atalla, M.M. Silicon-silicon dioxide field induced surface devices. In Proceedings of the IRE-AIEE Solid State Device Research Conference, Carnegie Institute of Technology, Pittsburgh, PA, USA, 13–15 June 1960.
2. Moore, G.E. Cramming More Components onto Integrated Circuits. *Electronics* **1965**, *38*, 114–117. [CrossRef]
3. Robertson, J.; Wallace, R.M. High-k materials and metal gates for CMOS applications. *Mater. Sci. Eng.* **2015**, *88*, 1–41. [CrossRef]
4. Choi, J.; Mao, Y.; Chang, J. Development of hafnium based high-k materials-A review. *Mater. Sci. Eng. R Rep.* **2011**, *72*, 97–136. [CrossRef]
5. Radamson, H.H.; Zhu, H.; Wu, Z.; He, X.; Lin, H.; Liu, J.; Xiang, J.; Kong, Z.; Xiong, W.; Li, J.; et al. State of the Art and Future Perspectives in Advanced CMOS Technology. *Nanomaterials* **2020**, *10*, 1555. [CrossRef]
6. Zhao, C.; Zhao, C.-Z.; Taylor, S.; Chalker, P.-R. Review on non-volatile memory with high-k dielectrics: Flash for generation beyond 32 nm. *Materials* **2014**, *7*, 5117–5145. [CrossRef]
7. Lu, C.-Y.; Hsieh, K.-Y.; Liu, R. Future challenges of flash memory technologies. *Microelectron. Eng.* **2009**, *86*, 283–286. [CrossRef]
8. Miller, S.L.; McWhorter, P.J. Physics of the ferroelectric nonvolatile memory field effect transistor. *J. Appl. Phys.* **1992**, *72*, 5999–6010. [CrossRef]
9. Tokumitsu, E.; Nakamura, R.; Ishiwara, H. Nonvolatile memory operations of metal-ferroelectric-insulator-semiconductor (MFIS) FETs using PLZT/STO/Si(100) structures. *IEEE Electron Device Lett.* **1997**, *18*, 160–162. [CrossRef]
10. Böscke, T.S.; Müller, J.; Bräuhaus, D.; Schröder, U.; Böttger, U. Ferroelectricity in hafnium oxide thin films. *Appl. Phys. Lett.* **2011**, *99*, 102903. [CrossRef]
11. Park, M.H.; Lee, Y.H.; Mikolajick, T.; Schroeder, U.; Hwang, C.S. Review and perspective on ferroelectric HfO_2-based thin films for memory applications. *MRS Commun.* **2018**, *8*, 795–808. [CrossRef]
12. Schroeder, U.; Park, M.H.; Mikolajick, T.; Hwang, C.S. The fundamentals and applications of ferroelectric HfO_2. *Nat. Rev. Mater.* **2022**, *7*, 653–669. [CrossRef]

13. Trentzsch, M.; Flachowsky, S.; Paul, J.; Reimer, B.; Utess, D.; Jansen, S.; Mulaosmanovic, H.; Müller, S.; Slesazeck, S.; Ocker, J.; et al. A 28 nm HKMG super low power embedded NVM technology based on ferroelectric FETs. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016; pp. 11.5.1–11.5.4.
14. Mulaosmanovic, H.; Breyer, E.T.; Dünkel, S.; Beyer, S.; Mikolajick, T.; Slesazeck, S. Ferroelectric field-effect transistors based on HfO2: A review. *Nanotechnology* **2021**, *32*, 502002. [CrossRef] [PubMed]
15. Dutta, S.; Schafer, C.; Gomez, J.; Ni, K.; Joshi, S.; Datta, S. Supervised Learning in All FeFET-Based Spiking Neural Network: Opportunities and Challenges. *Front. Neurosci.* **2020**, *14*, 634. [CrossRef] [PubMed]
16. Yu, S.; Hur, J.; Luo, Y.-C.; Shim, W.; Choe, G.; Wang, P. Ferroelectric HfO_2-based synaptic devices: Recent trends and prospects. *Semicond. Sci. Technol.* **2021**, *36*, 104001. [CrossRef]
17. Lin, L.; Robertson, J. Atomic mechanism of electric dipole formed at high-K: SiO_2 interface. *J. Appl. Phys.* **2011**, *109*, 094502. [CrossRef]
18. Iwai, H.; Toriumi, A.; Misra, D. High Dielectric Constant Materials for Nanoscale Devices and Beyond. *Electrochem. Soc. Interface* **2017**, *26*, 77–81. [CrossRef]
19. Kita, K.; Toriumi, A. Origin of electric dipoles formed at high- interface. *Appl. Phys. Lett.* **2009**, *94*, 132902. [CrossRef]
20. Abe, Y.; Miyata, N.; Shiraki, Y.; Yasuda, T. Dipole formation at direct-contact HfO_2/Si interface. *Appl. Phys. Lett.* **2007**, *90*, 172906. [CrossRef]
21. Miyata, N. Electric-field-controlled interface dipole modulation for Si-based memory devices. *Sci. Rep.* **2018**, *8*, 8486. [CrossRef] [PubMed]
22. Kirihara, Y.; Tsujiguchi, R.; Ito, S.; Yasui, A.; Miyata, N.; Nohira, H. Using hard X-ray photoelectron spectroscopy to study a SiO_2/HfO_2-based interface dipole modulation stack embedded in a metal–insulator-metal structure. *Appl. Phys. Express* **2022**, *15*, 111003. [CrossRef]
23. Miyata, N. Low temperature preparation of HfO_2/SiO_2 stack structure for interface dipole modulation. *Appl. Phys. Lett.* **2018**, *113*, 251601. [CrossRef]
24. Roy, K.; Jaiswal, A.; Panda, P. Towards spike-based machine intelligence with neuromorphic computing. *Nature* **2019**, *575*, 607–617. [CrossRef] [PubMed]
25. Ielmini, D.; Wang, Z.; Liu, Y. Brain-inspired computing via memory device physics. *APL Mater.* **2021**, *9*, 050702. [CrossRef]
26. Hasler, J.; Marr, H. Finding a roadmap to achieve large neuromorphic hardware systems. *Front. Comput. Neurosci.* **2013**, *7*, 118. [CrossRef] [PubMed]
27. Pan, W.-Q.; Chen, J.; Kuang, R.; Li, Y.; He, Y.-H.; Feng, G.-R.; Duan, N.; Chang, T.C.; Miao, X.S. Strategies to Improve the Accuracy of Memristor-Based Convolutional Neural Networks. *IEEE Trans. Electron. Devices* **2020**, *67*, 895–901. [CrossRef]
28. Aabrar, K.A.; Gomez, J.; Kirtania, S.G.; Jose, M.S.; Luo, Y.; Ravikumar, P.G.; Ravindran, P.V.; Ye, H.; Banerjee, S.; Dutta, S. BEOL compatible superlattice FerroFET-based high precision analog weight cell with superior linearity and symmetry. In Proceedings of the 2021 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2021; pp. 19.6.1–19.6.4.
29. Nandakumar, S.R.; Boybat, I.; Le Gallo, M.; Eleftheriou, E.; Sebastian, A.; Rajendran, B. Experimental Demonstration of Supervised Learning in Spiking neural networks with phase-change Memory Synapses. *Sci. Rep.* **2020**, *10*, 8080. [CrossRef] [PubMed]
30. Yang, S.-T.; Li, X.-Y.; Yu, T.-L.; Wang, J.; Fang, H.; Nie, F.; He, B.; Zhao, L.; Lü, W.-M.; Yan, S.-S.; et al. High-Performance Neuromorphic Computing Based on Ferroelectric Synapses with Excellent Conductance Linearity and Symmetry. *Adv. Funct. Mater.* **2022**, *32*, 2202366. [CrossRef]
31. Diehl, P.U.; Cook, M. Unsupervised learning of digit recognition using spike-timing-dependent plasticity. *Front. Comput. Neurosci.* **2015**, *9*, 99. [CrossRef]
32. Shrestha, A.; Ahmed, K.; Wang, Y.; Qiu, Q. Stable spike-timing dependent plasticity rule for multilayer unsupervised and supervised learning. In Proceedings of the International Joint Conference on Neural Networks (IJCNN), Anchorage, AK, USA, 14–19 May 2017; pp. 1999–2006.
33. Brivio, S.; Ly, D.R.B.; Vianello, E.; Spiga, S. Non-linear Memristive Synaptic Dynamics for Efficient Unsupervised Learning in Spiking Neural Networks. *Front. Neurosci.* **2021**, *15*, 580909. [CrossRef]
34. Izhikevich, E. Simple model of Spiking Neurons. *IEEE Trans. Neural Netw.* **2003**, *14*, 1569–1572. [CrossRef]
35. Yamazaki, K.; Vo-Ho, V.K.; Bulsara, D.; Le, N. Spiking neural networks and their applications: A Review. *Brain Sci.* **2022**, *12*, 863. [CrossRef] [PubMed]
36. Wang, W.; Pedretti, G.; Milo, V.; Carboni, R.; Calderoni, A.; Ramaswamy, N.; Spinelli, A.S.; Ielmini, D. Learning of spatiotemporal patterns in a spiking neural network with resistive switching synapses. *Sci. Adv.* **2018**, *4*, eaat4752. [CrossRef] [PubMed]
37. Saïghi, S.; Mayr, C.G.; Serranogotarredona, T.; Schmidt, H.; Lecerf, G.; Tomas, J.; Grollier, J.; Boyn, S.; Vincent, A.F.; Querlioz, D.; et al. Plasticity in memristive devices for spiking neural networks. *Front. Neurosci.* **2015**, *9*, 51. [CrossRef] [PubMed]
38. Kim, C.-H.; Lee, S.; Woo, S.Y.; Kang, W.-M.; Lim, S.; Bae, J.-H.; Kim, J.; Lee, J.-H. Demonstration of unsupervised learning with spike-timing-dependent plasticity using a TFT-type NOR Flash memory array. *IEEE Trans. Electron Devices* **2018**, *65*, 1774–1780. [CrossRef]
39. Kaneko, Y.; Nishitani, Y.; Ueda, M. Ferroelectric artificial synapses for recognition of a multishaded image. *IEEE Trans. Electron Devices* **2014**, *61*, 2827–2828. [CrossRef]
40. Han, H.; Yu, H.; Wei, H.; Gong, J.; Xu, W. Recent Progress in Three-Terminal Artificial Synapses: From Device to System. *Small* **2019**, *15*, 1900695. [CrossRef] [PubMed]
41. Miyata, N. Study of Direct-Contact HfO_2/Si Interfaces. *Materials* **2012**, *5*, 512–527. [CrossRef] [PubMed]

42. Miyata, N.; Ishii1, H.; Itatani, T.; Yasuda, T. Electron Mobility Degradation and Interface Dipole Formation in Direct-Contact HfO_2/Si Metal–Oxide–Semiconductor Field-Effect Transistors. *Appl. Phys. Express* **2011**, *4*, 101101. [CrossRef]
43. Lécun, Y.; Bottou, L.; Bengio, Y.; Haffner, P. Gradient-based learning applied to document recognition. *Proc. IEEE* **1998**, *86*, 2278–2324. [CrossRef]
44. Iakymchuk, T.; Rosado-Muñoz, A.; Guerrero-Martínez, J.F.; Bataller-Mompeán, M.; Francés-Víllora, J.V. Simplified spiking neural network architecture and STDP learning algorithm applied to image classification. *EURASIP J. Image Video Process.* **2015**, *4*, 1–11. [CrossRef]
45. Agarwal, S.; Plimpton, S.J.; Hughart, D.R.; Hsia, A.H.; Richter, I.; Cox, J.A.; James, C.D.; Marinella, M.J. Resistive memory device requirements for a neural algorithm accelerator. In Proceedings of the 2016 International Joint Conference on Neural Networks (IJCNN), Vancouver, BC, Canada, 24–29 July 2016; pp. 929–938.
46. Kim, M.K.; Lee, J.S. Ferroelectric Analog Synaptic Transistors. *Nano Lett.* **2019**, *19*, 2044–2050. [CrossRef] [PubMed]
47. Hauser, J.R.; Ahmed, K. Characterization of ultra-thin oxides using electrical C-V and I-V measurements. *AIP Conf. Proc.* **1998**, *449*, 235–239.
48. McPherson, J.; Kim, J.-Y.; Shanware, A.; Mogul, H. Thermochemical description of dielectric breakdown in high dielectric constant materials. *Appl. Phys. Lett.* **2003**, *82*, 2121–2123. [CrossRef]
49. McPhersona, J.W. Extended Mie-Grüneisen molecular model for time dependent dielectric breakdown in silica detailing the critical roles of O−Si≡O3 tetragonal bonding, stretched bonds, hole capture, and hydrogen release. *J. Appl. Phys.* **2006**, *99*, 083501. [CrossRef]
50. Sze, S.M. *Physics of Semiconductor Devices*, 2nd ed.; Wiley-Interscience Publication: New York, NY, USA, 1981; pp. 438–448.
51. Qian, C.; Sun, J.; Kong, L.; Gou, G.; Yang, J.; He, J.; Gao, Y.; Wan, Q. Artificial Synapses Based on in-Plane Gate Organic Electrochemical Transistors. *ACS Appl. Mater. Interfaces* **2016**, *8*, 26169–26175. [CrossRef]
52. Fuller, E.J.; Keene, S.T.; Melianas, A.; Wang, Z.; Agarwal, S.; Li, Y.; Tuchman, Y.; James, C.D.; Marinella, M.J.; Yang, J.J.; et al. Parallel programming of an ionic floating-gate memory array for scalable neuromorphic computing. *Science* **2019**, *364*, 570–574. [CrossRef]