



# Article **Physical Insights into THz Rectification in Metal–Oxide–Semiconductor Transistors**

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Abstract: Metal–oxide–semiconductor field-effect transistors (MOSFETs) have proven to be effective devices for rectifying electromagnetic radiation at extremely high frequencies, approximately 1 THz. This paper presents a new interpretation of the THz rectification process in the structure of an MOS transistor. The rectification depends on the nonlinear effect of the carrier dynamics. The paper shows that the so-called self-mixing effect occurs within the interface region between the source and the channel. The basic tool used numerical TCAD simulations, which offer a direct interpretation of different aspects of this interaction. The complex, 2D effect is examined in terms of its basic aspects by comparing the MOS structure with a simplified case study structure. We demonstrate that a contribution to the output-rectified voltage detectable at the drain arises from the charging of the drain well capacitance due to the diffusion of excess electrons from the self-mixing interaction occurring at the source barrier. In addition, the paper provides a quantitative description of the rectification process through the definition of the output equivalent circuit, offering a new perspective for the design of detection systems.

Keywords: THz detectors; receiver system; semiconductor device modeling; terahertz radiation



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## 1. Introduction

The terahertz radiation (THz) spectrum occupies the gap between the microwave and infrared regions. Its unique ability to deeply penetrate beneath the surface of materials makes it valuable for applications such as medical imaging, security/surveillance imaging, and spectroscopy. It is considered medically safe due to its nonionizing nature and low associated power. Despite its potential, detecting high-frequency electromagnetic radiation, especially in the THz range, using integrated commercial electronics poses a challenge, driving substantial experimental and theoretical efforts to achieve high resolution, sensitivity, and low cost.

Recent endeavors focus on developing THz sensors using standard complementary metal–oxide–semiconductor (CMOS) technology, leveraging its robustness and costeffectiveness. Comprehensive reviews underscore the rapid progress in THz science and technology [1–7]. The integration of these characteristics opens up the possibility of realizing detector arrays at a large scale, enabling broad-area detection. In this context, a reliable model that incorporates the rectification process and provides an equivalent electrical circuit is crucial for supporting effective detector design.

Currently, the widely acknowledged model for THz detection using a CMOS transistor is the one proposed by Dyakonov and Shur [8], known as the plasma wave model. Originally derived for a two-dimensional (2D) electron gas, this model has been extensively applied and developed for MOS devices by various authors [9,10]. According to this model, when terahertz frequency (THz) radiation hits the antenna, creating a voltage drop between the MOS-FET's gate and source electrodes, carrier waves are generated in the 2D electron gas within the transistor's inversion layer. Nonlinearities in the semiconductor equations result in DC photovoltage. Recently, a new approach was developed, referred to as a self-mixing model in the substrate, showing how the presence of an RF electric field in the whole device semiconductor structure can also produce a DC rectified voltage. This result was first obtained by analytically studying a double-barrier structure [11], and then it was extended to a single barrier present in a unidimensional MOS structure in the depletion condition [12].

In this paper, we present a new detailed interpretation of the detection process in MOS transistors, using as a basic tool the program TCAD, Sentaurus Device [13]. The paper shows that an interaction of THz radiation with the semiconductor carriers occurs all along the entire structure and not only along the channel. In particular, it will confirm that the main site of rectification occurs along the potential barrier between the source-doped region and the channel.

In this investigation, we employ Technology Computer-Aided Design (TCAD) simulations to scrutinize the MOS detector. Our focus is on delineating the rectification mechanism, achieved through Harmonic Balance analysis (HB). Specifically, we expound on the origin of the rectification potential measured at the drain in an open-circuit condition and elucidate the decrease in response with increasing gate voltage.

The analysis will shed new light on several aspects of the rectification process, identified in [14] but not yet clarified. In particular, a new explanation of the origin of the potential measured at the drain in an open-circuit condition will be proposed, as well as the reason for its decrease at the largest gate voltages, a trend widely verified in measurements [10]. In the second step, the basic physical aspects will be investigated through an analysis of a case study structure expressly designed to permit the identification of the different aspects of the rectification process and to offer a clear explanation of their origin. Finally, the paper proposes a calculation method for the equivalent circuit of the detector, offering a direct representation of the rectification effect. This quantitative definition represents an essential step to achieving optimization of the detector/receiver. This result is presented here for the first time in the literature.

### 2. The Rectification Process in CMOS Transistors

The rectification process has been described by the plasma wave model [8], extensively accepted by the THz community since the mid-1990s. Once an electric field penetrates the semiconductor structure, the majority carriers move at a THz frequency, with sinusoidal acceleration limited by scattering. Nonlinearities present in the semiconductor equations give rise to the generation of nonhomogeneous terms and ultimately to the rectification effect. In this complex picture, the plasma wave model only takes into account one minimal detail, which is the modulation of the carriers along the MOS channel. The number of carriers in the channel is only a small portion of the overall number in the semiconductor. Moreover, the rectification effect occurs at values of the gate voltage such that the channel is in a weak inversion state [10]. In this condition, the number of majority carriers, which is extremely low, is certainly not enough to screen the remaining portions of the semiconductor structure from the penetration of the THz electric field.

A theoretical analysis that goes beyond the plasma wave model has recently been presented, developed under simplified conditions [15]. This approach shows that any potential barrier present in the semiconductor structure, in principle, gives rise to a rectification process. The two-dimensional structure of an MOS transistor prevents an extension of this approach to explain the entire transistor response. In particular, it is difficult to evaluate all the sources of the rectification effect and, by comparison, demonstrate if the rectification effect occurring along the channel is of any importance. Moreover, it is important to obtain an actual quantitative model of the interaction capable of controlling the interaction of the detector with external components of the receiver, i.e., the antenna and the Low-Noise Amplifier.

Fortunately, numerical simulators can precisely describe the response up to very high frequencies based on hydrodynamic equations and the ballistic mobility assumption. The TCAD simulator performs analysis using the hydrodynamic equations, based on the work of Stratton [16] and Bløtekjær [17], adopting a simplified approach using six partial differential equations [18].

Additionally, HB analysis permits obtaining precise results of the effects of equation nonlinearities in the structure response [19]. In this section, we will use the TCAD simulator, employing numerical HB analysis performed on an MOS transistor.

In the literature, the TCAD simulator has already been used in attempts to evaluate the MOS rectification process, with different approaches and different results. In [20], characterization was carried out in the transient regime through the examination of the drain voltage and then the extraction of DC and harmonic components using a Fourier transform. In [21,22], the capability of TCAD Sentaurus to treat quasi-2D plasma behavior was used, with the specific intention of limiting the interaction occurring between the carriers, the THz field, and the channel zone. In [23], the bell-shaped response of the voltage at the drain versus the gate bias voltage was extracted from two-dimensional simulations. In [24], the TCAD simulation was obtained to achieve the hot electron distribution over time.

The author himself has carried out extensive work using a TCAD to achieve an understanding of the behavior of the semiconductor structure in an MOS transistor at a high frequency [14,25]. The chosen approach is the one that uses HB analysis, which precisely describes the nonlinear processes that originate from the nonlinearities of semiconductor equations. The paper thus appears to be the completion of a long research journey that has opened up a new vision of the CMOS rectification process.

In the following simulations of the MOS structure, we assume that the transistor under test has a channel length of 200 nm, a width of 1  $\mu$ m, and a thickness of the silicon dioxide layer of 6 nm. The drain contact has a load resistance of 1 M $\Omega$ , representing a standard input resistance for a lock-in amplifier used in measurements in the literature. A contact is also assumed at the bottom of the structure, connected to the ground.

The HB analysis of the TCAD takes into account the nonlinearities present in the semiconductor equations. The solution accurately describes the self-mixing effect, i.e., the zero-order harmonic of the semiconductor quantities inside the structure. This result permits an accurate description, at the nanometric level, of the effects resulting from the THz interaction with charge carriers.

Figure 1a shows the structure of the MOS transistor used for the simulation. It is a rather simplified device, adopted to highlight the physical aspects of rectification. The circuit in the inset indicates the THz voltage generator,  $V_{RF}$ , which synthesizes the effect of the antenna, connected between the gate and source contacts. While the antenna can be sensitive to the polarization of the incoming radiation, the rectifier itself is not directly sensitive to it. The gate DC polarization voltage is given by the generator  $V_G$ . Figure 1b reports the distribution of the electrostatic potential in the structure, simulated at 1 THz.

Rectification has been demonstrated previously [15] to take place across a potential barrier within the structure, provided it is intersected by the THz electric field. In the MOS configuration under investigation, the high-frequency electric field is oriented from the gate towards the source, traversing the heavily doped area beneath the source contact. Initially, rectification leads to the displacement of charges across the barrier along the n+/n junction, i.e., the source/channel interface, resulting in the formation of a dipole. Consequently, this process generates a potential drop, which supplements the existing potential within the structure. The excess displacement of carriers in the depletion layer of a barrier crossed by the THz electric field was indeed predicted in [15], described by the following expression:

$$\widetilde{n}(x) = -\frac{J_{DC}(x)}{q\mu_n E_0(x)} \tag{1}$$

where  $\tilde{n}(x)$  is the spatial distribution of excess electrons,  $J_{DC}(x)$  is the spatially distributed nonhomogeneous term due to self-mixing, q is the electron charge,  $\mu_n$  is the electron mobility, and  $E_0(x)$  is the steady-state electric field within the depletion region in the barrier.



**Figure 1.** (a) The structure of the MOS transistor used for the simulation; in the inset is the connection of the generators; (b) the distribution of the electrostatic potential in the structure, simulated at 1 THz and  $V_{RF} = 100 \text{ mV}$ .

Figure 2 depicts the drop in the rectified potential arising in the transistor structure along the X direction at Y = 0. We want to highlight that the quantity reported in the figure is the difference between the DC electrostatic potential in the structure under THz excitation and the DC electrostatic potential at rest. In this paper, we will conventionally refer to this quantity as AA. The quantity AA is plotted along the silicon–silicon dioxide interface at Y = 0 against different values of the gate voltage,  $V_G$ .



**Figure 2.** Generation of a potential drop arising in the transistor structure at Y = 0. The quantity reported in the figure is the difference between the DC electrostatic potential in the structure under 1 THz illumination and 100 mV minus the DC electrostatic potential at rest. The indicative positions of the electrodes are reported.

Firstly, it can be observed that there is a potential drop between the source and the initial portion of the channel, corresponding to the left corner of the gate. In this part of the structure, there is a potential barrier between the highly doped source diffusion and

the channel. In addition, in this part of the structure, the most intense THz electric field at 1 THz exactly crosses the barrier.

Another, more pronounced phenomenon manifests between the latter part of the channel and the drain, which is noticeable only under specific gate polarization conditions. Notably, this effect is conspicuous at VG = 0.5 V. Given its considerable significance, this phenomenon holds paramount importance in receiver design. The elucidation of this specific occurrence is not straightforward; it will be elucidated subsequently, along with the discussion in Figure 3, and further affirmed in the subsequent paragraph.



**Figure 3.** Self-mixing potential generated in the structure excited by gate bias voltages: (**a**)  $V_G = 0.0$ , (**b**)  $V_G = 0.5$ , (**c**)  $V_G = 1.5$ , and (**d**)  $V_G = 2.0$  V, respectively.

Figure 3a–d, from [14], depict the 2D distributions within the MOS transistor structure of the self-mixing potential (AA) for gate bias voltages  $V_G = 0.0, 0.5, 1.5, and 2.0 V$ . It provides a different representation of the status of the rectified voltage reported in Figure 2. The exiting voltage was  $V_{RF} = 100 \text{ mV}$  at a frequency of 1 THz.

At  $V_G = 0.0 V$ , the channel is completely depleted. However, even in this condition, there is a rectification process. Indeed, self-mixing occurs within the source/channel barrier, which is also crossed in this condition by the electric field due to the THz potential applied between the gate and source. The consequence of the self-mixing is the formation of a charge dipole within the barrier and the creation of a potential drop, which can be clearly observed in Figure 3a as the blue spot under the gate corner. The potential does not propagate along the channel toward the drain since the channel is not yet formed, and the drop in the load resistance is negligible.

At  $V_G = 0.5$  V (Figure 3b), a weak formation of the channel takes place in the structure. The self-mixing-rectified voltage is still generated at the source/channel interface. With the channel partially established, surplus electrons diffuse along it and eventually thermally equilibrate within the heavily doped drain diffusion region. The accumulation of these charges results in the creation of a potential across the drain capacitance, consequently initiating a current flow into the load resistance. This diffusion current, originating from the self-mixing process at the source/channel barrier and diffusing towards the drain, persists until a potential is established within the drain well of sufficient magnitude to balance the current flowing into the load resistance with the self-mixing current.

The potential drop in the load resistance is now significantly greater than that along the channel. It should be noted that in this condition, the potential gained by the drain is much larger than the potential generated at the source/channel barrier, approximately one order of magnitude larger (see Figure 2). This additional effect, discussed for the first time in this paper, is of the greatest importance since it leads to a magnification of the output potential at the drain contact, ultimately increasing the detector's sensitivity. This effect can be explained as the nonohmic transport of excess carriers into the drain well by diffusion and thermalization. The carriers generated by the self-mixing in the depletion region of the source/channel barrier move to charge the drain capacitance. A further detailed illustration of the effect will be offered in the next paragraph.

With an increasing gate voltage at  $V_G = 1.5$  and 2.0 V (Figure 3c,d), while the MOS structure undergoes strong accumulation, we observe a significant reduction in the rectified voltage. Also, this behavior cannot be explained with trivial arguments and will be justified with numerical simulations in the next paragraph.

#### 3. A Case Study Structure

In this paragraph, we will still use TCAD simulations as a basic tool, but we will look at the case study of a particular structure. The structure does not represent an actual existing physical device; rather, it aims to schematize the transistor channel. The structure is designed to separate geometrically the different zones of the THz rectification and highlight the different effects occurring in an actual MOS detector.

The structure is reported in Figure 4a. It constitutes a long, thin slice of silicon, 400 nm long and 20 nm thick, with a uniform n-type doping concentration. The doping density in the silicon is varied as a parameter. At the edges of the slice are assumed to be two n-doped regions, 10 nm thick, with a dopant concentration of  $10^{19}$  cm<sup>-3</sup>, holding, respectively, the source and drain contact. Due to the source- and drain-doped regions, the extremes of the slice undergo accumulation.

This structure mimics, in a geometrically simplified and completely insulated way, the channel in an MOS transistor. The change in the carrier density in this simulated channel is no longer due to the field effect from the gates; rather, it is controlled parametrically. The variable doping in the slice replaces the effect of electron accumulation in inversion condition.

A couple of very short gates, each 10 nm long, are placed along the slice, 100 nm away from the source-doped region, and separated by a thin silicon dioxide layer, 6 nm thick, each one forming an MOS capacitance. A 10 nm thick silicon layer and a contact form each gate. The silicon layers of the gates have the same doping density as the slice, which is varied as a parameter. This choice ensures that the flat-band voltage in the MOS structure is zero, thus avoiding the bending of the silicon bands at the interfaces. A variable voltage,  $V_{RF}$ , at 1 THz is applied between the source and the two gates in parallel. The bias voltage is zero. The relevant distance between the gates and the source allows us to consider the electrostatic potential to be constant in each X section of the slice, thus permitting us to ignore two-dimensional effects. In this structure, the role of the gates is completely different from that in an MOS transistor; they do not control the channel formation. The difference in the dimensions of the slide, 400 nm, compared to the dimensions of the gates, 10 nm, means that the overall conductivity of the slide is not controlled by the gates. In the MOS

transistor, at zero drain bias, the gate controls entirely the conductivity of the channel between the drain and source. On the other hand, since at the two gates one extreme of the THz signal is applied, the potential imposes a variable electric field all along the portion of the slice between them and the source. This is verified by simulations as long as the doping is lower than  $1 \times 10^{17}$  cm<sup>-3</sup>.



**Figure 4.** (a) The case study structure with doping in the  $10^{15}$  cm<sup>-3</sup> slice; (b) the distribution of the potential at 1 THz, with a 1 mV amplitude applied between the two gates and the source.

We aim to show that a self-mixing effect arises at the potential barrier between the source-doped region and the slice. The barriers between the semiconductor in the slice and the source/drain-doped zones are far from the gates, so the other possible origins of the generation of the self-mixing-rectified voltage, eventually present, could be easily individuated within the simulation results. In addition, the channel, in MOS transistor terms, i.e., under the gates, is extremely short. This allows us to discard, for example, the hypothesis of generation in the channel, as foreseen by the plasma wave model.

Figure 4a reports the structure with doping at  $10^{15}$  cm<sup>-3</sup>, while Figure 4b reports the distribution of the potential amplitude at 1 THz with V<sub>RF</sub> = 100 mV applied between the two gates and the source. In order to direct the explanation, we define two regions: one above the two gates (x < -0.1 µm), the region towards the source, and one below the gates (x > 0.11 µm), the region towards the drain.

Figure 5 reports the cut along the axis of symmetry at y = 0 of the distribution of the self-mixing DC potential generated within the structure for several different doping levels. One can first note that the lower doping level,  $10^{15}$  cm<sup>-3</sup>, produces the larger voltage. The potential has its maximum at the drain extreme and decreases along the slice. Incidentally, we note that the potential drop cannot be caused by a current, given the open drain.

The potential has two different branches. In the region above the gates, the potential increases from the source barrier, reaching a first plateau. In this region, the potential is due to the self-mixing dipole generation described by Equation (1). Below the gates, the potential still grows, reaching much higher values, with the maximum at the drain. In this

region, the potential is due to the charging effect of the capacitance of the drain diffusion well. The slope of growth along this region of the slice is also due to electrostatic charge since the semiconductor is partially accumulated. This second growth begins beside the two gates due to their capacitive effect, which deviates toward the ground as the electric field flows from the drain.



**Figure 5.** Cut at y = 0 of the distribution of the self-mixing DC potential generated within the structure for several different doping levels.

We note that the growth in the potential in the second region, below the gates, repeats what was observed in the second part of the channel in the MOS transistor, as shown in Figure 2. Now we understand that this is not an effect of the MOS transistor but rather an effect of the redistribution of the charges, displaced by the self-mixing effect, and accumulated in the drain.

At higher doping concentrations, the self-mixing voltage at the drain extreme is always at a maximum, even if this maximum decreases with increasing doping. The potential remains almost constant for the portion of the slice below the gates, sharply decreasing and reaching a common value at 110 nm, i.e., at the edges of the gates. This effect will be explained based on a discussion of Figure 8.

Before this, we concentrate on the potential amplitude in the region above the gates, which remains constant as long as the doping remains at  $10^{16}$  cm<sup>-3</sup>. A strong change in behavior occurs when the doping concentration of the slice reaches a value of  $3.10^{16}$  cm<sup>-3</sup>. There is a general decrease in the potential, both above and below the gates. Larger values of doping give rise to a further decrease in the potential, with the formation of a small peak arising in correspondence with the gates.

The interpretation of these results requires an evaluation of other information obtained by the TCAD simulations.

Figure 6a,b report the distributions along the slice of two quantities involved in the rectification process: the amplitude of the THz electric field in the X direction, Ex, and the amplitude of electron variations. The values of the two quantities are shown on the left axis. The different amplitudes permit a shifted representation.

The two figures report data from two simulations performed at two different doping levels in the silicon slice, respectively,  $10^{15}$  and  $10^{17}$  cm<sup>-3</sup>. On the left axis are quoted the amplitude of the THz electric field in the x direction,  $\tilde{E}_x$ , and the amplitude of the electron variations. On the right axis, the product of these two quantities, i.e., a term proportional

to  $J_{SM}$ , the DC nonhomogeneous term arising from nonlinearities, is shown [15] (in the plotted term, q and  $\mu_n$  have not been multiplied).

$$J_{SM} = q \left\langle \tilde{n} \mu_n \tilde{E}_x \right\rangle \tag{2}$$

Both quantities,  $\tilde{n}$  and  $\tilde{E}_x$ , are small signal variations at a THz frequency. These results indicate that the self-mixing effect only occurs in the upper portion of the slice. This could be interpreted by the fact that in this region there is a large intensity of the THz electric field, together with a large variation in the electron density, and thus it is there, due to the nonlinearities of the semiconductor equations, that the self-mixing mainly takes place.



**Figure 6.** Distributions along the slice of the quantities involved in the rectification process: the amplitude of the THz electric field in the x direction, Ex, and the amplitude of electron THz variations, quoted on the left axis. The self-mixing term, Jsm, is quoted on the right axis. (**a**) Doping of the slice at  $10^{15}$  cm<sup>-3</sup>; (**b**) doping of the slice at  $10^{17}$  cm<sup>-3</sup>.

The self-mixing forcing term,  $J_{SM}$ , is a current. It pushes electrons away from the doped region of the source toward the slice, giving rise to an increase in the electron density at the border. Most of the displaced electrons just diffuse back directly to the source well due to the formation of a dipole inside the barrier. A side effect of the formation of the dipole is the generation of a potential variation.

This effect has been extensively described in former works [15]. We assume it is responsible for the rise in the self-mixing potential in the upper portion of the slice, from the source barrier up to the gates.

One can note in Figure 6b how the nonlinear forcing term becomes closer to the source barriers as the doping increases, as long as the width of the region with the electric field reduces. We also notice that a peak arises, just in correspondence with the gates. This peak, which spatially coincides with the peak noted in Figure 5, will be explained later, after Figure 11.

Let us now come to a second important effect which must be considered. As in an MOS structure, the increase in the electron concentration within the source/slice barrier also increases the electron density at the slice boundary in this structure. Also, in this structure, this gives rise to a diffusion current in the slice, equivalent to the current in the MOS channel, which reaches the drain. The current can be directly sensed at the drain electrode in short-circuit conditions, Isc. Figure 7a shows the behavior of Isc under  $V_{RF} = 100 \text{ mV}$  at 1 THz versus the gate DC bias voltage.

The initial growth in the current in Figure 7a follows calculations in [15], which show an increase in the offset of electrons due to self-mixing with a decrease in the barrier height. The subsequent decrease in Isc, up to two orders of magnitude, is, on the contrary, related



to the screening effect occurring at large doping concentrations and will be illustrated in the last part of this description.

**Figure 7.** (a) The short-circuit drain current, Isc, under 100 mV at 1 THz versus the DC bias voltage at the gate; (b) the absolute value of the open-circuit voltage at the drain, Voc, versus the DC bias voltage at the gate.

In an open-circuit condition, the injection of electrons into the slice leads to a collection of electrons in the highly doped, n-type drain well. In turn, this gives rise to the generation of a negative potential at the drain. A negative potential produces a decrease in the barrier between the n-well and the slice semiconductor, generating a reverse flow of electrons. The accumulation of electrons at the drain terminates when the two current terms, the barrier current and the diffusion current from self-mixing, equate. The higher the doping of the slide, the lower the barrier versus the drain well, and the lower the potential reached before the compensation of Isc will be.

An illuminating comparison that we can propose here is that with a solar cell. A solar cell is a p–n junction. Once illuminated by light, and in short-circuit conditions, a photocurrent proportional to the light intensity is measured. In open-circuit conditions, a voltage drop is generated as a result of the charging of the parasitic capacitance of the collector. This produces a current across the p–n junction that is equal and opposite to the photocurrent, which thus nulls the total current.

Figure 7b reports the behavior of the absolute value of the DC potential at the drain in open-circuit conditions, Voc, versus the doping density of the slice. It can be noted that, moving toward lower doping values, Voc does not decrease with Isc. This can be explained by the fact that, in order to compensate for the self-mixing current, the drain voltage must overcome the built-in voltage, whose value increases, following the simple barrier law, with the logarithm of the inverse of the doping in the slice.

The THz potential adopted in the simulations of the case study structure is equal to the one adopted in the MOS simulations, 100 mV. Nevertheless, the distance between the electrodes is now quite a bit larger: 100 nm with respect to 6 nm for the oxide. Thus, the electric field in the case study structure is more than one order of magnitude smaller than that in the MOS. Being the rectification quadratic, this justifies almost two orders of magnitude of difference in the detected DC voltage. The values obtained are coherent with several measurements reported in the literature [9,26–28].

Second-order nonlinear effects, which are certainly possible in principle, are not relevant at the levels of the variable electric field and variable potential adopted. In particular, we obtain a trend of the rectified potential proportional to the square of the applied potential amplitude.

In order to further prove the effect of the charging of the drain, Figure 8 reports the portion of the distribution of the density of the electrons accumulated at the drain in opencircuit conditions. The quantity plotted here, conventionally named A1, is the difference





Figure 8. A portion of the distribution of the density of the electrons at the drain in open-circuit conditions.

It is evident that a greater increment occurs when the doping level of the slice is lower. This observation aligns with the previous finding that a higher barrier necessitates a larger generated potential, resulting in a greater accumulation of electrons to produce a current equal and opposite to the self-mixing current. Specifically, this accounts for the heightened self-mixing potential at the drain observed in the case of low doping in Figure 5.

The equivalent circuit obtained from simulations, whose parameters change following Figure 7a,b, can have an important role in receiver design. We must consider that a Low-Noise Amplifier must follow the detector, and its input capacitance must be considered in the detection process. The capacitance has to be charged and discharged at the frequency of the signal. For example, in the case of a radiation sensor, chopping of the radiation is necessary to reduce the effect of noise, which at low frequencies is of the 1/f type. In the case of a detector in a communication system, the de-modulated signals may have a very high frequency. The structure "Rectifier–Low-Noise Amplifier" is schematically reported in Figure 9. The capacitance reported represents schematically the combination of the drain well capacitance and the LNA input capacitance. The detector is represented by the equivalent circuit, Voc–Rout. The detector design must verify that the capacitance may be charged and discharged at the signal frequency.



**Figure 9.** Schematic of the structure "Rectifier–Low-Noise Amplifier". The Thévenin equivalent circuit is reported as superimposed on the MOS transistor rectifier.

In [14], we thus suggested extracting from the TCAD simulation the value of the equivalent output resistance, obtained using the following ratio:

$$R_{out} = V_{oc} / I_{sc} \tag{3}$$

Figure 10 reports the values of the output resistance,  $R_{out}$ , obtained for different values of gate voltage. The values decrease significantly as the gate voltage increases. The necessity to fulfill the required bandwidth for the signal prevents us from using the lower  $V_{\rm G}$  values, where the rectified voltage would be higher, but  $R_{out}$  would be much higher. An optimization process is necessary to find the best condition for the polarization of the detector.



Figure 10. Output resistance obtained for different values of gate voltage.

The obtained behavior of the output resistance permits us to discuss the bell-shaped curve presented by several reports in the literature [9,26–28]. Real measurements, for practical reasons, present the rectifier loaded with a finite load impedance from the reading amplifier, further reduced by the input admittance at the chopping frequency of the input radiation. This produces a decrease in the detected voltage at low bias voltages when the output resistance of the rectifier reaches the highest values.

The simulated curve shown in Figure 10 instead was obtained through HB analysis, thus in steady-state conditions with an extremely high value of load resistance (10<sup>+10</sup> ohms) to obtain a good approximation of the Thévenin equivalent circuit. The output voltage shown in Figure 7b thus maintains a monotonic decrease.

To the author's knowledge, there is only one measurement, reported in [10], performed at decreasing chopping frequencies up to very low values, in which the bell-shape of the voltage measurements clearly tends to transform into a descending step.

In order to summarize this part, we may conclude that we have determined that the rectification process takes place only in the portion of the slice closer to the source, while the accumulations into the drain of electrons driven by the self-mixing effect constitute the main contribution to the rectified voltage.

At the end of this analysis, we examine a further point of relevant importance. It is relative to the strong decreases in the rectified current and voltage with the increase in the slice doping, as obtained in the simulations reported in Figure 7. The effect is visible starting from a doping concentration of  $10^{17}$  cm<sup>-3</sup>. From the consideration presented when discussing Figure 6b, we know that at this doping level, the THz electric field starts to interact with electrons in the slice right beside the gates. This screens all the other portions of the slice. The THz potential decreases, as can be seen in Figure 11, which shows the simulated distribution along the center of the slice for different values of silicon doping under 1 mV applied at the gate. This effect, in particular, produces a strong reduction in the THz electric field in the doped region of the source, thus reducing the self-mixing effect with the electrons.

The presence of large amplitudes of the variable electric field and variable electron density in the slice region under the gates produces a new site of rectification, just under the gates. This alternative effect is much lower than the one occurring at the source. First, because of the lack of a DC electric field in the interaction zone (the slice is homogeneous in the Y direction), the largest term of the self-mixing rectification described in [11] is cancelled out. Secondly, the THz electric field is, in this case, normal to the oxide; therefore, the direction of the nonhomogeneous current term generated is also normal to the oxide. The current direction, directed against the oxide, nullifies the flow toward the drain. The null contribution of this second effect, together with the screening of the THz electric field from the other junctions, reduces the output-rectified voltage.



**Figure 11.** Distribution of the amplitude of THz potential along the slice for different values of silicon doping.

In the former Figure 5, this effect corresponds to an increase in the self-mixing potential, and in Figure 6b, it corresponds to an increase in the self-mixing current, just under the gates, with doping equal to or greater than  $10^{17}$  cm<sup>-3</sup>. This self-mixing current is now generated orthogonally to the gate oxide, and the DC potential is generated between the semiconductor and the gate, toward the ground. For this reason, the interaction does not produce a current along the slice, and it has no effect on the drain potential.

To conclude the section, we wish to point out that, even if obtained using a case study structure, these results can be directly extended to interpret the behavior of the MOS transistor structure. In an actual transistor, the channel length is shorter but comparable with that of the study structure (300 nm). The main difference is the geometry of the barrier source region/channel, which is located just below the gate corner, receiving the THz electric field distributed in a 2D shape, making the interpretation of the TCAD simulations less direct, and nevertheless, in this case, the self-mixing effect also generates a charge dipole. Similarly, the accumulation of electrons confined to a very thin region beside the oxide, following the field effect, makes the variable behavior less evident, but the MOS structure also undergoes no screening in weak inversion and complete screening in strong inversion once the density of electrons accumulated varies.

## 4. Conclusions

This paper presented a new interpretation of the THz rectification process in the structure of an MOS transistor. The rectification depends on the nonlinear effect of the carrier dynamics. The so-called self-mixing effect occurs within the interface region between the source and the channel. It is enhanced by the presence of a DC electric field. The numerical TCAD simulations offered an interpretation of the different aspects of this interaction. The complex, 2D effect was examined in terms of all its aspects by comparing the MOS structure with a simplified case study structure.

In particular, the obtained interpretation depicts the THz modulation mechanisms of the carriers in the interface region between the source-doped region and the channel. In addition, we demonstrated that a contribution to the output-rectified voltage detectable at the drain, a contribution which can be of a relevant amplitude, arises from the charging of the drain well capacitance due to the diffusion of excess electrons from the source.

Finally, we showed that an additional site of self-mixing is generated just below the gate once the density of the electrons in the channel increases above a value of 10<sup>17</sup> cm<sup>-3</sup>. The drain contact in this case does not sense this further effect, mainly due to the orthogonal geometrical orientation of the self-mixing current term. This prevents the generated rectified current from reaching the drain well. Rather, this interaction screens the variable electric field from the area of the source, reducing the self-mixing effect, an effect that occurs there at lower doping values. This final observation explains the reduction in the rectified voltage detected once the gate potential and density of electrons in the MOS channel increase.

The paper aims to provide the essential tools for the design of a THz rectifier. A side result of the paper is that showing the exact mechanisms of rectification in an MOS transistor, in the author's opinion, brings into discussion the validity of the plasma wave model.

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