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A New 3-Dimensional Graphene Vertical Transistor with Channel Length Determination Using Dielectric Thickness

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Abstract: This study introduces a novel three-dimensional (3D) vertical field-effect transistor (FET) structure that utilizes two-dimensional (2D) graphene as the channel, with channel length controlled by deposited dielectric thickness. The dielectric deposition process allows for the easier implementation of small-scale features on the order of nanometers compared to traditional patterning processes. Incorporating 3D vertical structures with 2D channel materials enhances device performance beyond conventional planar designs. The fabrication process involves direct graphene growth for the channel and nanometer-scale dielectric deposition for the facile adjustment of channel length. The experimental results validate successful graphene formation and transistor operation, as evidenced by current–voltage characteristics. The 3D Vertical FET holds promise for improved device integration and overall system performance due to its unique device structure and an effective short-channel implementation method. This research underscores the potential of 2D materials in advancing transistor technology, and presents a practical approach for increasing device density and enhancing performance in semiconductor production processes.

Keywords: vertical transistor; short channel length; 2D materials; field effect transistor; graphene

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1. Introduction

The continuous drive for smaller, faster, and more energy-efficient electronic devices has led to the exploration of advanced transistor architectures [1,2]. Traditionally, transistor designs have predominantly relied on planar geometries with a two-dimensional (2D) channel. However, as device dimensions approach their physical limits, the performance gains obtained through conventional scaling are diminishing [3–5]. Furthermore, the limitations of small-scale components are also determined by the constraints of the manufacturing technology. Reducing the size of components requires increasingly smaller patterning technologies, but the infinite development of patterning technology is not an easy task. To overcome this challenge, researchers have turned their attention to three-dimensional (3D) integration and the incorporation of 2D channel materials [6]. One of the primary advantages is the increased device density achievable by stacking multiple transistor layers vertically. This vertical integration approach provides a pathway to circumvent the limitations imposed by planar scaling, allowing for a higher number of transistors within a given chip area. Furthermore, 3D transistors exhibit improved electrostatic control, reduced leakage current, and enhanced short-channel control, which collectively contribute to enhanced device performance [7,8].

Two-dimensional channel materials, such as graphene, have garnered significant attention due to their exceptional electronic properties. These atomically thin materials offer superior carrier mobility, ballistic transport, and excellent electrostatic control, making them highly promising candidates for use as the channel material in transistors [9,10].

By combining 3D vertical structures with 2D channel materials, researchers aim to harness the unique properties of both to achieve enhanced device performance and functionality. This study aims to explore a semiconductor device structure and manufacturing

method that can implement 2D material components in a 3D vertical structure, providing the advantages of both. We intend to discuss the possibility of achieving both benefits by suggesting a semiconductor device structure and manufacturing method. Additionally, we aim to enhance the feasibility of 3D structure fabrication, including a method to more easily implement short channels using Depo processing instead of patterning processes. This paper describes the experimental methods and manufacturing processes used to validate the proposed ideas, as well as the physical and electrical characteristics resulting from the experiments conducted based on these methods. Additionally, it presents interpretations of the results and confirmation of the feasibility of the ideas based on the final validation results, and discusses potential applications of the research content in the semiconductor industry.

2. Materials and Methods

In this study, we propose a novel structure of a 3D vertical field-effect transistor that utilizes a 2D material as the channel, with the channel length controlled by the deposition thickness of the dielectric material. As mentioned earlier, the research results from the integration of these two aspects are limited in practical utility. Short channel devices have not been implemented, or the fabrication processes are exceedingly complex and costly, such as relying on fine lithography processes. However, in this study, we propose a method that addresses these challenges by utilizing graphene as the 2D channel material and directly growing it to form the channel. Graphene has gained attention as a material to replace silicon due to its high charge mobility, and research on components utilizing graphene has been ongoing for decades. However, most studies either involve creating a simple component structure after conducting physical and chemical tuning to open a band-gap or propose alternative uses of graphene for IC components other than logic devices. We aim to utilize the relatively facile growth of graphene as a type of 2D channel material in the channel of a 3D vertical FET. Our intention is to use this configuration to validate that the proposed 3D FET component structure can function as a transistor. Moreover, the thickness of the short channel is easily achieved through the deposition and adjustment of the dielectric layer at the nanometer scale, offering a simple and cost-effective implementation approach.

Figure 1 illustrates the structure of a 3D vertical field-effect transistor that utilizes graphene, a 2D material, as the channel, with the channel length controlled by the dielectric thickness. In contrast to the conventional planar device structure, where the Source–Body–Drain components are located on the same plane, the 3D vertical field-effect transistor shows a vertical arrangement with the Source–Body–Drain components positioned upright, while the gate insulator and electrodes are placed on the sidewalls. The cross-sectional view depicted on the right side of Figure 1 shows that the Drain–Body–Source components form a Metal–Insulator–Metal (MIM) stack, with the 2D channel material positioned on the sidewall of the MIM structure, enabling operation of the channel. The thickness of the dielectric material located in the center of the MIM structure becomes the channel length, allowing for easy control of the channel length through adjustments of the deposition thickness of the insulator. If the gate insulator and electrodes, deposited on the sidewall, are not separated, the transistor can operate as a dual-channel transistor, utilizing both sides of the MIM structure as channels. Conversely, if they are separated, each side of the sidewall can form one transistor, with both functioning as individual transistors.

The detailed fabrication process of the device is illustrated in Figure 2. Initially, a SiO_2 layer with a thickness of 300 nm was deposited onto the wafer to serve as the substrate and bottom electrode. The motivation behind the use of such a substrate is that Si wafers are the most readily available in the market; moreover, they are easily adaptable to semiconductor processes. Additionally, Si wafers need to be insulated with materials such as SiO_2 to eliminate the influence of the underlying substrate, allowing for smooth verification of the operation of the structure proposed in this study. To determine the channel length, a dielectric material was also deposited. One of the newly proposed aspects in this study

is precisely this: the utilization of dielectric deposition processes instead of traditional patterning processes to achieve a short channel length. To achieve a short channel length in current semiconductor devices, one of the crucial processes is the patterning process, which involves photo and etching steps. The foundation of all patterning processes ultimately relies on the photo process, and securing an overall patterning process that can support this step is a practical necessity for realizing a short channel length. However, as we enter the sub-nanometer scale of device dimensions, the development of such processes is gradually becoming more challenging, and the associated costs are also significant. Nevertheless, the deposition process, one of the key processes in semiconductor manufacturing, has been operating on the sub-nanometer scale for quite some time. Notably, in processes such as ALD, deposition on the atomic layer level is possible, allowing sub-nanometer-scale deposition through multiple cycles. In the presented vertical field-effect transistor, the channel length is positioned in the vertical direction, unlike in planar devices, where it is in a horizontal orientation on the substrate. Consequently, the material deposited in the initial stages, rather than the substrate itself, serves as the substrate or body of the device. This newly deposited material, essentially the outcome of the deposition (depo) process, plays a role in determining the channel length. As mentioned earlier, the ALD process used for depositing dielectric materials can already be undertaken on the sub-nanometer scale. This allows for the straightforward construction of the body region at this scale, effectively determining the channel length in the resulting structure.

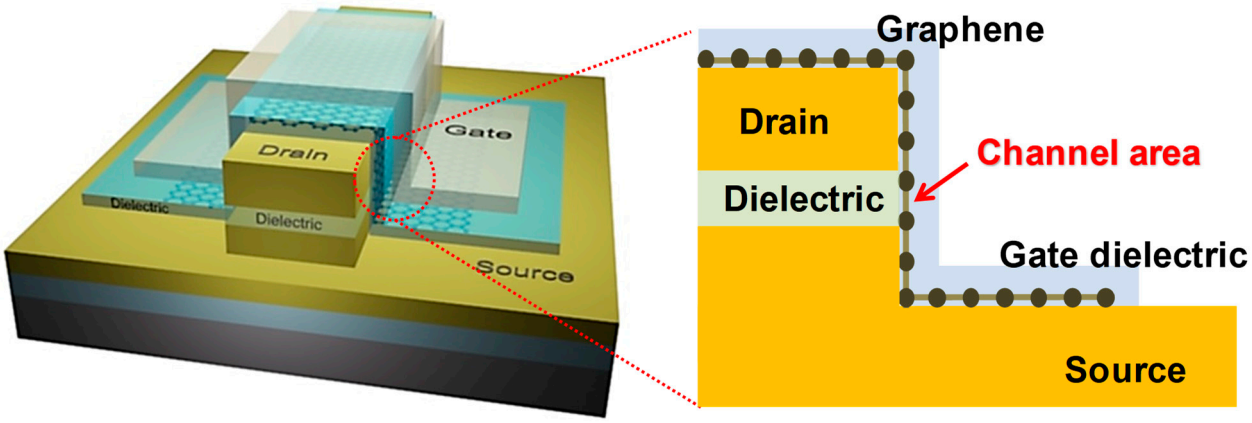

Figure 1. A schematic image depicting the determination of the channel length in a vertical transistor structure based on the dielectric thickness, along with a cross-sectional view of the channel area.

Electrodes capable of forming the source and drain are deposited through the deposition process on both sides of the dielectric material. As graphene was utilized as the channel material, a material capable of direct graphene growth was chosen for the bottom electrode to facilitate patterning. While there is a method involving a transfer process, where graphene grown on a different substrate is physically moved and utilized, in this study, a more simplified and integrated process flow was adopted. The chosen approach involves directly growing graphene, with the goal being to streamline the process as much as possible and validate the potential of the direct utilization of graphene in the future. Consequently, Co was selected for this purpose [11,12]. For the dielectric layer, Al_2O_3 was used, and a 10 nm-thick film was deposited. For the top electrode, a patterned shape was easily formed through a lift-off process using a photoresist. Ni was employed for this purpose, as it allows for easy patterning while withstanding the dry etch process during the patterning of the bottom electrode and dielectric.

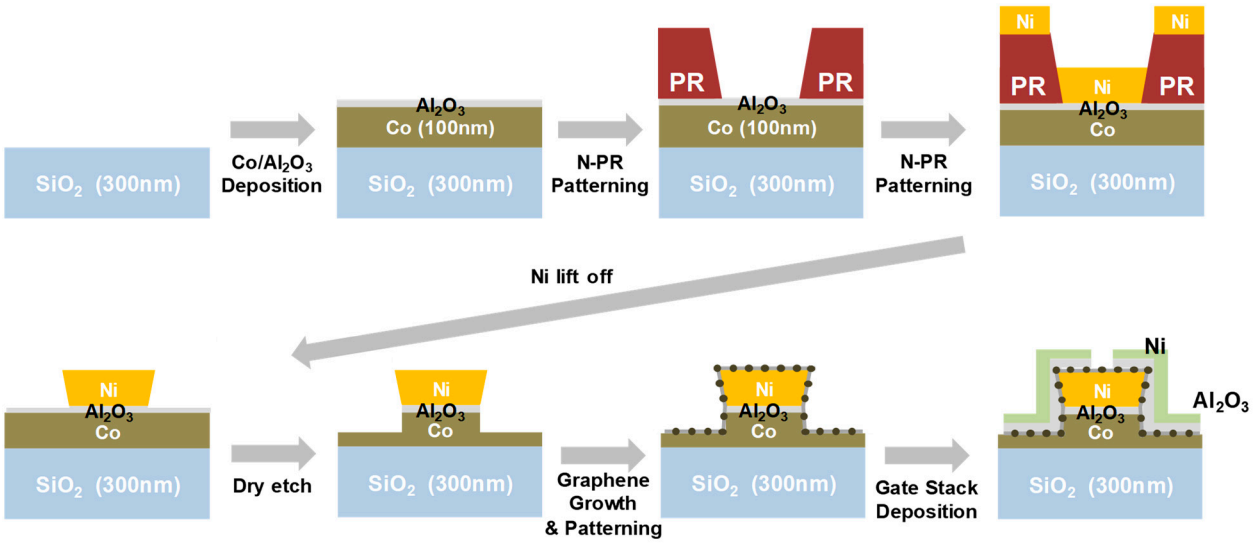

Figure 2. Schematic process flow for a vertical transistor; a 300 nm SiO_2 wafer substrate was prepared, onto which the Al_2O_3/Co stack was deposited. The stacked substrate was then patterned with a photoresist (PR). Ni was subsequently deposited on the patterned substrate, followed by a lift-off process to form the top metal. The Al_2O_3/Co stack was etched using ICP-RIE with Ni serving as a hard mask. Subsequently, graphene growth was carried out on Co and Ni substrates, followed by defining the channel area through patterning. Finally, the gate stack (Al_2O_3/Ni) was formed on the graphene via a lift-off process.

As mentioned earlier, the foundational framework for developing vertical devices is built upon the utilization of Ni to pattern Co and Al_2O_3. This initial establishment of the framework lays the groundwork for subsequent advancements and innovations in the field. After the development of the framework, the focus shifts to the growth of graphene to serve as the primary channel material. In this process, the Inductively Coupled Plasma Chemical Vapor Deposition (ICP-CVD) method plays a pivotal role. The ICP-CVD method is chosen for its effectiveness in facilitating the growth of graphene under controlled conditions. The substrate undergoes a meticulous heating process, reaching a temperature of 970 °C, while maintaining a pressure of 50 mTorr in an Ar ambient environment infused with H_2 plasma. This carefully calibrated thermal environment sets the stage for the subsequent stages of graphene development. Following the heating phase, the substrate is subjected to a strategic exposure of a mixture of C_2H_2 and Ar, with a specific flow rate of 1:150 sccm. This exposure lasts for five minutes, ensuring the thorough and comprehensive integration of the desired graphene characteristics. The deliberate selection of these growth conditions reflects a meticulous approach towards achieving optimal graphene properties. This intricate process is integral to ensuring the success of the subsequent stages of device fabrication and functionality. The comprehensive nature of these growth conditions not only serves the immediate goal of producing graphene, but also lays the foundation for further explorations and experimentations in the realm of advanced semiconductor device architectures. Through this elaborate process, this study aims not only to advance current technology, but also to pave the way for future breakthroughs in the field of graphene utilization in semiconductor devices.

In the context of this particular structure, where short channel devices are involved, it should be noted that while graphene typically exhibits growth solely on metal surfaces, there was the anticipation that some of the graphene formed on the top/bottom electrodes may extend laterally, establishing contact with the sidewalls of the dielectric. This lateral expansion could potentially contribute to enhancing certain device characteristics, especially concerning the short channel effects. Subsequent electrical characterization experiments were conducted to validate and ascertain the success of this anticipated graphene formation. The confirmation of graphene formation as expected paved the way for the sub-

sequent steps in the fabrication process. Following the successful generation of graphene, photolithography was employed to meticulously match the channel width to the desired specifications. This step ensures precision and accuracy in the dimensions of the channel, critical aspects when optimizing device performance capabilities. With the channel width now tailored to the required specifications, the next phases involved the patterning and deposition of the gate dielectric and gate electrode. In these subsequent steps, the lift-off method was employed to pattern and deposit the gate dielectric and gate electrode. This resulted in the formation of a structured layer comprising Al_2O_3 (10 nm)/Ni (50 nm). In this study, in addition to directly growing 2D materials, we fabricated devices utilizing graphene grown on Cu and transferred using a wet transfer method, demonstrating its applicability beyond growing materials directly on substrates. Although all fabrication processes were similar to those described earlier, the key difference lies in the method of transferring graphene rather than growing it directly. The process of transferring graphene remains consistent with conventional wet transfer methods. After growing graphene on Cu, the PMMA polymer was deposited, followed by physical delamination to separate Cu from the SiO_2 substrate. Subsequently, Cu was removed through wet etching, and the remaining graphene and PMMA were transferred onto the desired substrate, followed by the removal of PMMA.

The careful selection of materials and the meticulous deposition process contribute to the creation of a robust and precisely engineered structure. This not only functions as a critical element within the device's architectural framework, but also introduces a layer of adaptability and functionality to the broader semiconductor design. It is imperative to underscore that each procedural step in this methodology is intricately interconnected, where the success of one phase significantly impacts the effectiveness of subsequent stages. The intentional and systematic approach undertaken at each juncture underscores our dedication to achieving not only the formation of graphene, but also the optimal configuration of the ensuing device components. As this intricate process unfolds, it symbolizes not merely the fabrication of a semiconductor device, but the meticulous coordination of a sequence of thoughtfully designed measures aimed at expanding the boundaries of both device performance and functionality in a scholarly context.

3. Experimental Results and Validation

As previously discussed, the utilization of graphene as the channel material was a fundamental aspect of this study, and the channel itself was meticulously fashioned through a direct growth method. It is crucial to highlight the significance of ensuring the accurate and optimal formation of the channel in the semiconductor device. This critical aspect was subjected to a comprehensive evaluation, and its integrity and characteristics were thoroughly examined using advanced techniques. First, Raman spectroscopy, a powerful analytical tool, was employed for a meticulous analysis of the graphene channel. This technique allows for the non-destructive characterization of the material's structural and vibrational properties. By leveraging the unique spectral features of graphene, Raman spectroscopy serves as a valuable diagnostic tool in validating the crystalline structure and quality of the channel material. The acquired spectroscopic data provide insights into the vibrational modes of the graphene lattice, offering a nuanced understanding of its atomic arrangement and the potential presence of defects. Furthermore, beyond the spectroscopic analysis, the integrity of the graphene channel was further scrutinized through precise current–voltage measurements. The application of electrical characterization techniques, as depicted in Figure 3, allows for a detailed examination of the electronic behavior of the graphene channel.

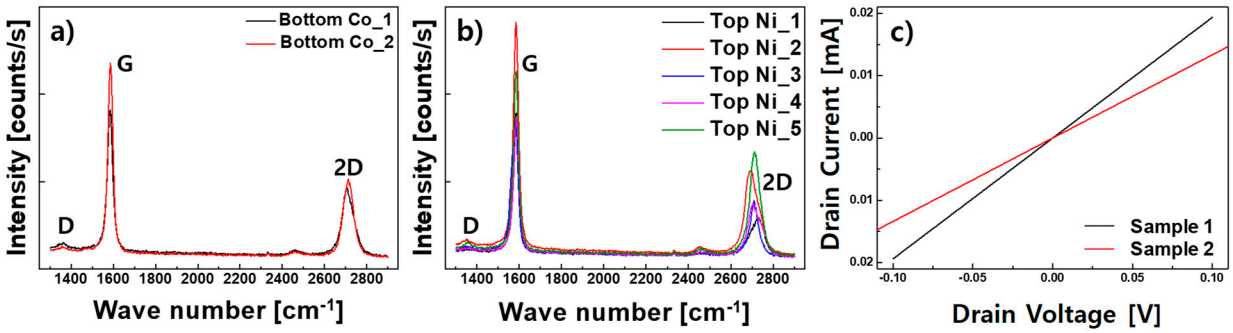

Figure 3. Verification results of graphene formation in the dielectric region: (**a**) ratio mapping of the 2D Raman spectroscopy revealing the presence of graphene on the bottom Co and (**b**) the top Ni electrode, and (**c**) I_{Drain}-V_{Drain} characteristics after graphene growth indicating the presence of graphene on the sidewall of the Al_2O_3 dielectric material.

By subjecting the channel to varying voltage levels and measuring the resulting current, a comprehensive electrical profile is obtained. This profile aids in assessing the conductivity, carrier mobility, and overall electronic performance of the graphene channel. The amalgamation of Raman spectroscopy and current–voltage measurements not only ensures a multi-faceted evaluation of the graphene channel, but also establishes a robust foundation for validating its suitability for semiconductor applications. The acquired data serve as a comprehensive guide with which to ensure the efficacy of the direct growth method employed during the channel formation process. This meticulous scrutiny is not merely an exercise in validation; rather, it is a crucial step towards refining and advancing our understanding of the properties of the graphene channel and the potential implications for future semiconductor technologies.

In Figure 3a,b, the Raman spectra following the formation of graphene are showcased, with Ni as the top electrode in (a) and Co as the bottom electrode in (b). Raman spectra serve as a valuable tool for extracting information about material based on the intensity at various wavelengths. The ratio of peaks discerned from these spectra becomes particularly significant as it offers insights into the successful formation of multi-layer graphene [13–15]. Generally, monolayer graphene exhibits a ratio of 1:1.5~2 between the first (G-peak: ~1580 cm^{-1}) and second peaks (2D-peak: ~2680 cm^{-1}). Additionally, the presence of a small peak (D-peak: ~1350 cm^{-1}) preceding the first peak indicates the existence of impurities (e.g., oxygen, hydrogen) within the graphene. The larger the size of this peak, the higher the concentration of impurities. These impurities can arise during the graphene growth process or may be introduced by wet chemical etchants or polymers used in the physical transfer process. Examining the spectra presented in Figure 3a,b, it is evident that because the graphene is directly grown on metal, there are almost no peaks indicating impurities. However, the ratio of peaks indicates the absence of a monolayer structure. This implies the formation of multi-layer graphene. Although multi-layer graphene does not possess the same characteristics as monolayer graphene, it still exhibits properties that could allow for the modulation of the charge transport with the fabrication of a field-effect transistor controlled by the gate voltage. The primary objective of this research was to validate the functionality of the proposed transistor structure. In pursuit of this goal, different metal materials were employed, and the overall structure was treated as a transistor. A deliberate decision was made not to explore the formation of monolayer graphene; given that doing so was not aligned with the central focus of verifying the transistor structure's functionality. Instead, emphasis was placed on the successful verification of multi-layer graphene formation. This achievement proved sufficient in establishing the feasibility of the operation of the transistor through channel modulation. The confirmed success of multi-layer graphene formation provided a solid foundation, ensuring the viability of transistor functionality and paving the way for the seamless continuation of the subsequent processing steps in the fabrication process. This strategic approach not only aligns with

the research's core objectives but also underscores the meticulous and purposeful decision-making undertaken to advance our understanding of the proposed transistor structure. The Raman spectra presented in Figure 3a,b stand as visual proof of the intricate processes undertaken to validate the material composition and, by extension, the potential success of the transistor structure in achieving the desired operational outcomes.

To substantiate the occurrence of graphene formation on the dielectric material, conducting a direct Raman analysis on the sidewall presented a formidable challenge. The spot size of Raman measurements is relatively large (~μm scale), given that we are verifying the dielectric sidewall as the channel region. Moreover, due to the vertical nature of the channel region, even if a structure is created with a significant slope, both the top electrode and bottom electrode surfaces of Ni and Co are included within the analysis spot. Consequently, the validation process pivoted towards the alternative method of employing current–voltage measurements. The rationale behind opting for the current–voltage measurement method is straightforward and rooted in the fundamental operation of graphene as the channel. As graphene assumes the critical role of facilitating the movement of charges between the source and drain electrodes, it essentially acts as a conduit for this charge flow. Even amidst potential current modulation, the essence remains unaltered—a singular wire in the form of graphene connecting the source and drain electrodes. Expanding upon this, the application of voltage between the source and drain enables us to delve into the intricacies of resistance changes before and after graphene growth. In the nuanced exploration of these resistive alterations, if a reduction in resistance is noted after the growth of graphene, it signifies the emergence of a connecting element between the previously insulated source and drain. This intricate transformation, in which graphene plays a pivotal role, becomes indirectly discernible through the observed decrease in resistance—a subtle yet impactful confirmation of the graphene-induced changes in the connectivity of the source-drain circuit. To determine the channel width, the produced graphene underwent meticulous patterning by means of photolithography. Following this, a voltage spectrum ranging from −0.1 V to 0.1 V was meticulously applied to the top electrode, while the bottom electrode was maintained at 0 V to examine the potential current flow. This confirmation after the completion of graphene patterning serves to mitigate the potential risks associated with the processes involved in defining the channel width. Utilizing photolithography and etching with O_2 plasma to establish the channel width increases the risk of inadvertent damage to the graphene channel. By conducting a post-patterning verification step, we aim to meticulously assess and safeguard against any unintended consequences that may compromise the integrity and functionality of the graphene channel within the semiconductor device.

The absence of current would serve as a key indicator, suggesting either a discontinuity or the non-existence of graphene formation on the sidewall of the dielectric. Contrary to such expectations, the visual representation in Figure 3c confirms the presence of graphene formed on Al_2O_3 10 nm by sweeping the voltage on the drain electrode from −0.1 V to 0.1 V, demonstrating a consistent and linear current flow, unequivocally affirming the existence of graphene on the sidewall. The observable variations in the current values across the fabricated devices, evident in the distinctive red and black graphs within Figure 3c, should also be noted. Such variability stems from the inherent non-uniformity of the graphene layers arising from the intricate process of multi-layer graphene formation. The diversification in the current values underscores the need for precise control and optimization in the fabrication process to achieve a more uniform and consistent graphene structure. Despite these variations, the overarching confirmation of the presence of graphene on the dielectric sidewall adds a layer of assurance to the overall success of the proposed methodology.

Following the meticulous deposition and precise patterning of both the gate insulator and gate electrode, the next crucial step in the experiment involved a thorough verification of the operational characteristics of the device. Figure 4 comprehensively visualizes the operational nuances of the vertical transistor structure as meticulously described and proposed in this study. In the context of graphene-based devices, the intricacies of N/P-type currents form a discernible pattern concerning the Dirac point, creating a distinctive

U-shaped current variation [16]. However, it is crucial to note that the Dirac point's precise location is contingent upon the thickness and doping level of the graphene. This is more complex in devices featuring multi-layer graphene and undergoing multiple processing steps, such as photolithography. In these scenarios, the Dirac point undergoes a substantial rightward shift, resulting in the current modulation manifesting predominantly in one direction [17]. Delving into the specifics of the operational analysis, with a fixed drain voltage at 0.5 V and with the gate voltage ranging from −1 V to 1 V, Figure 4a presents discernible current modulation at approximately 1.4 times, unequivocally confirming the occurrence of modulation. Furthermore, an intriguing revelation surfaces when the drain voltage undergoes a sweeping transition from −0.5 V to 0.5 V on the same device, revealing an additional layer of current modulation. This nuanced observation underscores the significance of the channel's role in the modulation process. Absent modulation due to the channel, the dynamic variations in the current values with fluctuations in the voltage would be notably absent.

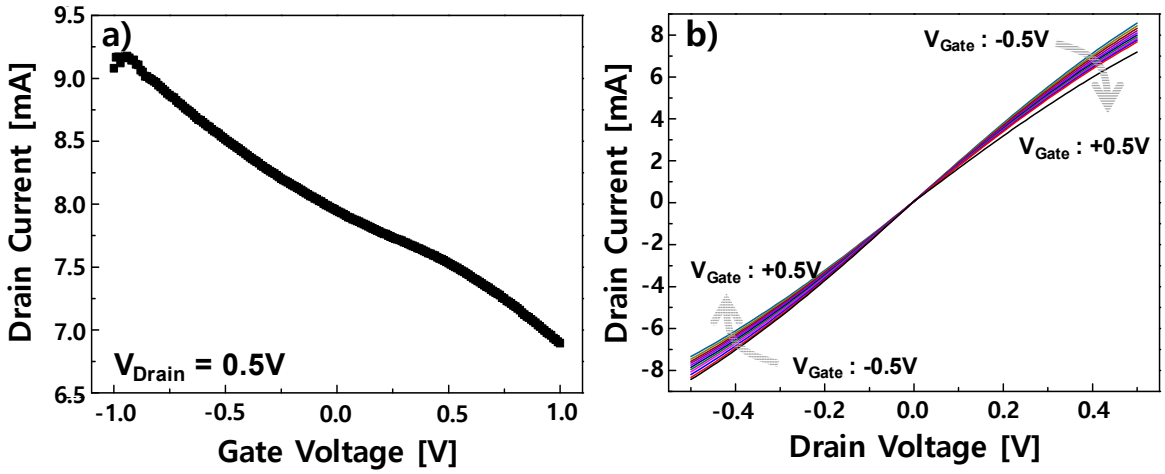

Figure 4. I–V characteristics of channel length determination in a vertical transistor based on the dielectric thickness at room temperature: (**a**) drain current as a function of the gate voltage at V_{Drain} = 0.5 V, and (**b**) as a function of the drain voltage at V_{Gate} −0.5 V~0.5 V.

To verify the practical value of the device structure proposed in this study and the implementation method of the short channel, electrical characteristics of samples were analyzed. Instead of growing graphene directly, graphene grown on Cu was transferred onto the device structure using a wet process to form the channel. Figure 5 illustrates this process. The characteristics of graphene grown on Cu have been confirmed using Raman spectroscopy, and its functionality as a device was validated by measuring IV characteristics, similar to the method described earlier. The reason for conducting this was to confirm the operability of the device structure in this study using graphene. However, graphene is just one option among many 2D materials, and the actual intention was to demonstrate the feasibility of operation by forming the channel through a transfer process, even if various 2D materials are not grown directly. Similar to direct growth, it was shown that this method also achieves the modulation of current by gate voltage, proving that the structure can function as an FET.

Hence, the obtained results provide compelling substantiation that within the intricately designed vertical transistor structure outlined in this study, graphene operates as an exceptionally efficient channel. Mirroring the functionality of a field-effect transistor, these discoveries lay the foundation for a more profound comprehension of the intricate interplay between graphene and the proposed vertical architecture, opening up potential pathways for advancements in semiconductor technology.

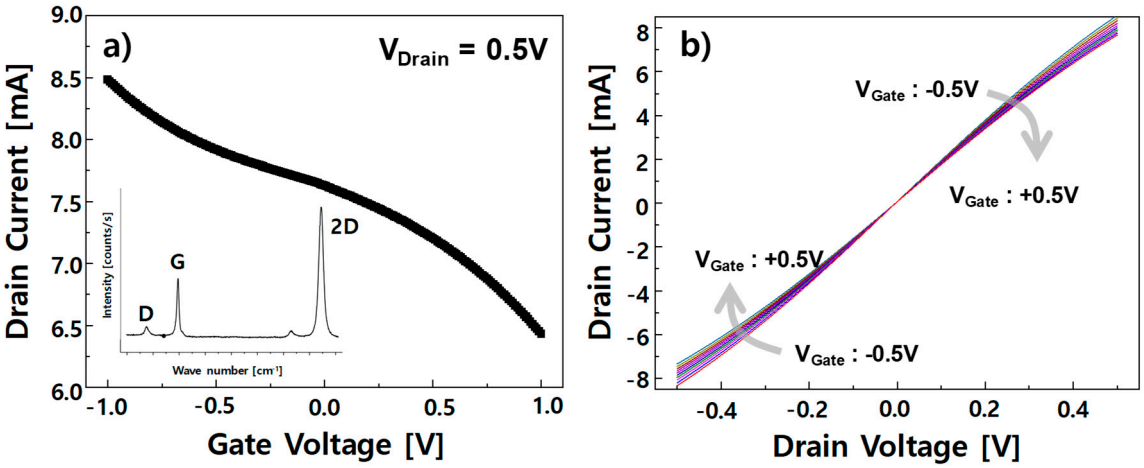

Figure 5. I–V characteristics of channel length determination in a vertical transistor based on the dielectric thickness at room temperature with the graphene transfer method (not direct growth): (**a**) drain current as a function of the gate voltage at V_{Drain} = 0.5 V, and the inset shows the Raman spectrum of Cu growth graphene (**b**) as a function of the drain voltage at V_{Gate} −0.5 V~0.5 V.

4. Discussion

In summary, our research introduces a groundbreaking new paradigm for semiconductor device architecture. This transformative approach leverages the extraordinary properties of graphene, a cutting-edge 2D material, by incorporating it as the channel material in a revolutionary vertical field-effect transistor. This innovative integrated structure not only provides a platform for the seamless adjustment of the channel length, but also triumphs over the inherent limitations of traditional lithography processes, historically hindering efficient integration. This breakthrough opens up unprecedented opportunities for achieving remarkable cost efficiency in semiconductor device manufacturing.

The strategic adoption of a vertical structure, utilizing the sidewall of the dielectric as the channel, not only enhances integration capabilities but also introduces a novel dimension to semiconductor device design. This structure goes beyond simply adopting a vertical configuration for components; it introduces a three-dimensional integration of circuits by allowing electrode input from at least two directions, unlike conventional components that are unidirectional in a top-down manner. This multidirectional input capability enhances the overall integration of the circuit, leading to an improvement in the overall density of the semiconductor system. Additionally, the method proposed in this study for determining the channel length through the dielectric thickness offers advantages in terms of cost-effectiveness by leveraging the existing ALD process. It provides a more straightforward and uniform implementation of a shorter channel length compared to traditional patterning processes. Moreover, the dielectric, a crucial element in constructing the component's structure, plays a significant role. The suggested component structure and processing method, utilizing the dielectric thickness for channel length determination, offer substantial industrial benefits as they eliminate the need for highly challenging process technologies, making them economically advantageous. This innovative configuration promises to reshape the landscape of semiconductor technology, offering improved performance and scalability. By pushing the boundaries of conventional design, we aim to pave the way for the next generation of semiconductor devices. Furthermore, our deliberate choice of utilizing graphene in device fabrication serves as a testament to the immense potential of 2D materials. Beyond their use as mere alternatives to silicon, these materials demonstrate the ability to significantly enhance various characteristics of semiconductor devices. The results of our study not only highlight the feasibility of incorporating 2D materials, but also showcase a pioneering vertical device structure that aligns seamlessly with existing silicon processes, thereby ensuring practicality in real-world applications.

This distinctive aspect sets our research apart from conventional device studies by offering a unique perspective on semiconductor technology. It not only provides compelling evidence for the viability and practicality of harnessing the extraordinary properties of 2D materials, but also sets in motion a transformative evolution of semiconductor devices to unparalleled heights. As we embark on a continued journey to explore and refine these innovative concepts, our work stands as an enduring testament to the promising and exciting future of semiconductor technology. This future is distinctly driven by the thoughtful integration of graphene and other 2D materials into novel device architectures, marking a significant leap forward in the realm of semiconductor advancements.

5. Summary and Conclusions

The structure allows for the easy adjustment of the channel length through the deposition thickness of the dielectric, overcoming the limitations of lithography processes that hinder integration and presenting opportunities for cost efficiency. By implementing a vertical structure that utilizes the sidewall of the dielectric as the channel, we can achieve improved integration. Furthermore, the use of graphene in device fabrication validates the potential of 2D materials as promising alternatives to silicon in enhancing semiconductor device characteristics. The results of this study not only demonstrate the feasibility of utilizing 2D materials and propose a novel vertical device structure, but they also verify the practicality of our approach by utilizing existing Si processes. In this study, graphene has been utilized; however, materials such as hexagonal boron nitride (h-BN) or Molybdenum disulfide (MoS_2) among 2D materials possess excellent electrical properties, and, unlike graphene, have a bandgap. These materials have the potential to be sufficiently utilized in the structure proposed in this study. This sets our research apart from conventional device studies, as it provides valuable evidence for the viability and practicality of utilizing 2D materials in the pursuit of enhanced semiconductor devices.

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