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A 16 Bit 125 MS/s Pipelined Analog-to-Digital Converter with a Digital Foreground Calibration Based on Capacitor Reuse

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Abstract: A 16-bit 125 MS/s pipelined analog-to-digital converter (ADC) implemented in a 0.18 µm CMOS process is presented in this paper. A sample-and-hold amplifier-less (SHA-less) modified 2.5-bit front-end is adopted, which splits the sampling capacitor in half to eliminate the common-mode voltage buffer. The multiplying-digital-to-analog converter (MDAC) in the first pipeline stage is modified by reusing the sampling capacitor in a foreground digital calibration for improving the ADC linearity. This design can circumvent a dedicated reference buffer to generate the calibration voltages at all comparator thresholds. By calibrating the ADC in the digital domain, the integral non-linearity (INL) is improved from −9.2/10 LSB to −3/2.2 LSB, and the spurious-free dynamic range (SFDR) is optimized by over 8dB. The ADC consumes 154mW (reference buffer and clock included) from a 1.8 V supply.

Keywords: analog–digital conversion; pipeline processing; foreground calibration; capacitor reuse; SHA-less

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1. Introduction

The boom of the wireless communication is driving the world into a ubiquitous information exchange environment, which strongly calls for high speed and high resolution analog-to-digital converters (ADCs). Pipelined ADC architectures outperform others for their better trade-off between speed and resolution [1]. However, as a CMOS device enters the nanoscale region, a mismatch between the capacitors in DACs (digital-to-analog converters) could severely degrade the linearity of a pipelined ADC. To tackle the problems mentioned above, some papers have reported approaches in the analog domain, which has suffered a lot from low power budgets and area overheads [2–4]. In [5–8], an additional calibration RDAC was introduced to extract the capacitor mismatch error of ADCs, store the error information in the RAM, and then quantize compensation. The extra analog circuits consume a lot of on-chip resources and a large area. In addition, the analog calibration is strictly limited by the ADC architecture because of its poor compatibility [9]. As a result, calibration techniques that detect and compensate for errors in the analog domain have been gradually replaced over time.

Recently, numerous researchers have investigated digital calibration techniques [10–17], since the scaling of CMOS device dimensions offers clear advantages for digital circuitry in terms of area, speed, and integration. According to whether the ADC is calibrated in real time, digital calibration technology is divided into foreground calibration and background calibration. Background calibration refers to when the ADC is calibrated while working, but it takes a period of time to converge. The algorithms reported in [18,19] have quite a

fast convergence speed; however, they are ineffective at certain frequencies and can even deteriorate the ADC performance due to its own defects, whereas the digital background calibration algorithms in [20–25] do require the external input injection, such as a pseudo-random (PN) noise sequence [20–23] and sinusoidal signals [24] for calibration, which typically have convergence speeds in the order of approximately 10^6 to 10^8 cycles [20–23], 10^5 cycles, and 10^4 cycles [25]. Compared with the background calibration, the foreground one is much more reliable. Once powered on, the ADC is calibrated first. After calibration, the error code is usually stored in a one-time-programmable (OTP) or electronic fuse (Efuse) module. Furthermore, it is important to note that a calibrated ADC avoids the convergence time while working, so the ideal output can be obtained quickly.

This paper describes a digital foreground calibration technique based on the capacitor reuse to estimate the mismatch between capacitors in MDAC. The first two stages employ a modified MDAC, whose sampling capacitors are separated from the sub-DAC. In the calibration mode, one of the sampling capacitors is utilized to generate an equivalent calibration voltage of $\pm\frac{1}{8}V_{ref}$ and estimate the error code caused by capacitor mismatch. Reusing the capacitor in MDAC can eliminate the requirement for a dedicated reference buffer to generate the calibration voltage at all threshold voltages, thereby minimizing the chip size and significantly reducing the power consumption. Furthermore, the separated MDAC not only realizes the calibration target, but also eliminates the kickback effect on the input signal and reference buffer. In addition, we split the sampling capacitor in half to avoid the use of a common-mode voltage buffer. In this way, the power and area requirement can be relaxed further.

The paper is organized as follows: Section 2 describes the effect of a mismatched ADC output performance of the capacitor array in an MDAC. Section 3 introduces the pipeline ADC proposed by SHA-less type, including the structural principle of the improved MDAC capacitor array, the performance analysis, and the calibration algorithm principle based on the improved MDAC. Section 4 shows the results of the calibration algorithm based on a 180 nm process verification, and Section 5 provides the conclusion.

2. Capacitor Mismatch in MDAC

A traditional 2.5-bit MDAC is depicted in Figure 1a. For simplicity, only half of the differential implementation is shown. Ideally, all of the capacitors are equal to 2C under perfect matching. C is the unit capacitor of the MDAC, and the interstage gain is 4. The amplifier output can be expressed as follows:

$$V_o = V_{in} \times \frac{C_T}{C_F} - V_{ref} \times \frac{\sum (C_{V_{RP}} - C_{V_{RN}})}{C_F} \tag{1}$$

where C_T is the total capacitance of the sampling capacitor, C_i is the ith capacitor of the MDAC, C_F is the feedback capacitor, and V_{ref} is the reference voltage of the ADC which is equal to $V_{RP} - V_{RN}$. In Equation (1), the term with the footnote V_{RP} (V_{RN}) means the capacitor connecting to V_{RP} (V_{RN}).

Nevertheless, after the tape-out process, the capacitors in MDAC differ from each other due to the mismatch. Assuming that ΔC_i is the deviation from an ideal capacitor C_i, then Equation (1) can be rewritten as follows [2]:

$$V_o = V_{in} \times \left(4 + \frac{\sum \Delta C_i}{C_F}\right) - V_{ref} \times \frac{\sum (C + \Delta C_i)_{V_{RP}}}{C_F} + V_{ref} \times \frac{\sum (C + \Delta C_i)_{V_{RN}}}{C_F} \tag{2}$$

where 4 is the interstage gain of the 2.5-bit MDAC.

Figure 1b shows the transfer curve. The deviation (black dotted line) from the ideal case (red solid line) can be seen from the plot in Figure 1b. Then, the residue voltage in Equation (2) is processed by the back-end pipelined stages. To observe the mismatch effect on the ADC output code, the same V_{in} is quantized by the adjacent residue transfer curve in

the neighbored subranges. The shifting voltage ΔV and the error voltage V_{err} at comparator thresholds can be expressed as follows:

$$\Delta V = \left(1 + \frac{\Delta C_i}{C_F}\right) \times V_{ref}, \tag{3}$$

$$V_{err} = \frac{\Delta C_i}{C_F} \times V_{ref}. \tag{4}$$

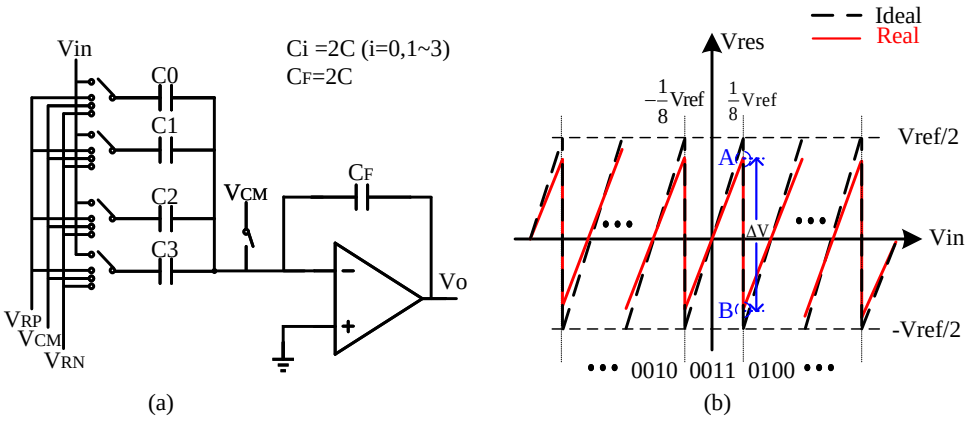


Figure 1. Traditional 2.5-bit MDAC (**a**) and its transfer curve in the first stage (**b**).

The output results of the ADC are depicted in Figure 2. Obviously, there are many "jumps" at each of the two adjacent subranges. Attention should be paid when $V_{err} < 0$ because the missing code decreases the ADC performance greatly [26]. Thus, if the V_{err} can be measured and compensated for in a certain way, we can eliminate the nonlinearity caused by capacitor mismatch.

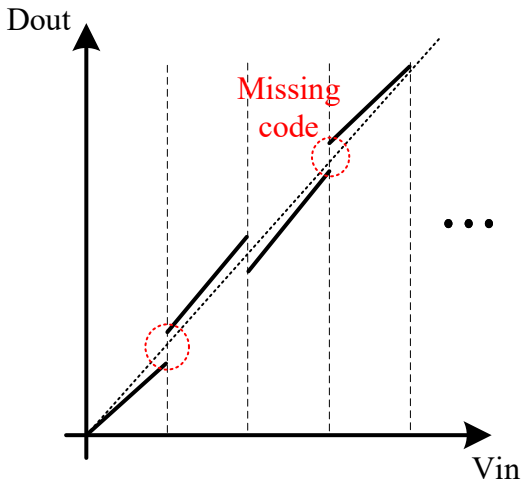


Figure 2. The output results of the pipelined ADC with capacitor mismatch.

3. Proposed 16 Bit SHA-Less Pipelined ADC

The implementation of the proposed pipelined ADC is shown in Figure 3. The pipelined ADC is SHA-less, where the sample-and-hold circuit is integrated with the first-stage MDAC. Taking the power and noise into consideration, the first three stages resolve 2.5 bits, which is then followed by eight stages with 1.5-bit/stage and a 3-bit back-end flash ADC. After that, all the stage output bits are sent to the digital bit alignment block. Furthermore, the capacitor mismatches in first and second stages need to be calibrated for a desired linearity.

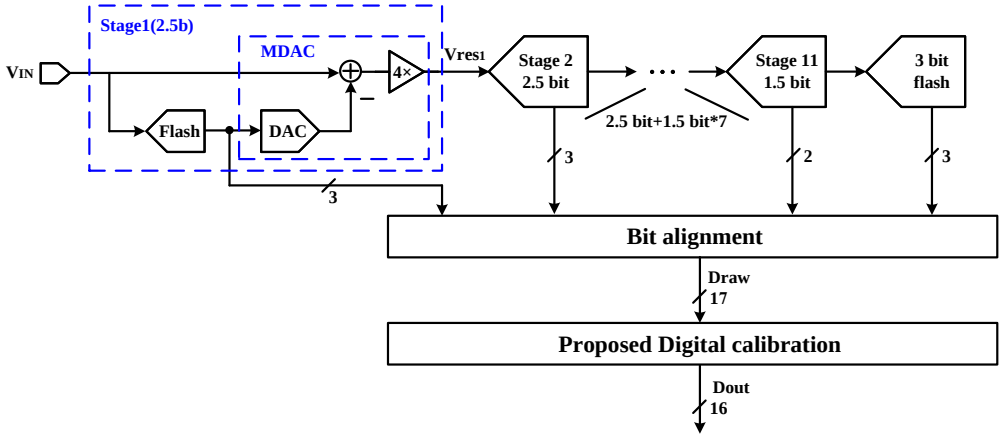


Figure 3. Proposed 16 bit SHA-less pipelined ADC architecture.

As the diagram shows, all the 17 bits codes obtained from each stage are fed to the digital module to reconstruct the digital output. Here, an extra bit obtained from the pipelined stages is used for decreasing the quantization noise. After that, for a higher linearity, the proposed digital foreground calibration is employed.

3.1. Modified MDAC in the First Stage

The 2.5-bit MDAC we propose is shown in Figure 4. Compared with the traditional one in Figure 1a, we separate the sampling capacitors C_{si} (i = 0, 1. . . 7) from the sub-DAC capacitors.

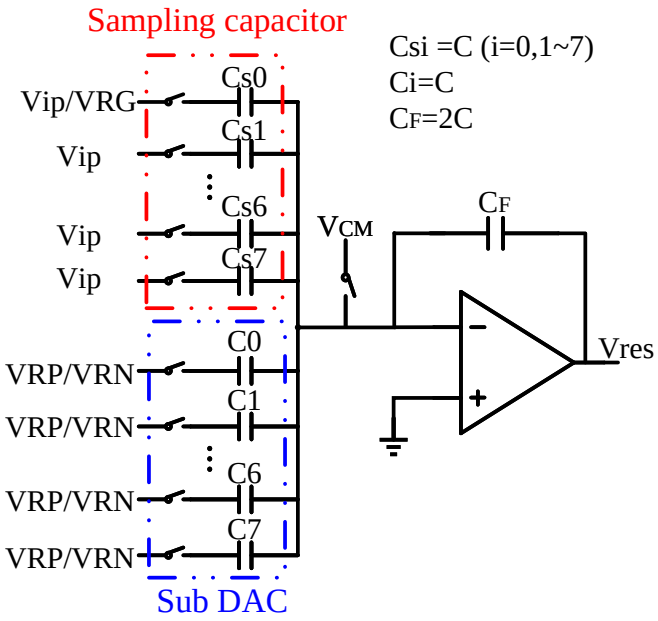


Figure 4. Modified MDAC in the first stage.

This study adopted the bottom plate sampling technique. Under a normal conversion mode, in the sampling phase, for example, $\varphi 1$, the differential input voltage is sampled to the bottom plates of the MDAC. For simplicity, only the single-ended structure is display here. As shown here in Figure 5a, all the top plate of the capacitors in MDAC are applied to a common-mode voltage V_{CM}, whereas for the bottom plate, the situation is different. The input voltage Vip is supplied to the sampling capacitors C_{si} (i = 0, 1,. . . 7), while the V_{RP} and V_{RN} are connected to C_i (i = 0∼3) and C_i (i = 4∼7) in sub-DAC, respectively. At the same time, the output of the opamp is switched to the output common-mode voltage $V_{out,cm}$.

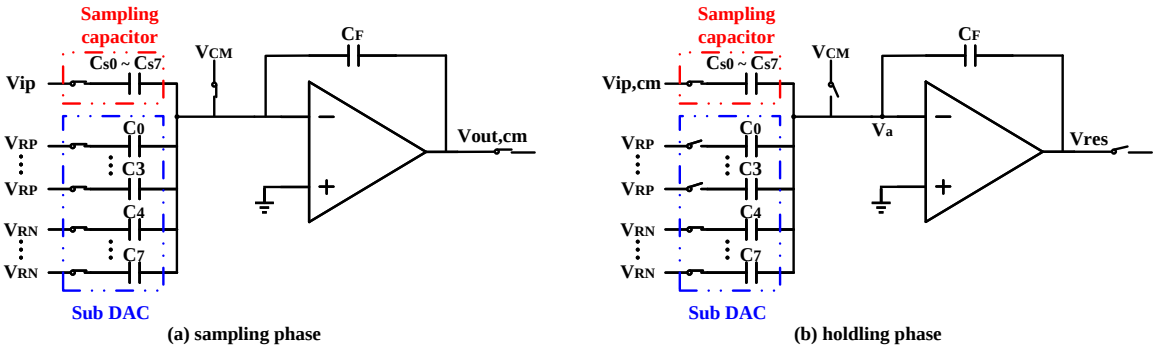


Figure 5. In a normal conversion mode, the switching method of the modified MDAC in the sampling phase $\varphi 1$ (**a**) and holding phase $\varphi 2$ (**b**). The two clock phases $\varphi 1$ and $\varphi 2$ are non-overlapping.

By switching the capacitor array in phase $\varphi 1$, the differential charge sampled on the capacitors can be expressed as Equation (5):

$$Q_1 = (V_{ip} - V_{in}) \times \sum_{i=0}^{7} C_{si}, \tag{5}$$

where $V_{IN} = V_{ip} - V_{in}, V_{ref} = V_{RP} - V_{RN}$. In the holding phase $\varphi 2$ shown in Figure 5b, the top plate is open from V_{CM}. The input voltage is changed to a stable-input common-mode voltage $V_{IN,cm}$. For the capacitors in a sub-DAC, C_i (i = 0∼7) are switched to V_{RN} or V_{RP} according to the comparator results $D(i)$. When $D(i)$ = 1, C_i is switched to V_{RN}; otherwise, C_i is switched to V_{RP}. Therefore, the charge in holding phase $\varphi 2$ can be expressed as Equation (6):

$$\begin{aligned} Q_2 &= (V_{RP} - V_{RN}) \times \sum_{i=0}^{7} C_i[1 - 2D(i)] - V_{res} \times C_F \\ &= V_{ref} \times \sum_{i=0}^{7} C_i[1 - 2D(i)] - V_{res} \times C_F. \end{aligned} \tag{6}$$

C_F is the feedback capacitor of the MDAC, which is equal to 2C. As the result of charge conservation, Q_1 equals Q_2. Finally, the transfer function of the modified MDAC can be obtained:

$$V_{res} = \frac{C_T}{C_F}\left[V_{IN} - \frac{\sum_{i=0}^{7}(2D(i) - 1) \times C_i}{C_T} \times V_{ref}\right], \tag{7}$$

where C_T refers to the total capacitance of sampling capacitor; $C_i = C + \Delta C_i$.

The use of separated sampling capacitors offers many advantages over the reuse of a sub-DAC to process the sampling and quantization. Firstly, there is no charge redistribution on C_s in the holding phase, which, avoiding the reset pulse before C_s, goes back to track. Secondly, the kickback effect of a charge glitch on a reference buffer is decreased [27]. Furthermore, the structure for splitting the unit capacitor in half is free from the common-mode voltage buffer compared with the conventional one.

Based on the modified MDAC, reusing 1/8 of the sampling capacitors (e.g., C_{s0}) as the assistant capacitor in the calibration mode can also generate a calibration voltage ($\pm\frac{1}{8}V_{ref}$) without an extra circuit implementation. Cooperating with the switching scheme mentioned later, all the capacitor mismatches in a sub-DAC can be calibrated in the absence of the dedicated reference buffer, which relaxes the area and power overhead greatly.

3.2. Calibration Technique

In practice, owing to the interstage gain of the pipelined ADC, the mismatches of the back-end stages can be neglected. Here, we choose the first two stages for calibration. Once the ADC is powered on, the calibration process starts. The first two stages' amplifiers are

shown in Figure 6 for a single-ended implementation. Without any hardware costs, C_{s0} in MDAC1 is reused directly to generate the threshold voltages in the first stage of calibration. A capacitor C_{cal} is regarded as the unique assistant capacitor when calibrating in stage2.

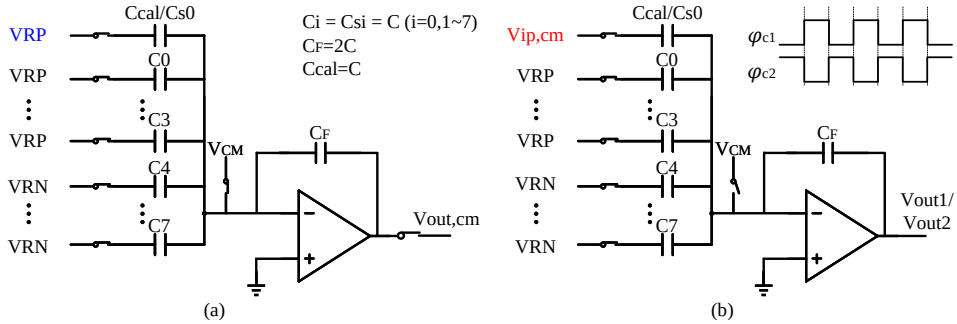


Figure 6. The first two stages' amplifier in a calibration mode to generate the calibration voltage $\frac{1}{2}V_{ref}$; (**a**) sampling phase φc1, (**b**) holding phase φc2.

As shown in Figure 6, when calibrating stage1, the capacitors C_i(i = 0, 1...7) are switched to "00001111" in sampling phase φc1, meaning that the capacitors C_0~C_3 are switched to V_{RP} and the capacitors C_4~C_7 are switched to V_{RN}. It is equivalent to connecting the input of stage1 to GND. After that, V_{RP} is applied to the reused capacitor C_{s0}, where C_{s0} = C. All the top plate are connected to V_{CM}. Quantitatively, the charge Q_{c1} sampled differentially in phase φc1 can be represented as follows:

$$Q_{c1} = (V_{RP} - V_{RN}) \times C_{S0} + (V_{RP} - V_{RN}) \times \sum_{i=0}^{3} C_i - (V_{RP} - V_{RN}) \times \sum_{i=4}^{7} C_i. \quad (8)$$

In the holding phase φc2, C_{s0} is open from V_{RP}. Furthermore, the top plate is open from V_{CM}. Thus, the charge accumulated on C_{s0} is redistributed later. The charge at this time can be expressed as follows:

$$Q_{c2} = (V_{RP} - V_{RN}) \times \sum_{i=0}^{3} C_i - (V_{RP} - V_{RN}) \times \sum_{i=4}^{7} C_i + Vout1 \times C_F. \quad (9)$$

Due to the charge conservation, $Q_{c1} = Q_{c2}$. So, it can be derived as follows:

$$(V_{RP} - V_{RN}) \times C_{S0} = Vout1 \times C_F, \quad (10)$$

$$Vout1 = \frac{1}{2}V_{ref}. \quad (11)$$

With an interstage gain of 4, an equivalent calibration voltage of $\frac{1}{8}V_{ref}$ at the input is consequently generated. The ideal output voltage is $\frac{1}{2}V_{ref}$. Nevertheless, as Figure 3 shows, the mismatch between C_i and C_F shifts the output voltage from $\frac{1}{2}V_{ref}$ to point A in Figure 1b. After being processed in the following stages, an equivalent input voltage of $\frac{1}{8}V_{ref}$ can be quantized as Dout1 (17 bits).

Then, switching C_4 from V_{RN} to V_{RP} as Figure 7 shows, the charge in the sampling phase φc1 is the same as that expressed in Equation (8), while in the holding phase φc2, the charge can be expressed as follows:

$$Q_{c3} = (V_{RP} - V_{RN}) \times \sum_{i=0}^{4} C_i - (V_{RP} - V_{RN}) \times \sum_{i=5}^{7} C_i + Vout2 \times C_F. \quad (12)$$

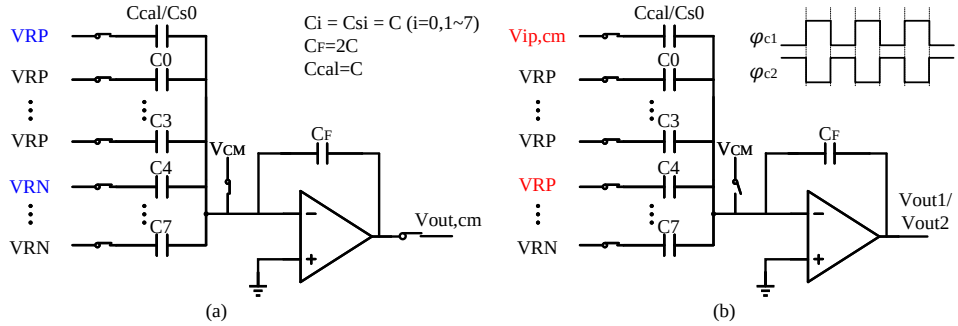


Figure 7. The first two stages' amplifier in calibration mode to estimate the C4 error code: (**a**) sampling phase φc1, (**b**) holding phase φc2.

Vout2 can be derived as follows:

$$Vout2 = \frac{1}{2}V_{ref} - 2\frac{C_4}{C_F}V_{ref}. \tag{13}$$

Taking the mismatch of C_4 into consideration, Equation (13) can be rewritten as follows:

$$Vout2 = \frac{1}{2}V_{ref} - \frac{C + \Delta C_4}{C}V_{ref}. \tag{14}$$

For the same V_{in}, it is quantized by an adjacent subrange (0100) in the transfer curve. Finally, we can obtain Dout2 (the same Vin with the error information of C_4 after quantization) in the same way. Dout2 refers to point B in Figure 1. Subtracting Dout2 from Dout1 via a digital circuit, the error introduced by the capacitor mismatch in stage1 is digitized. The error of C_4 can be expressed as follows:

$$err(4) = \frac{\Delta C_4}{C}V_{ref}. \tag{15}$$

To filter the noise, a 512-point averaging filter is employed after repeating the quantization 512 times.

Instead of generating all the threshold voltages at once, the error code is calculated by switching the capacitors C_i one by one. The weights of C_i are the same. Combining this with the switching method in Table 1, we can move all the threshold voltages to $\frac{1}{8}V_{ref}$ or $-\frac{1}{8}V_{ref}$ without any calibration voltage generation circuits. Then, the error of C_5~C_7 is shown in Table 1. For C_0~C_3, switch C_{cal} to V_{RN} to generate an equivalent input voltage of $-\frac{1}{8}V_{ref}$ in the sampling phase φc1. Hence, according to the aforementioned switching method (presented in Table 1), the error code of C_0~C_3 can be calculated in turn.

Table 1. Switching method to calculate the error(i) caused by a capacitor mismatch.

	Err(i)	C_i Switch to V_{RP}	C_i Switch to V_{RN}	Capacitor Switched Code of C_7-C_0
	0	1~3	0, 4~7	00001110
	1	0, 2~3	1, 4~7	00001101
	2	0~1, 3	2, 4~7	00001011
i=	3	0~2	3~7	00000111
	4	0~4	5~7	00011111
	5	0~3, 5	4, 6~7	00101111
	6	0~3, 6	4~5, 7	01001111
	7	0~3, 7	4~6	10001111

When calibrating stage2, a capacitor C_{cal} is introduced as an assistant capacitor to yield the desired threshold voltages. In the sampling phase, C_{cal} is connected to V_{RP} or V_{RN}, respectively. Therefore, the equivalent input voltage of $\frac{1}{8}V_{ref}$ or $-\frac{1}{8}V_{ref}$ can be injected

the same way as in stage1. The error code caused by the capacitor mismatch of stage2 is obtained by an approach similar to that of stage1 and according to the capacitor switching method shown in Table 1. As the flowchart in Figure 8 depicts, the calibration starts with stage2 because it is applied to digitize the residue voltage of stage1 when estimating the error code of stage1.

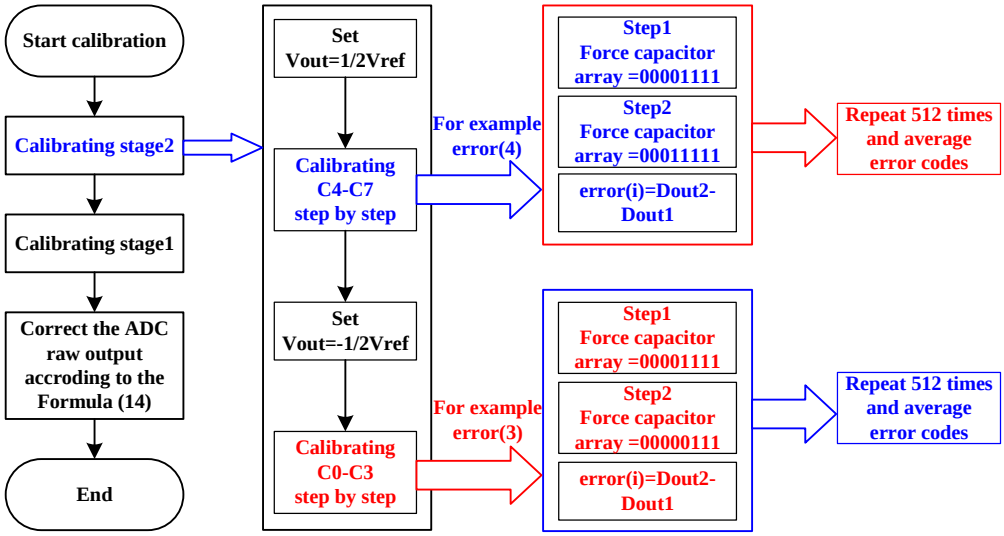


Figure 8. The flowchart of the proposed calibration.

Once the error code of stage1 and stage2 is evaluated, it is stored in memory until the normal conversion mode. According to the output code of the first two stages, the compensation is made for the original ADC output D_{raw}, as expressed in Equation (16):

$$D_{out} = D_{raw} + \sum_{i=0}^{3}(D_1(i) - 1) \times err_1(i) + \sum_{i=4}^{7}(D_1(i)) \times err_1(i) + \sum_{i=0}^{3}(D_2(i) - 1) \times err_2(i) + \sum_{i=4}^{7}(D_2(i)) \times err_2(i), \quad (16)$$

where $D(i)$ is the comparison result of the ith capacitor, $D(i)$ = 0 or 1, and err(i) is the compensation code calculated in the calibration mode. Footnote 1 in $D_1(i)$ refers to the first stage. The assistant capacitor for calibration slightly decreases the amplifier feedback factor, thus leading to a small overhead of amplifier design. However, the advantages of the proposed calibration method by far exceed the shortcomings.

4. Measurement Results

A 16 bit SHA-less pipelined ADC with a digital foreground calibration was verified in a 0.18 µm CMOS process. The layout is illustrated in Figure 9. It occupies an area of 1030 µm × 2125 µm. As shown in Figure 10, differential and integral non-linearity (DNL and INL) before calibration are in the range of −0.7/1.1 LSB and −9.2/10 LSB, which are improved to −0.87/0.82 LSB and −3/2.2 LSB, respectively. Figure 11 shows the FFT spectrum of the ADC with and without calibration while sampling a 30.5 MHz input signal with an amplitude of −2 dBFS at 40 MS/s. In addition, Figure 12a shows a plot of the dynamic performances, which depict the SNDR (signal-to-noise-plus-distortion ratio) and SFDR versus the sampling rates. Furthermore, Figure 12b shows the THD (Total Harmonic Distortion) characteristics. The results show, with the help of calibration, that the SFDR can even achieve about an 8 dB improvement at some frequency. A degradation of SFDR at a higher sampling frequency mainly originates from the imperfect settling of the ADC. The ADC consumes 154 mW of total power (reference buffer and clock included) when operating at a 1.8 V supply. The measured results are summarized in Table 2.

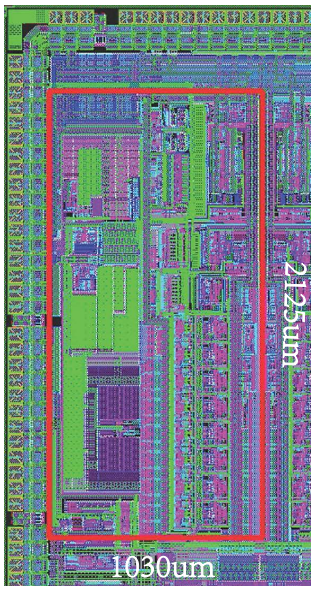


Figure 9. The layout of the ADC.

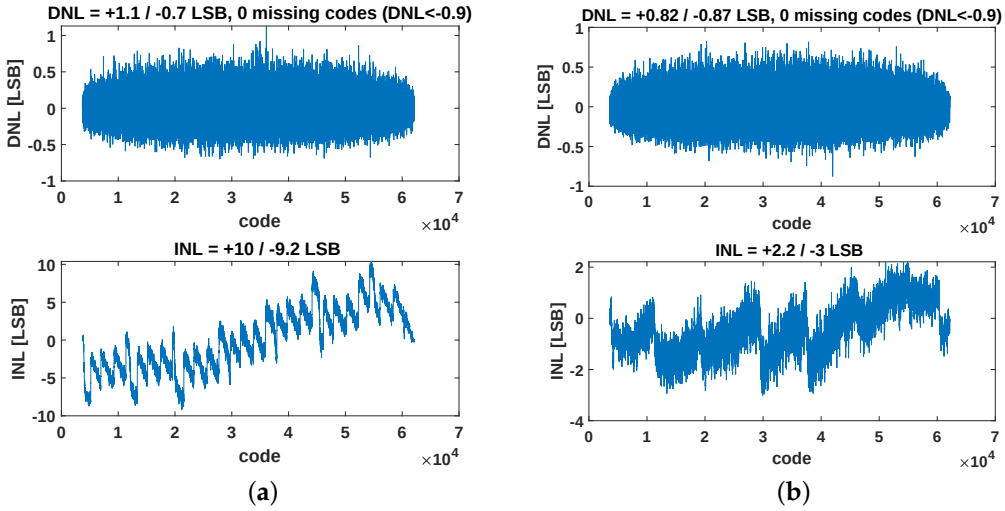


Figure 10. Measured DNL and INL of the ADC. Before (**a**) and after calibration (**b**).

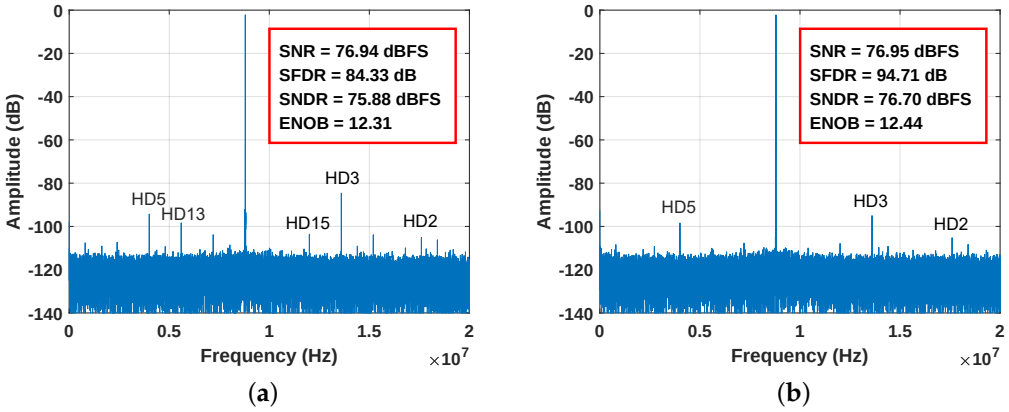
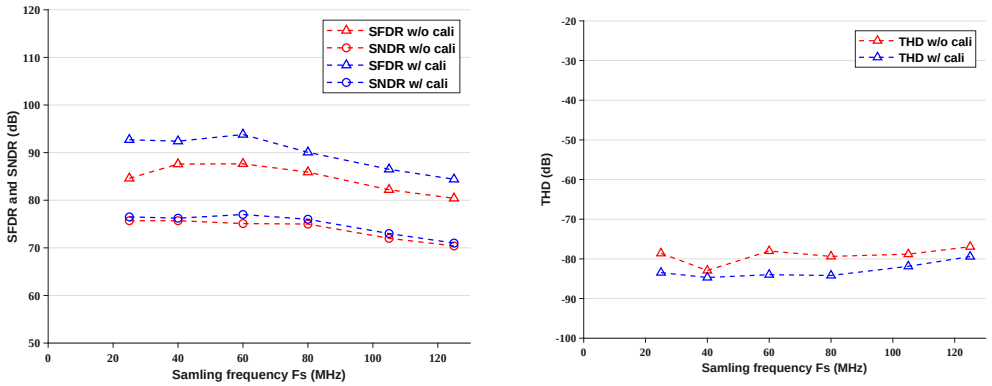


Figure 11. Measured spectrum of the ADC output at 40 MS/s for an input frequency of 30.5 MHz at −2 dBFS. Before (**a**) and after calibration (**b**).



(**a**) (**b**)

Figure 12. Measured dynamic performances at a 10.5MHz input signal frequency with and without calibration. SFDR and SNDR (**a**) and THD (**b**).

Table 2. Performance comparison with state-of-the-art ADCs.

Specification	[10]	[11]	[14] [1]	This Work
Process (nm)	180	180	180	180
Fs (MHz)	125	250	125	125
Resolution (Bits)	16	14	16	16
SFDR (dBFS)	92	87.9	90.7	94.7
SNDR (dBFS)	78.6	68.2	79.5	76.7
DNL/INL (LSBs)	0.6/3.0	0.15/1	-/-	0.8/3.0
Power (mW)	385	300	58.6 [2]	154
Area (mm^2)	6	6	-	2.19

[1] Simulation results. [2] The power of front-end stages.

Table 2 compares the proposed ADC with several pipelined ADCs using different calibration techniques reported recently. As shown in the table, other methods are based on dithering or others, which need a large area and power consumption. The proposed calibration method achieves better performance with both a lower power budget and less circuit complexity. More specifically, the proposed foreground calibration approach achieves a significant reduction in power consumption by half, while simultaneously attaining a threefold decrease in area, owing to getting rid of the dedicated buffer to generate the calibration voltage. Furthermore, the SFDR of the ADC is comparable to the best results in [10], which is mainly because of the modified MADC and the proposed calibration technique.

5. Conclusions

In this brief, a 16 bit SHA-less 125 MS/s 0.18 μm CMOS pipelined ADC with a digital foreground calibration based on capacitor reuse is presented. Combined with the modified MDAC in the first stage, no extra circuit is required except for one assistant capacitor in the second stage during the calibration mode. We avoid a common-mode voltage buffer by splitting the sampling capacitors in half, which saves the area and power overheads. The measurement results show that the proposed calibration method significantly improves the ADC performance, especially for SFDR.

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