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A 500 mV_{pp} Input Range First-Order VCO-Based ADC with a Multi-Phase Quantizer for EEG Recording Front Ends

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Abstract: This paper proposes a VCO-based ADC with first-order noise shaping for EEG signal recording front ends. Addressing the challenge of applying analog integrators in advanced processes due to low voltage issues, a multi-phase quantizer structure is introduced based on V-F conversion within the VCO structure, resulting in lower analog power consumption at the same output bit-width. By introducing a form of Gray code encoding, errors caused by circuit metastability are limited to within 1 bit. Considering the effects of motion artifacts and the electrode DC offset, the circuit achieves a wide input range of 500 mV_{pp} by adjusting the feedback coefficients. A prototype ADC is fabricated using 180 nm CMOS technology, operating at a 1.8 V/1 V power supply voltage, with power consumption of 17.1 µW, while achieving a 62.1 dB signal-to-noise and distortion ratio (SNDR) and 55.2 dB dynamic range (DR). The proposed ADC exhibits input noise of 8.64 µV_{rms} within a bandwidth of 0.5 Hz–5 kHz.

Keywords: EEG signal; first-order noise shaping; large input range; multi-phase quantizer; VCO-based ADC

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1. Introduction

In modern clinical practice, EEG signals are obtained by measuring the scalp electrical potential at multiple locations on the head to reflect the spontaneous electrical activity in the brain [1]. Meanwhile, scalp EEG measurement, as a non-invasive method, has played an important role in measuring and assessing brain diseases, including epileptic seizures and Alzheimer's disease, as well as sleep disorders [2]. In brain–computer interface (BCI) systems, EEG recording circuits capture information about the brain by capturing the strength and spatial distribution of the electrical potentials at different locations in the brain. Compared to invasive methods, which carry the risk of trauma, non-invasive EEG recording circuits face greater challenges due to the electrode DC offset (EDO) and motion artifacts (MA), which can affect the accuracy of the recordings [3].

Currently, there are two main approaches to non-invasive EEG recording circuits. In one, each channel is composed of a low-noise instrumentation amplifier (IA) and a medium-accuracy analog-to-digital converter (ADC) [3–13], as shown in Figure 1. This method can obtain relatively low input reference noise (IRN) and superior common mode rejection ratio (CMRR) performance. However, MA and EDO on the mV scale tend to saturate the front-end amplifier, limiting the gain of the front-end amplifier. To reduce the impact of EDO, amplifiers usually require large external capacitors or additional DC servo loops (DSL) [14–16]. This approach increases the chip area and power consumption and limits the miniaturization of EEG recording circuits. Another approach is to use the ADC direct structure [17–20], combine the IA and ADC functions, and directly digitize the input EEG signals. This is commonly achieved using discrete-time (DT) or continuous-time (CT) ΔΣ

ADC architectures, allowing for a relatively high signal-to-noise and distortion ratio (SNDR). However, this structure faces challenges due to its heavy reliance on voltage-domain-based integrators and comparators, which are sensitive to process scaling. Additionally, suppressing kT/c noise in DT structures or maintaining the linearity of the G_m-C filter in CT structures is often required [21].

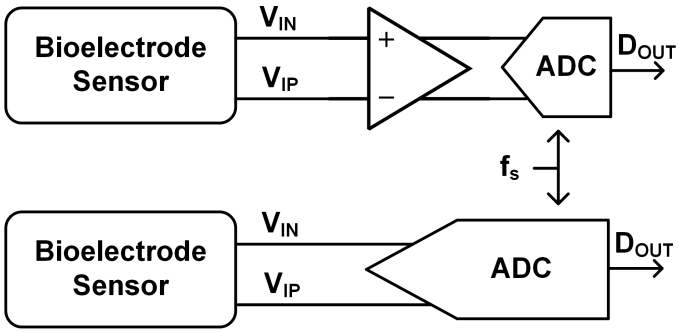

Figure 1. The implementation method of an EEG recording circuit.

To overcome the limitations of traditional voltage domain processing in advanced technology nodes, the EEG recording circuit topology based on a voltage-controlled oscillator (VCO) directly converts the input voltage to the frequency domain, thus avoiding the constraints imposed by the power supply voltage [22–26]. The frequency output of the VCO is quantized by measuring the phase increment over a specific time window. At the same time, VCO-based circuits do not need to stack transistors like traditional analog amplifiers to achieve unlimited DC gain. Although the VCO-based structure offers a high level of digitization, the analog components, particularly the VCO circuit, still account for a significant portion of the overall circuit's power consumption.

This paper proposes a digital circuit structure with multiple quantizers, which reduces the center frequency f_c of the VCO in the analog circuit to 1/2 N, achieving a significant reduction in the power consumption of the analog VCO circuit with the same output bit resolution. By introducing a form of Gray code encoding, the errors caused by circuit metastability are limited to within 1 bit. By adjusting the feedback coefficients to constrain the residual signal to within 10 mV, the circuit achieves a wide input range of 500 mV_{pp}. The overall circuit is highly digitized, and a first-order noise shaping effect is achieved using digital differential circuits.

This paper provides a comprehensive description of the architecture and theory of the circuit, as well as the details of its implementation and measurement. The content is structured as follows. Section 2 provides a detailed description of the principle analysis and implementation status of the proposed circuit. Section 3 introduces the measurement results and analysis and compares the performance with other works. Finally, Section 4 concludes the paper.

2. Circuit Design

2.1. V/I Conversion Circuit

The VCO can convert the input analog voltage into a corresponding frequency or phase signal, as shown in Figure 2. The mathematical model is equivalent to a CT voltage phase integrator with an infinite DC gain. In the specific circuit implementation, a VCO-based ADC can be achieved with a combination of digital circuits and simple analog circuits. It replaces the traditional, predominantly analog integrators and comparators, performing integration and quantization in the phase or frequency domain. Despite the high scalability of VCO-based ADC structures, the nonlinearity introduced during the V-F conversion process by the VCO is one of the key factors affecting the performance.

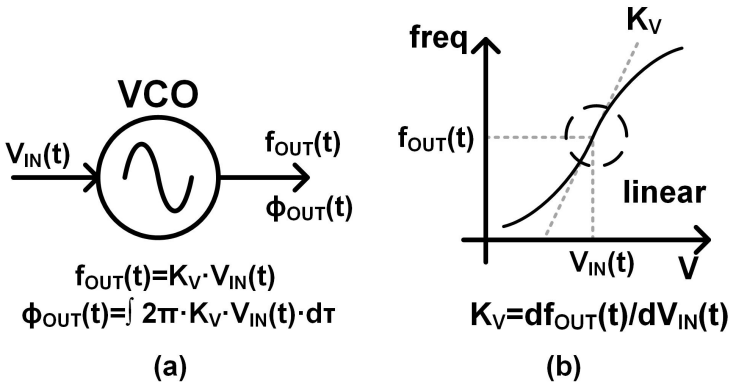

Figure 2. (**a**) VCO conversion. (**b**) Nonlinearity of the VCO.

For a current-starved VCO composed of N stages of inverters, its K_{VCO} can be expressed as follows:

$$K_{VCO} = \frac{G_m}{N * C * VDD_{CCO}} \tag{1}$$

where C represents the parasitic capacitance of the VCO composed of inverters, which is associated with the WL of the inverter. VDD_{CCO} denotes the output voltage swing of the current-starved VCO. G_m denotes the transconductance of the input V/I circuit. G_m is not a linear quantity. As the input voltage varies, the state of the MOS transistor changes. There are two methods to improve the linearity of the transconductance G_m. The first method involves operating the entire circuit in a closed loop, adjusting the feedback coefficient, and controlling the ratio of C_{DAC} to C_{IN} to reduce the amplitude of the summed input to several millivolts. The second method is to improve the linearity of the V/I circuit.

As shown in Figure 3, the VCO-based ADC front end consists of a V/I converter composed of differential pairs M1 and M2 and a set of current-starved voltage-controlled oscillators (CCOs). To enhance the linearity of the differential pairs, a source degeneration structure with a resistor R_S is employed, resulting in the following gain of the V/I converter:

$$G_{mR} = \frac{G_m}{1 + g_m * R_S} \approx \frac{1}{R_S} \tag{2}$$

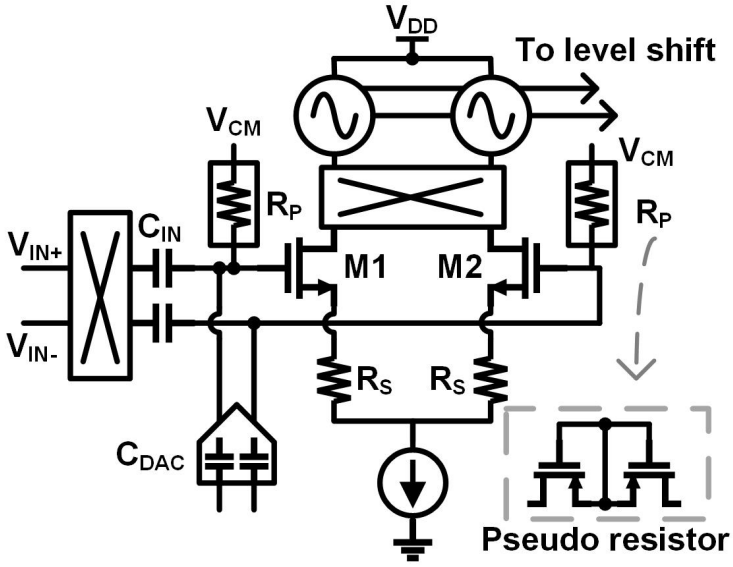

Figure 3. Schematic diagram of V/I conversion circuit.

The linearity of the V/I conversion is enhanced by employing the source degeneration structure. To achieve current multiplexing and improve the current efficiency, the V/I conversion circuit is stacked with 16 pairs of CCOs. The frequency range of the EEG signal distribution is typically 0.5–100 Hz, which requires the high-pass filter (HPF) cutoff frequency composed of the input capacitor C_{IN} and the bias resistor R_p to be below 0.5 Hz. To achieve resistance of tens of GΩ, the input of the V/I conversion is biased by a pseudo-resistance composed of an MOS transistor. The amplitude of the summed input at the input terminal of the V/I circuit is kept within 10 mV by adjusting the feedback coefficient. This approach not only ensures that the MOS transistors remain in saturation but also minimizes the input swing, thereby maintaining the pseudo-resistor at a high level and effectively reducing the impact of noise originating from the pseudo-resistor. To avoid a gate leakage current, thick oxide transistors are used for the differential pairs M1 and M2. Furthermore, chopper techniques are used to reduce the IRN.

Figure 4a shows the implementation of the CCO circuit, where each delay cell comprises an inverter pair and two cross-coupled PMOS transistors, effectively reducing flicker noise. Regarding the phase noise of VCO, it is negligible when equivalent to the input. Due to the CCOs being stacked on the differential pair, the output waveform amplitude remains relatively small. Therefore, a level shifter is required to achieve a rail-to-rail output waveform, as shown in Figure 4b.

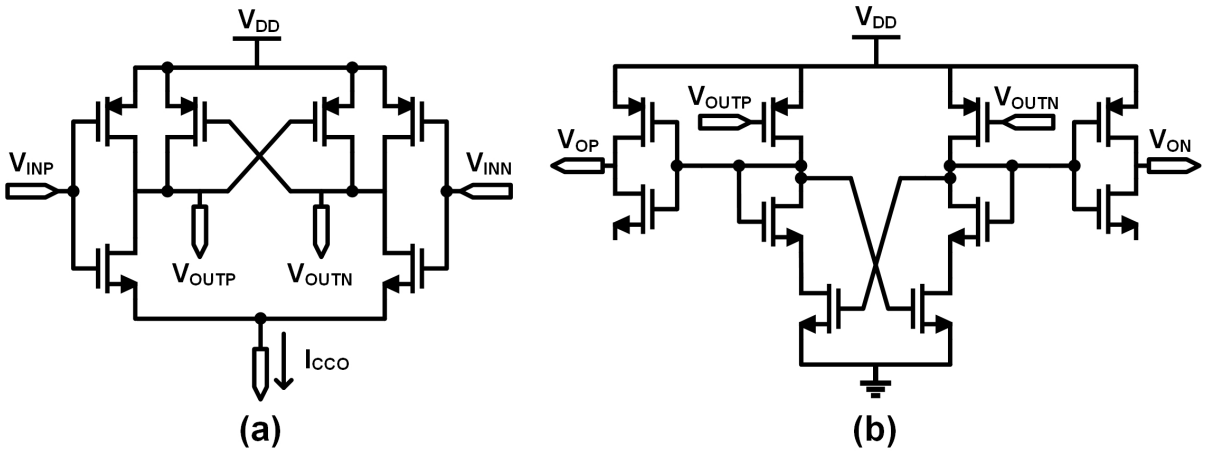

Figure 4. (**a**) Delay cell circuit. (**b**) Level shift circuit.

2.2. Basic Linear Model

Firstly, an analysis of the first-order linear model for a VCO-based ADC is conducted. In Figure 5, the upper part is the functional block diagram of a VCO quantizer, while the lower part corresponds to its linearized frequency domain model. The VCO module, corresponding to the VI and CCO, performs voltage-to-current and current-to-frequency conversions on the input VIN signal, respectively. The quantizer module, represented by a set of registers, is responsible for sampling and quantizing the phase signal output from the VCO.

In the corresponding frequency domain model, the VCO module is represented as an integrator with a gain of $2\pi K_V$, tasked with converting the input V_{IN} signal into the VCO's phase signal, introducing a certain amount of phase noise in the process. The quantizer is depicted as a sampling circuit with a specific sampling time, where quantization noise is introduced into the circuit. For ease of understanding, the first-order differencing module is represented as a discrete-time differentiator performing the transfer function $1 - Z^{-1}$.

As shown in Figure 6, the quantization noise first undergoes first-order noise shaping through the differencing operation depicted in the diagram. It is also observable that the VCO's phase noise undergoes shaping. However, due to the original phase noise signal possessing a slope of -20 dB/dec, the result of the shaping is a flat spectrum. In practical

scenarios, the shaped VCO phase noise would also contain 1/f noise, but, for the sake of the following analysis, this aspect is temporarily simplified.

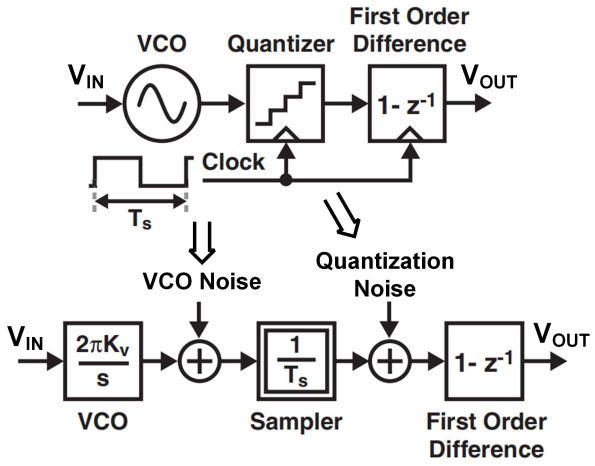

Figure 5. Block diagram model and corresponding linearized frequency domain model of VCO-based quantizer.

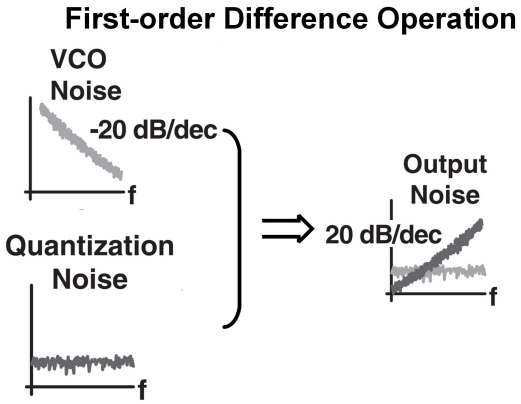

Figure 6. Noise shaping of linearized frequency domain models.

In fact, the first-order differencing module transforms the VCO phase signal into the corresponding VCO frequency signal. However, discrete-time (DT) differentiation is not the exact inverse of continuous-time (CT) integration. Firstly, sampling introduces aliasing in the input signal, and the $1 - Z^{-1}$ filter only serves as an approximation of CT differentiation. As depicted in Figure 7, the resulting DT spectrum of the VCO frequency measurement closely follows the input spectrum at low frequencies and possesses a low-frequency gain factor of $2\pi K_V$. However, as the frequency approaches $F_s/2$ ($\phi = \pi$), the spectrum begins to slightly drop due to the CT/DT inversion approximation.

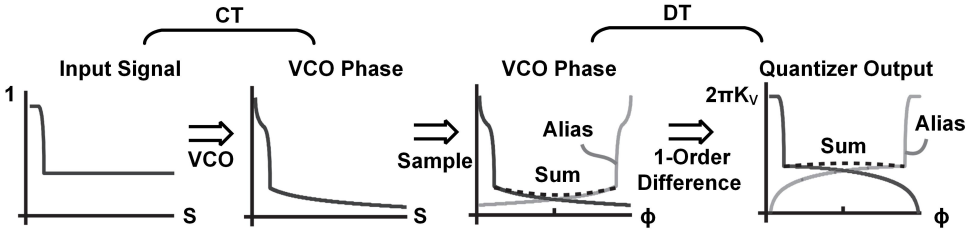

Figure 7. Spectrogram based on VCO quantization.

By comparing the reconstructed input signal (in dark lines) with a copy of the aliased signal (in lighter lines) through the output of the VCO quantizer, it can be observed that the VCO-based quantizer inherently functions as a first-order anti-aliasing filter. Although the structure of this first-order anti-aliasing filter is simple, its effectiveness in suppressing the aliased signal is roughly equivalent to 20 log (F_s/F_b).

For linear analysis, it is necessary to select a primary time domain for the corresponding calculations. Typically, modeling and analysis in the DT domain are already quite mature. Therefore, it is required to convert models operating in the CT domain into their respective DT domain models.

Firstly, CT integration can be approximated as a DT accumulator by using the Taylor series expansion of the exponential function e^x.

$$\frac{1}{1-Z^{-1}} = \frac{1}{1-e^{-sT}} = \frac{1}{1-(1+\frac{(-sT_s)^1}{1!})+(1+\frac{(-sT_s)^2}{2!}\ldots} \approx \frac{1}{sT_s} \tag{3}$$

To construct the DT model, first replace the gain of the CT-VCO, $2\pi K_V/\mathrm{s}$, with the gain formula for the DT-VCO, $2\pi K_V T_s/(1-Z^{-1})$, and move the gain of the sampler, $1/T_s$, in front of the VCO quantizer, as shown in Figure 8. For low-frequency input signals, the VCO quantizer is approximated as a single module with a gain $VCO_{gain}(\mathrm{z})$, which converts the input voltage $V_{IN}(\mathrm{z})$ into the frequency at VCO output $V_{OUT}(\mathrm{z})$:

$$VCO_{gain} = \frac{V_{OUT}(z)}{V_{IN}(z)} \approx 2\pi K_V T_s \tag{4}$$

Combining the expression for K_{vco} given in Equation (1), the expression for the signal-to-quantization-noise ratio (SQNR) can be derived as follows [12]:

$$SQNR_{peak} = \frac{(3A*N*K_{VCO})^2 F_s}{\pi^2 f_b^3} = \frac{9A^2 f_s}{\pi^2 f_b^3}\left(\frac{G_m}{C*VDD_{CCO}}\right)^2 \tag{5}$$

where A is the amplitude of the input sinusoidal signal, and f_b represents the signal bandwidth. It can be observed from Equation (5) that the size of the SQNR is related to the delay and swing of the VCO. With the continuous advancement of technology, both the parasitic capacitance C and VDD_{CCO} of the VCO can be reduced, thereby increasing the SQNR. This demonstrates the advantages of VCO-based quantizers in advanced process technologies.

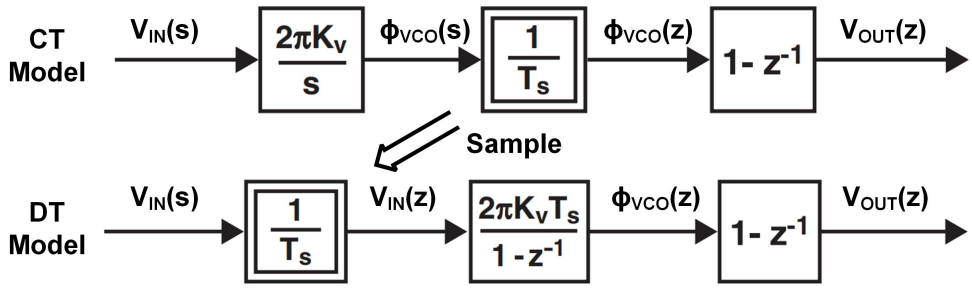

Figure 8. The conversion of the CT linear model and DT linear model.

2.3. VCO-Based ADC Quantization Process

As shown in Figure 9, different input voltages V_{turn} result in varying oscillation frequencies in the VCO. The output waveform of the VCO is sampled by an edge counter after level shifting and stored in a set of registers (DFFs) at a sampling frequency f_s. In this design, the edge counter operates in a cyclic manner without the need for resetting and provides the output as the difference between two consecutive register values. The purpose of this approach is to preserve the truncation error q[n] that occurs at the end of each clock cycle, allowing it to accumulate in the next cycle. If the accumulated quantization error exceeds one LSB, an additional output is generated. This ensures that the quantization error between samples remains within one LSB.

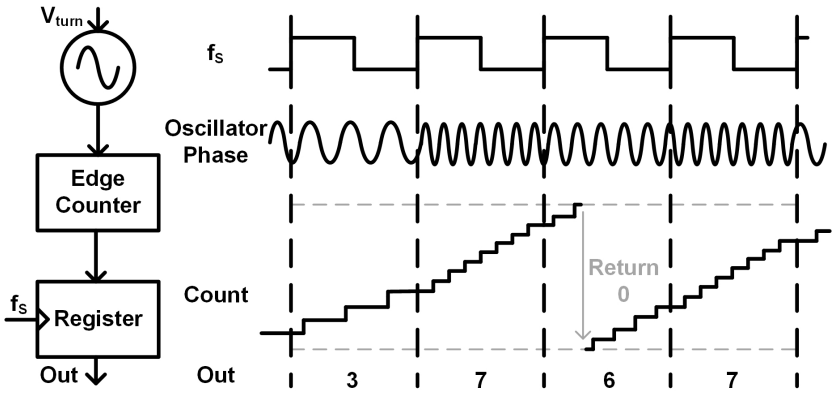

Figure 9. Simplified VCO-based ADC quantization process.

As shown in Figure 10, since the residual phase from the previous sampling period q[n] inherently becomes the initial phase for the next sampling period, when the quantization error of the third sample exceeds one LSB, the output sequence is [3 3 4 3]. At this point, the manifestation of the quantization error is as follows:

$$Q_{error}[n] = q[n] - q[n-1] \tag{6}$$

where q[n] corresponds to the truncation error that occurs between the edges of each clock cycle. The output of the VCO-quantizer can therefore be expressed as

$$Y_q[n] = \frac{N_q}{2\pi}(\phi_{turn}[n] + \phi_q[n-1] - \phi_q[n]) \tag{7}$$

where N_q is the number of VCO phases and ϕ_{turn} is the VCO phase change caused by the analog input V_{turn}. By applying the z-transform to the equation, we can obtain

$$Y_q(z) = \frac{N_q}{2\pi}(\phi_{turn}(z) + \phi_q(z)(z^{-1} - 1)) \tag{8}$$

From Equation (8), it can be observed that the quantization error of the VCO quantizer is shaped by first-order noise shaping. Therefore, it is equivalent to a first-order Sigma-Delta modulator.

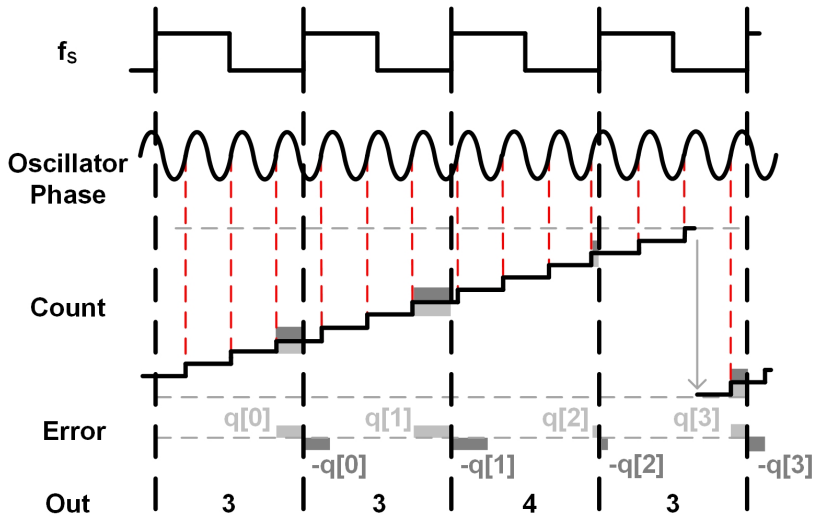

Figure 10. The principle of first-order noise shaping.

2.4. Multi-Phase Quantizer Circuit

The power consumption of the analog section in the circuit mainly originates from the oscillation of the VCO, where a higher oscillation frequency requires a larger current. To reduce the power consumption of the analog circuit and improve the original resolution, the VCO needs to generate more edge transitions during sampling. This design utilizes an edge counter that counts both rising and falling edges simultaneously. Assuming that the center frequency of the VCO is f_c, in the case wherein the number of ADC output bits is determined, this design can reduce f_c to half of its original value. Moreover, this design uses a multi-phase quantizer to quantify the output of the VCO. Assuming that the number of quantizers is N, this method can reduce f_c to the original 1/N. By combining these two approaches, the center frequency of the VCO in the analog circuit can be decreased to $f_c/2$ N, significantly reducing the current consumption of the analog circuit.

As shown in Figure 11, to balance the reduction in current consumption of the analog VCO and the increased power consumption of multiple phase quantizers, a simulation was conducted to obtain the relationship between the number of phase quantizers and the total power consumption of the chip. From the figure, it is evident that with an increase in the number of phase quantizers, there is a significant reduction in the power consumption of the analog VCO part. The reason for the slow increase in digital power consumption is twofold: on one hand, the digital supply voltage is relatively lower compared to the analog voltage, and on the other hand, the digital part can be optimized through synthesis. When the number of phase quantizers reaches 4, the total power consumption of the entire chip is optimized. Similarly, another reason for selecting 4 phase quantizers is that this count increases the total output bit count by 2 bits. Although using 5 phase quantizers could increase the output bit count by 3 bits, it does not reach saturation, leading to the wastage of chip resources. Therefore, in this design, the number of phase quantizers is set to 4.

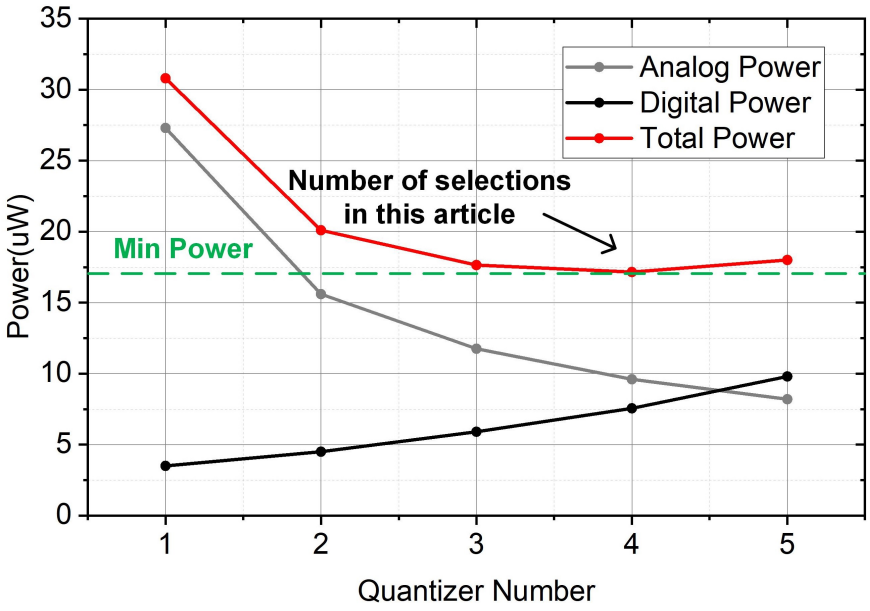

Figure 11. Simulation of the relationship between the number of phase quantizers and chip power consumption.

Figure 12 presents the schematic diagram of the VCO phase quantizer. The phase quantizer contains a counter that counts and samples the phases from the VCO simultaneously. After the end of a sampling period, the counter result is sent to a digital differencing circuit to implement first-order noise shaping. The digital differencing circuit consists of two sets of registers controlled by the same clock. The phase change of the VCO during a

sampling period is obtained by subtracting the values of the two register sets. Finally, by summing the four sets of 6-bit values, an 8-bit output is produced.

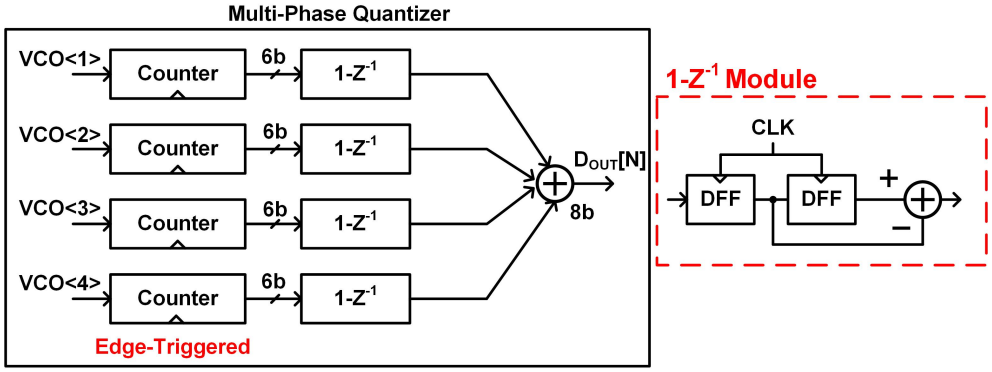

Figure 12. Schematic diagram of the VCO phase quantizer.

The DFF registers in the edge counter are triggered by the rising edges of f_s. Due to non-idealities in the circuit, such as clock skew, the timing of the polarity transitions may slightly differ. The binary count output flips multiple bits in each transition. If the rising edge of f_s coincides with the conversion in the edge counter, it may lead to large errors in the output of the DFF. To address this issue, the design incorporates Gray code encoding, as shown in Figure 13. After the edge counter, the binary count is first converted into Gray code, and, after passing through the DFF, it is converted back to binary. Since the Gray code only flips one bit at a time, even in the presence of metastability in the DFF, the errors can be constrained within one bit.

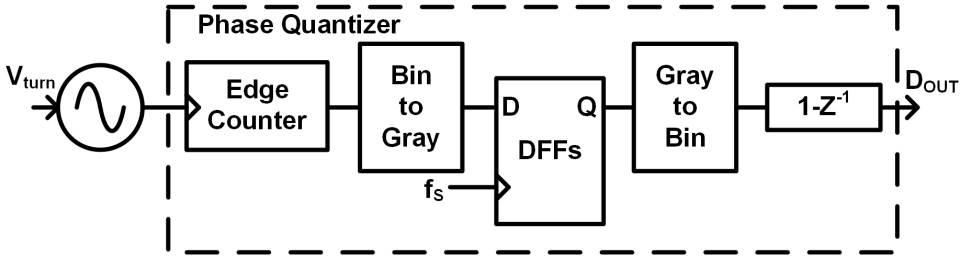

Figure 13. Gray code coded phase quantizer.

2.5. Architecture of the Proposed Circuit

The simplified schematic of the proposed VCO-based ADC is shown in Figure 14. The input signal undergoes chopping and is then summed with the C_{DAC} feedback signal. In order to improve the linearity, the amplitude of the summative residual signal V_{ERR} is below 10 mV. The size of the residual signal VERR is usually determined by the loop coefficient, the DAC step size ΔDAC, and the DAC jitter (1 LSB). It can be expressed as follows:

$$V_{ERR} = V_{IN}(1 - z^{-1})^2 + \frac{1}{2}\Delta DAC + LSB = V_{IN}(1 - z^{-1})^2 + \frac{3V_{ref}}{2^{N+1}} \quad (9)$$

where N is the number of output bits of the ADC. It can be seen that the input signal V_{IN}, the reference voltage V_{REF}, and the output bit N together determine the size of the V_{ERR}. The input range of the chip can be calculated as

$$V_{IN}(InputRange) = V_{ref} * \frac{C_{DAC}}{C_{IN}} \quad (10)$$

where V_{REF} is the reference voltage of C_{DAC}, C_{DAC} is the capacitance of the total DAC, and C_{IN} is the AC coupling capacitance of the input end. Similarly, the IRN of the chip can be expressed as

$$\overline{V_{ni}^2} = \overline{V_{ni,VCO}^2} * (1 + \frac{C_{DAC} + C_{V/I}}{C_{IN}})^2 \quad (11)$$

where $C_{V/I}$ is the parasitic capacitance of the input difference pair, and $\overline{V_{ni,VCO}^2}$ is the IRN of the VCO quantizer. From Formulas (10) and (11), it can be observed that a larger ratio of C_{DAC} to C_{IN} increases the chip's input range, enhancing its ability to withstand the impact of EDO, but at the expense of degrading the chip's input referred noise performance. Therefore, a trade-off must be made between the chip's input range and IRN.

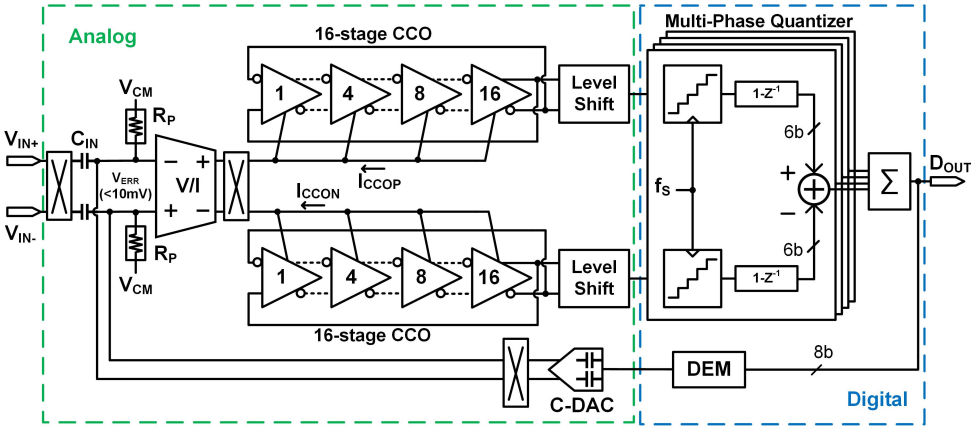

Figure 14. Simplified schematic of the proposed VCO-based ADC.

The V/I conversion circuit converts the residual signal V_{ERR} into the corresponding current signal to control the oscillation frequency of the CCO. The CCO consists of 16 cascaded differential delay cells, and the oscillating signal is converted into a digital signal by a level shifter circuit. Four phase quantizers sample and quantize the cascaded CCO at intervals of every 4 delay cells, with the sampling frequency f_s set at 256 kHz. Subsequently, a digital differencing circuit is employed to achieve first-order noise shaping. The final digital output is obtained by summing the outputs of the four quantizers. A DEM structure is implemented in the feedback loop to mitigate capacitance mismatch. The entire circuit is primarily divided into digital and analog domains, with all digital logic being implemented in Verilog and synthesized using standard digital design methodologies.

3. Measurement Results

The circuit proposed in this paper is implemented using CMOS 180 nm technology with a core area of 0.225 mm^2 (550 µm × 410 µm). Figure 15 is a microscopic view of the proposed circuit. As shown in Figure 15, the area of the analog part of the V/I and VCO circuit (250 µm × 55 µm) is only 1/8 that of the digital circuit (280 µm × 410 µm), indicating that the circuit proposed in this paper is highly digital. The entire chip achieves power consumption of 17.1 µW under a power supply voltage of 1.8/1 V. Through simulation verification, if only one quantizer is used to quantize the VCO, the power consumption of the analog section exceeds 20 µW. The proposed multi-quantizer structure reduces the analog power consumption to 9.6 µW, while the digital circuit consumes 7.5 µW. In more advanced processes, the power consumption and area of the digital circuit can be further reduced.

Figure 16 presents the test PCB and testing environment for a first-order multi-quantizer ADC chip based on a VCO. On the PCB shown in Figure 16a, the chip's inputs, power, and clock are all externally provided. An APx555 audio analyzer, serving as a pure signal source, is used to input an analog differential sine wave signal to the chip. As shown in Figure 16b, the output of the chip is a differential 8-bit output, which is connected to a logic analyzer, the 16802A (Agilent, Santa Clara, CA, USA). Finally, the output spectrum is calculated by MATLAB R2022b in a PC.

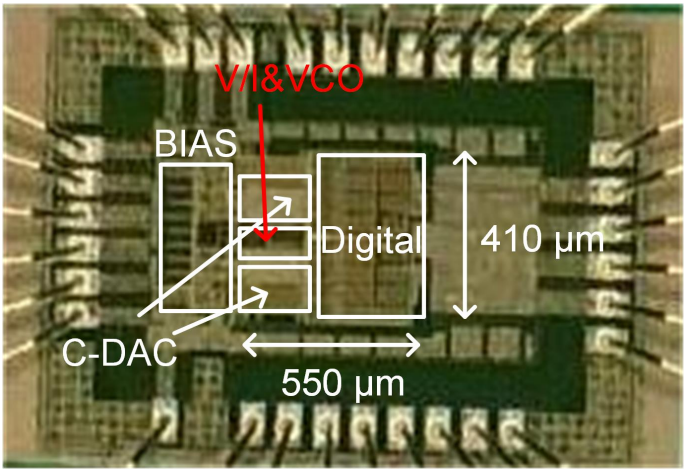

Figure 15. Microscopic view of the proposed circuit.

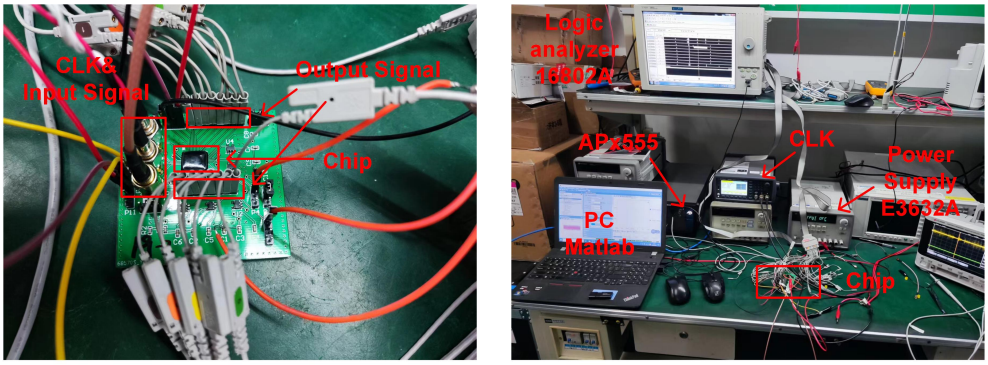

Figure 16. First-order VCO test diagram: (**a**) test PCB, (**b**) test environment.

The performance parameters of the ADC were tested using an APx555 audio analyzer as an ultra-low distortion signal source, generating a 100 mV_{pp} amplitude and 1.375 kHz sine wave. In total, 524,288 points of the output signal were subjected to FFT, and the resulting output spectrum is shown in Figure 17. Within a 5 kHz bandwidth, the ADC achieved an SNDR of 62.1 dB and an SFDR of 65.1 dB. The presence of a digital first-order differentiator affected the ADC, resulting in a first-order noise shaping effect of 20 dB/decade.

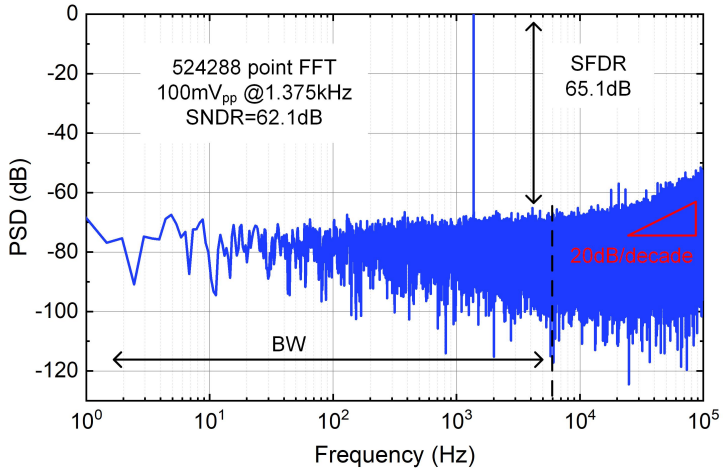

Figure 17. Measured ADC output spectrum.

As shown in Figure 18, the relationship between the SNDR of the proposed ADC and the input frequency was measured across a bandwidth of 50 Hz to 5 kHz. As indicated by Formula (5), derived in the text, the precision of the ADC is influenced by the size of the VCO parasitic capacitance due to process variations. To lend more credibility to the test data, multiple samples were measured. The results demonstrate that within the 5 kHz frequency range, the variation in the SNDR across multiple samples remains within an acceptable margin of 2.3 dB.

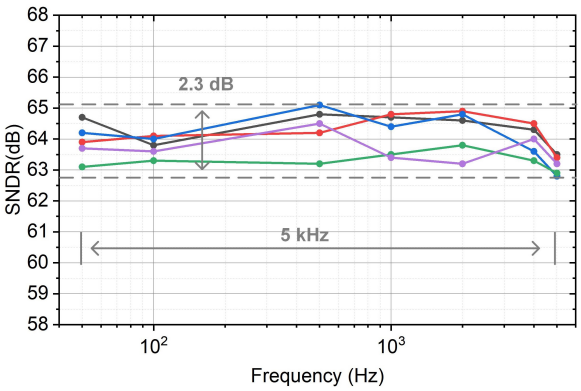

Figure 18. Measured SNDR versus input frequency (5 samples).

Figure 19 illustrates the measured SNDR versus the input amplitude, demonstrating the ADC's dynamic range (DR) of 55.2 dB. Figure 20 presents the measured ADC input reference noise spectrum, which was measured at 8.64 μV_{rms} within a 5 kHz bandwidth.

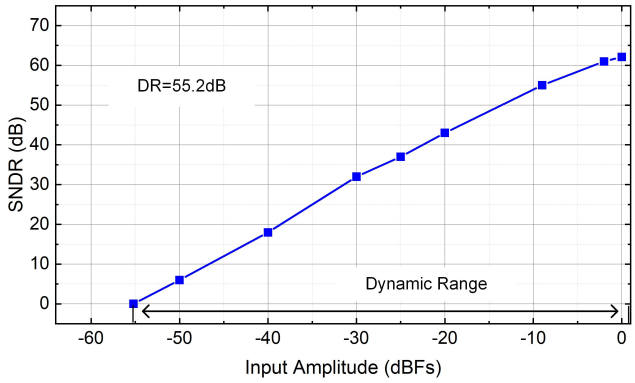

Figure 19. Measured SNDR versus input amplitude.

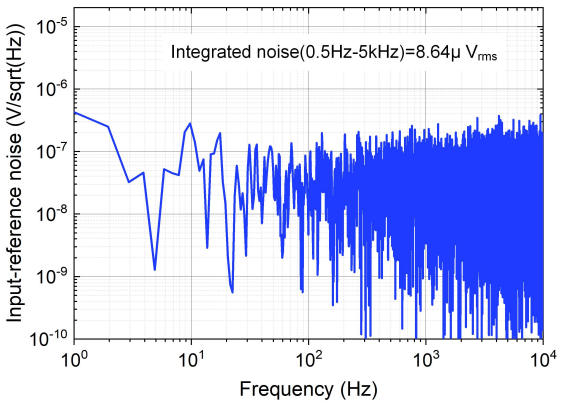

Figure 20. Measured ADC input-referred noise spectrum.

Table 1 presents a performance comparison with advanced technologies introduced in recent years. Compared to the IA+ADC architecture described in [27], this work achieves a lower area of 0.225 mm^2 and power consumption of 17.1 μW. In contrast to the ΔΣ ADC structure shown in [28], this paper realizes a higher input range and SNDR. While similar to [29] in terms of power consumption and SNDR, this work has managed to achieve an input range of 500 mV_{pp} by adjusting the feedback coefficients. The lower power consumption reported in [12,23] is based on the use of more advanced processes and narrower bandwidths, whereas our design supports a wider bandwidth of 5 kHz. The multi-channel structure discussed in [30] features very small per-channel areas, yet it falls short of our proposed architecture in aspects such as the input range and SNDR. Considering EDO and MAs, our study significantly exceeds the input range of approximately 100 mV_{pp} found in other studies by achieving a substantial 500 mV_{pp}. In summary, within the context of EEG signal recording circuits, the first-order VCO structure of the ADC introduced in our study is highly digitalized, offering superior adaptability to the demands of advanced technological nodes.

Table 1. Comparison with the EEG signal recording circuit.

	TBCAS [27]	**JSSC [28]**	**JSSC [29]**	**JSSC [23]**	**LSSC [12]**	**Electronics [30]**	**This Work ***
Topology	IA+ADC	ΔΣ ADC	VCO-based	VCO-based	VCO-based	VCO-based	VCO-based
Technology (nm)	180	180	40	40	65	55	180
Die area (mm^2)	3.7	0.005/channel	0.0145	0.135	0.01	0.004/channel	0.225
Supply voltage (V)	1.8	1.8	1.2(A)1(D)	1.2(A)0.45(D)	0.6	1.2(A)1(D)	1.8(A)1(D)
Power (μW)	56	14.6	17	7	3.2	13.75	17.1
Fs (kHz)	1000	2720	4200	3	1	256	
BW (kHz)	2.5	10	5	0.2	0.5	10	5
Input range (mV_{pp})	rail-to-rail	7.6	8	100	<100	149	500
IRN (nV/sqrt(Hz))	55	48.8	32	367	98.4	142.9/69.7	122
SNDR (dB)	N/A	57	61.85	75.2	51	52.7	62.1
SFDR (dB)	56.6	62.1	70.8	79	62	59.38	65.1
DR (dB)	59	<50	<50	77.4	N/A	77.6	55.2
* FOM (dB)	137.5	145.3	146.5	149.6	132.9	141.3	146.7

* FOM = SNDR + 10 log (BW/Power).

4. Conclusions

This paper presents a first-order noise shaping VCO-based ADC for the EEG signal recording front ends. To address the difficulty of applying analog integrators in advanced processes due to low voltages, a multi-phase quantizer structure is proposed to reduce the fc of the VCO to 1/2N, achieving lower analog power consumption with the same output bit resolution. The core area of the proposed circuit is 0.22 mm^2, consuming 17.1 μW, and it achieves a 62.1 dB SNDR and 10.02 bit ENOB within a bandwidth of 0.5–5 kHz, meeting the requirements of multi-channel EEG signal recording front ends. By introducing a form of Gray code encoding, the errors caused by circuit metastability are limited to within 1 bit. By employing digital differencing circuits, a first-order noise shaping effect is achieved, with input noise of 8.64 μV_{rms} within the 0.5–5 kHz bandwidth. In view of the influence of MA and EDO, compared with the small input ranges of other EEG acquisition circuits, the circuit proposed in this paper achieves a large input range of 500 mV_{pp}, which greatly expands the application potential in the complex EEG recording environment. In summary, the EEG front end demonstrated in this paper holds significant research value and practical implications.

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