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Aging Analysis and Anti-Aging Circuit Design of Strong-Arm Latch Circuits in 14 nm FinFET Technology

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Abstract: Despite the advantages of fin field-effect transistors (FinFETs), there are hidden issues such as electric field enhancement and exacerbated self-heating effects, which will intensify device aging effects. Due to the escalating costs associated with aging protection at the device process level, there is an urgent need to reduce the impact of aging on circuit performance from the circuit design perspective. This study focuses on the specific structure of the strong-arm latch comparator and conducts a detailed aging analysis. Based on the quasi-static approximation (QSA) model, the threshold voltage shift under operational stress is simulated. It is concluded that both the hot carrier injection (HCI) effect and negative bias temperature instability (NBTI) effect play equally non-negligible roles. Furthermore, aging tests were conducted based on 14 nm FinFET devices, validating the substantial HCI effects induced by short-duration pulses. Simultaneously, the test results suggest that the aging effect becomes more remarkable with increasing current. An improved circuit is proposed to reduce the HCI effect by reducing the current pulse by the way of pre-charging, which effectively reduces the threshold voltage shift of the latch comparator input transistors.

Keywords: strong-arm latch; FinFET; hot carrier degradation; negative bias temperature instability; anti-aging design

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1. Introduction

As metal–oxide–semiconductor (MOS) device dimensions scale to the nanometer scale, the electric field of the gate oxide layer continuously strengthens. Concurrently, with the rise in chip operating temperature, the degradation in device and circuit performance caused by aging effects becomes increasingly inevitable. The reliability issues of integrated circuits are gradually emerging as critical bottleneck issues in enhancing circuit performance [1,2]. Research has indicated that time-dependence dielectric breakdown (TDDB), bias temperature instability (BTI), and hot carrier injection (HCI) are critical degradation mechanisms affecting device reliability [3]. With the decrease in power supply voltage, the aging effect of TDDB gradually diminishes, while the latter two aging effects become key factors affecting device lifetime [1]. BTI is attributed to carrier trapping in the gate dielectric, leading to performance degradation, including negative bias temperature instability (NBTI) in P-metal–oxide–semiconductor (PMOS) devices and positive bias temperature instability (PBTI) in NMOS devices [4–6]. In addition, when carriers acquire sufficient energy within the channel to become hot carriers, it leads to the aging effect known as HCI in the device [7–10].

Upon entering the 16/14 nm process nodes, the introduction of a three-dimensional fin field-effect transistor (FinFET) enhances gate control capability and increases integration density. However, on the other hand, the reliability issues associated with FinFET devices introduce new challenges for applications. For instance, the three-dimensional structure of the gate electrode in FinFET devices leads to different crystal orientations at the sidewalls and the top, resulting in variations in trap densities. Additionally, the fin-shaped structure of FinFETs exacerbates reliability degradation due to two main factors: the corner effect, which intensifies the local electric field at the corners, and reduced heat dissipation capabilities, leading to severe self-heating effects (SHEs). This results in channel temperatures far exceeding ambient temperatures, both of which contribute to the deterioration of FinFET device reliability [11–15].

Circuit performance will degrade with the deterioration of device performance. Therefore, when devices are applied to specific circuits, it is essential to combine the circuit structures and device aging before conducting analyses [16,17]. In digital circuits, sequential circuits composed of flip-flops and other logic gates are often influenced by aging effects. In analog circuits, the impact of aging effects on performance parameters of circuits such as inductance and capacitance voltage-controlled oscillators (LC-VCOs), comparators, and current mirrors needs to be considered during the design phase [18,19]. For instance, aging can affect the frequency of LC-VCOs and introduce input pair imbalances in comparators. Comparators find extensive applications in circuits such as analog to digital converters (ADCs), over-voltage protections (OVPs), and over-temperature protections (OTPs), where there is often a high requirement for the comparator's resolution. As a result, aging effects on comparators can directly impact the overall circuit performance. For comparators, whether dynamic or static, the input pair transistors are typically subjected to different stresses. Therefore, as operating time and temperature increase, the key performance variation stems from the degradation-induced offset. For instance, in latch comparators, if there is a significant difference in stress between the two input transistors, the resulting threshold voltage degradation will vary, leading to a certain level of offset and thereby reducing the comparator's resolution [18,20].

In order to mitigate the reliability issues associated with the introduction of FinFET devices, past research has primarily focused on optimizing devices from a process perspective. For instance, some studies have explored the use of nitridation treatment and high-temperature annealing to optimize the dielectric interface properties of FinFETs, thereby suppressing NBTI effects [21]. Additionally, there have been proposals to use nanowire channel field-effect transistors as substitutes for FinFETs to achieve lower power supply voltages [22], consequently reducing chip operating temperatures. Nevertheless, transistor-level enhancements incur relatively high costs, and the current technology is not mature enough. Furthermore, there is related research focusing on optimizing transistor layout and arrangement at the circuit level to improve thermal conduction paths [23], thereby reducing self-heating effects. Alternatively, the effectiveness of this method in mitigating device aging effects is limited, necessitating more circuit-level design improvements [24] to enhance the circuit's aging resistance.

For specific comparator circuits, the exacerbated aging performance of devices will also adversely affect their offset. In past research, in order to mitigate the impact of offset on resolution, methods such as output offset storage (OOS) and input offset storage (IOS) have often been employed to eliminate bias [25]. Nonetheless, they fail to address the residual issue stemming from the increase in V_{TH} input transistors under aging effects. Thus, for the strong-arm latch comparators used in FLASH ADCs, more measures aimed at reducing the degradation effects on critical transistors themselves are required.

In this way, when employing 14 nm FinFET devices, it is necessary to conduct more in-depth research into the reliability issues hidden beneath the advantages of speed enhancement and area reduction. Furthermore, considerations for aging protection should be made from a circuit design perspective. The second part of this paper primarily analyzes the critical aging components and the stresses they undergo in the application of the strong-arm latch comparator, while the aging prediction was conducted using the quasi-static approximation (QSA) model. Building upon the analysis, the fourth section describes aging tests on real 14 nm FinFET devices incorporating three stress patterns, revealing that increased HCI stress in this stress alternation waveform exacerbates aging. Consequently, this serves as the basis for circuit design optimization to mitigate aging stress on the devices and specific circuit improvements and the demonstrated anti-aging effects are presented in the fifth section.

2. Aging Stress Analysis of the Strong-Arm Latch

In the field of chip design, ADCs serve as crucial bridges connecting analog and digital signals, playing an indispensable role in signal processing. Among them, the FLASH ADC is a commonly used member of the signal chain. It can be used independently when high speed is desired or as a sub-ADC in hybrid architecture ADCs, such as in pipeline ADCs. A FLASH ADC typically incorporates $2^N - 1$ comparators, where N represents the output bit width. Figure 1a illustrates the architecture of a 3-bit FLASH ADC, comprising 7 comparators. And the DECODE LOGIC converts the outputs of these 7 comparators into the appropriate 3-bit result. Each stage of comparators often utilizes strong-arm latch comparators, as depicted in Figure 1b. Furthermore, each comparator is provided with a reference voltage one bit value higher than the previous one. This results in different stress levels experienced by the input terminals of different comparators for different inputs, thereby causing varying degrees of offset.

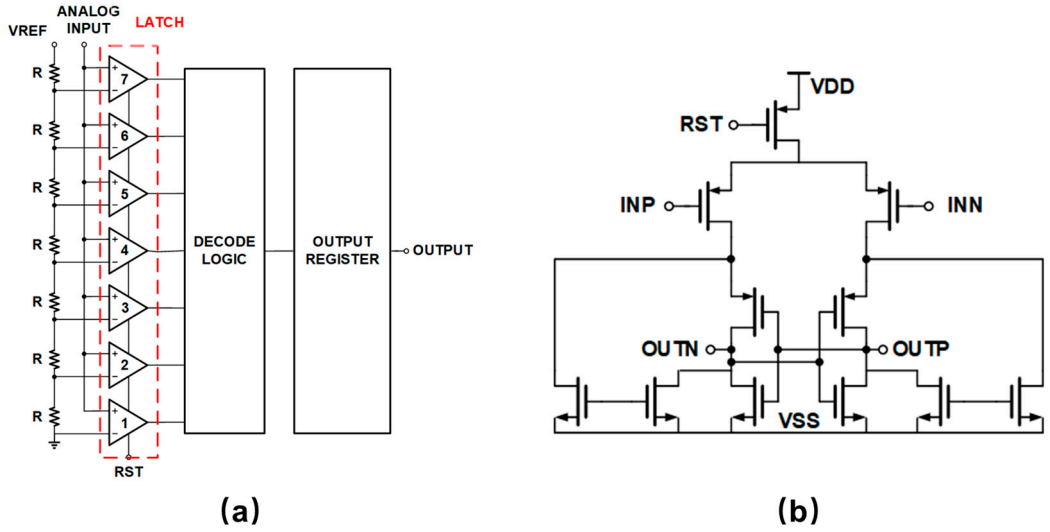

Figure 1. (**a**) Architecture schematic diagram of a 3-bit FLASH ADC; (**b**) Architecture schematic diagram of a Strong-arm Latch Comparator.

As the demand for circuit performance continues to rise, the application of small-sized FinFET devices can offer benefits in reducing chip area and improving circuit speed. However, when introducing 14 nm FinFET devices into the strong-arm latch comparator, the aging effects of FinFET devices are exacerbated to some extent compared to planar transistors [11–15]. Therefore, the degradation of circuit performance due to device aging will be more pronounced.

For a strong-arm latch comparator, from one perspective, the threshold voltage of the input transistors is inherently constrained by the power supply voltage. On that account, while NBTI and HCI effects cause an increase in the threshold voltage, it not only reduces the margin of the circuit but also slows down the comparison speed. From the other perspective, although the threshold voltage of individual transistors itself does not cause mismatch issues in the input transistors, when the threshold voltage is affected by factors such as process variation and aging, mismatch in threshold voltage between the two input transistor pairs often occurs. This contributes to the comparator having its own offset, negatively impacting the resolution of the comparator and the integral non-linearity/difference non-linearity (INL/DNL) of the entire ADC. Hence, the input transistors are the primary focus of attention in comparator aging, as the stress they bear is the main issue causing degradation in circuit performance.

Figure 2a depicts the gate–source voltage and drain–source voltage of the input transistor in the comparator under a reset signal with a 400 ns period and a duty cycle of fifty percent. The stress waveform is primarily biased towards NBTI stress, occupying approximately 50% of the entire cycle. Its magnitude is determined by the PMOS gate voltage, with a smaller gate voltage resulting in a larger voltage difference between it and the source terminal during reset (relatively high), thus increasing NBTI stress. Additionally, the waveform includes HCI stress bias, as illustrated in the inset of Figure 2a, introducing high-current pulses with a very short duration, only in the picosecond range, but with significant current magnitude, making it non-negligible. These two effects are major contributors to aging, leading to significant threshold voltage shifts in transistors as operating time and temperature increase. Therefore, under operational conditions, the input transistor is subjected to the long-term effects of these two aging phenomena. It is necessary to further predict the threshold voltage shift caused by this stress and estimate the influence weights of these two stresses. Subsequently, circuit improvements can be made based on the predictions.

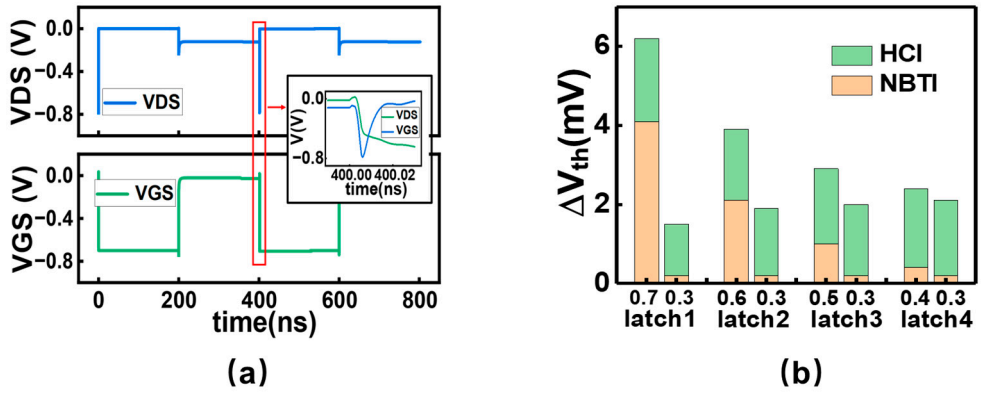

Figure 2. (**a**) The waveform diagram of gate–source voltage and drain–source voltage of the input transistor in the comparator; (**b**) Under conditions of operation at 125 degrees Celsius for ten years, the threshold voltage offset of the strong-arm latch comparator's input transistors.

3. Aging Prediction of Input Transistor

In FinFET devices, the three-dimensional structure exacerbates the aging effects of BTI and HCI. A QSA model [26,27] can be used to predict the threshold voltage degradation caused by them, and the expression of this model is:

$$\Delta V_{th\_hci} = \left(\left(W_g \times \frac{1}{H_g} \left(\frac{I_{gate}}{W} \right)^{m_g} + (1 - W_g) \times \frac{I_{ds}}{HW} \left(\frac{I_{sub}}{I_{ds}} \right)^{m} \right) \times t \right)^{n_1} \quad (1)$$

$$\Delta V_{th\_bti} = AE_{ox}e^{(\Gamma_E E_{ox})}\, e^{-\frac{E_{a2}}{kT_j}} \times t^{n_2} \quad (2)$$

In the expression of HCI degradation, W_g represents the weighting coefficient, which denotes the proportion of gate current and channel hot carrier injection in this effect. In this scenario, the current's magnitude significantly influences the extent of this aging phenomenon. When considering parameters within the BTI aging model, E_{a2} represents the temperature activation energy, Γ_E represents the electric field acceleration coefficient, and E_{ox} is the electric field acceleration coefficient perpendicular to the channel. From Equations (1) and (2), it can be observed that both aging effects follow power-law functions over time. Using these two models as a foundation, aging simulation predictions can be conducted to ascertain the degradation of threshold voltage for various latch comparators within the FLASH ADC illustrated in Figure 1 during operational states.

Under the conditions of V_{IN} = 0.5 V, V_{REF} = 0.8 V, and a temperature of 125 °C, the simulation predicts the aging effects over a ten-year period as shown in Figure 2b. The yellow portion in the figure represents the degradation caused by NBTI, while the green portion represents the degradation induced by HCI. Each pair of adjacent bar charts represents the input pair transistors within the same comparator. The horizontal axis indicates the magnitude of V_{GS} when subjected to NBTI stress, which can be used as a proxy for NBTI stress magnitude.

The data from Figure 2b indicate that for transistors with higher levels of NBTI stress within latch1 through latch4, the V_{TH} degradation is primarily attributed to NBTI. However, when NBTI stress is relatively low, the degradation caused by HCI surpasses that induced by NBTI, becoming a dominant portion of the total degradation. Additionally, for all input pair transistors in latch1 to latch4 of the Figure 1a, despite their differing gate voltages leading to varying levels of NBTI stress, the degradation caused by HCI remains relatively consistent, around 1.8 mV, and does not exhibit a clear relationship with the magnitude of NBTI stress experienced by the transistor. However, the degradation caused by NBTI varies from 0.3 to 0.7 mV depending on the magnitude of NBTI stress, resulting in differences ranging from 0.2 to 4 mV. The V_{TH} variation caused by HCI does not exhibit significant differences among different input transistors. This is because, in the latch comparator, only a short-duration current flows through the input transistors during the reset signal transition, with a duration of <1 ns. Therefore, based on the V_{TH} calculation formula of the QSA model, it can be inferred that the magnitude of degradation caused by HCI at this point is primarily determined by the duration of the current. Additionally, through model predictions, it can be observed that even for very short durations of current, the impact of HCI on the input transistors is not negligible.

4. FinFET Test Result and Discussion

The motivation of this study is to mitigate the impact of FinFET aging effects on circuits. In view of the research on FinFET aging not being comprehensive enough, more FinFET aging test data are demanded to investigate whether the HCI effect caused by transient current pulses will have a negative effect on the degradation of input transistors. Moreover, exploring the relationship between the duration and magnitude of transient currents and transistor aging can provide support for circuit design improvements. As a consequence, this study utilizes FinFET devices at the 14 nm node to conduct tests on actual waveforms in circuits, aiming to explore the aging effects of relatively short durations and magnitudes of current on FinFET devices.

Firstly, it is necessary to consider the aging impact on FinFETs of stress waveforms that combine three different stress modes. In existing research, there has been extensive investigation into the individual impacts of NBTI, HCI, and non-conducting stress (NC)

on various devices, resulting in different degradation scenarios and patterns. Among them, NC has minimal effect on the degradation of V_{TH} in devices while devices exhibit significant degradation effects under individual NBTI and HCI stresses. Yet, research on the interaction of these three stress conditions is still insufficient. While studies have analyzed the impact of NBTI duty cycles on degradation and explored the relationship between HCI and switch counts [28,29], there is currently no research on the influence of HCI proportion on degradation. In this way, we plan to test FinFET devices by controlling stress cycles based on combined waveforms of these three stress conditions. We will adjust the duration and magnitude of current presence by modulating the HCI proportion, aiming to better understand its impact on FinFET aging.

The test was performed using a 300 mm commercial 16/14 nm FinFET wafer. In the fabrication process of the FinFET, self-aligned double patterning (SAPD) is used to form fin channels first, and then shallow trench isolation (STI) is used for isolation. After isolation is complete, the type of FinFET is defined using ion implantation. We then use a sacrificial material to form a temporary gate, then form a doped source and a doped drain through an epitaxial process. After all the high-temperature processes are completed, the temporary gate is removed, and finally a gate is deposited with the high-performance metal material and the high-K dielectric material. The high-k metal gate (HKMG) stack of the device consists of a silica interface layer, a high-k layer of HfO_2, and a TiN metal gate, while the height and width of the fin are 40 nm and 10 nm, respectively, and the structural transmission electron microscope (TEM) image is shown in Figure 3a. This test selected a 10-fin device with a channel length of 16 nm.

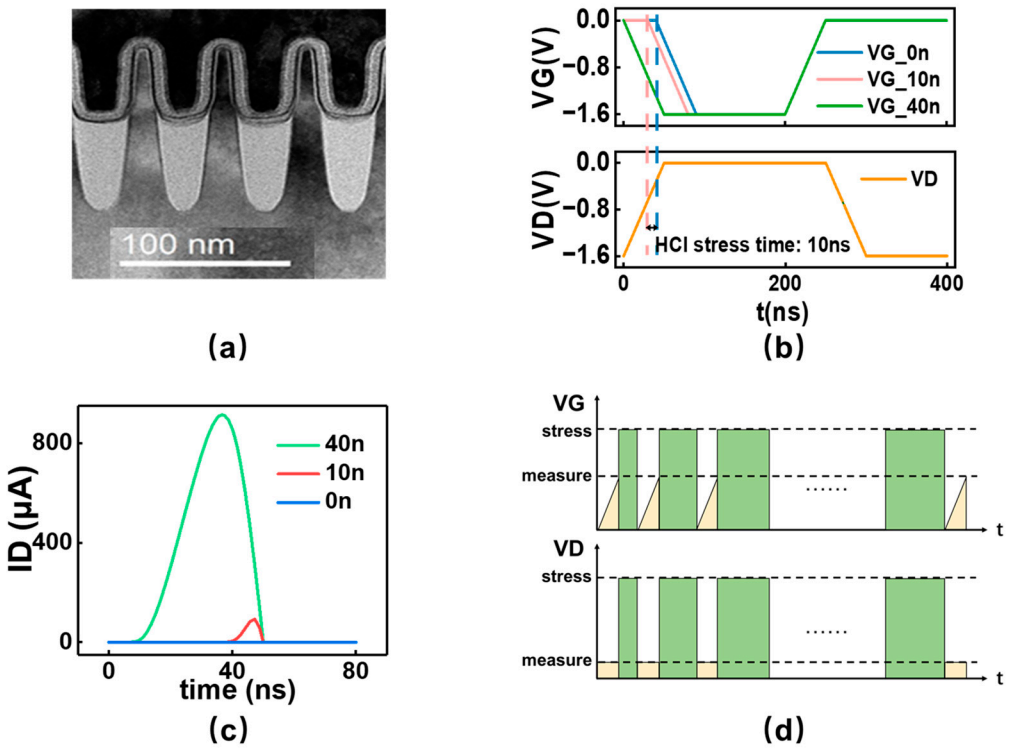

Figure 3. (**a**) The TEM of FinFET in the channel direction; (**b**) Three sets of AC stress waveforms with varying proportions of HCI; (**c**) The current magnitudes and durations for the HCI stress stage in the three AC stresses; (**d**) Illustration of the measure–stress–measure (MSM) waveforms.

The experiments were conducted using four stress waveforms with different HCI stress ratios for comparative testing, all with a testing temperature of 125 degrees Celsius and a stress time of 1000 s. The first group was used to test the aging effect of NBTI alone, which was used as the reference group, with the testing conditions of $V_G = -1.6$ V,

$V_D = -0.05$ V. The remaining three groups are AC waveforms with a period of 400 ns, where the second group is alternating between NBTI stress with a duty cycle of fifty percent and non-conducting stress with a duty cycle of fifty percent, and the voltage setting of the NBTI stress portion is the same as that of the first group. The third group is a duty cycle of 50 percent NBTI stress and 10 ns HCI stress, and the fourth group is a duty cycle of fifty percent NBTI stress and 40 ns HCI stress. The three sets of AC stress waveforms are shown in Figure 3b, and the dashed portion demonstrates the 10 ns interval in which the HCI effect dominates in the third set of test stress.

The constructed V_G and V_D waveforms are applied to specific FinFET devices for transient simulation to obtain the current magnitudes and durations at the three AC stresses in the HCI stress stage as shown in Figure 3c, and it can be observed that the current pulses are significantly decreased with the reduction of the HCI stress time, which indicates that the construction of the waveforms can ensure that only the current pulses are minimized for the test with the NBTI stresses basically remaining unchanged.

The experiments were conducted using a Keysight B1500A semiconductor analyzer (Manufacturer: Keysight Technologies, Santa Rosa, CA, USA). The instrument is equipped with a source measure unit (SMU) that emits DC stress and a semiconductor pulse generator unit (SPGU) that emits AC stress, and these four stress waveforms are applied sequentially to the ports of selected FinFETs. When using the SMU to emit the first set of DC stresses, the amount of threshold voltage degradation at different time points can be extracted by scanning the I_D–V_G curves at a series of fixed points, and the waveform test diagram is shown in Figure 3d. The yellow part represents the voltage setting in the measure phase and the green part represents the voltage setting in the stress phase. In the case of stress testing with AC waveforms, considering the recovery effect of BTI and the inability of the SPGU module to perform DC scanning over the full I_D–V_G range, the one-point drop down (OPDD) version of the ultra-fast measure–stress–measure (MSM) method is used to record aging data under AC stresses. This method involves applying a voltage of $V_G = -0.8$ V, $V_D = -0.05$ V to the device at a series of critical time points and measuring the source leakage current through the device. Before imposing stress, the initial threshold voltage of the device can be obtained by scanning the I_D–V_G curve using the SMU module for each device to be tested at $V_D = -0.05$ V. Subsequently, after each set of AC stress tests, the preset single-point current value is recorded, and the threshold voltage of the device at that moment is inferred by single-point current calculation. The N-exponent of the curve is derived by fitting a power exponent curve to the extracted degradation of the threshold voltage, and the total V_{TH} degradation at 1000 s is also measured for comparison between different groups.

Most of the current studies support that the sources of NBTI are attributed to three categories: interface trap generation (ΔV_{IT}), hole trapping (ΔV_{HT}), and bulk trap generation (ΔV_{OT}). Meanwhile, it is generally accepted that the source of HCI is mainly hot electrons, but HCI also has several degradation mechanisms, and the power index N of the degradation caused by the interface trap generation is above 0.5 [30,31]. Moreover, theoretically, interface trap generation plays a dominant role in the aging effect in PMOS devices, which is due to its carrier holes having a higher injection barrier and a lower tunneling probability relative to electrons. As a consequence, the N-index of the amount of degradation caused by HCI in PMOS devices is larger in comparison to that caused by NBTI.

Due to the different power-law exponents associated with degradation when different mechanisms dominate [32], the power-law exponent obtained by fitting the degradation versus time curve can be used to determine the sources of the two degradation effects. Figure 4a displays the initial I_D–V_G curve of the device as well as the I_D–V_G curve after

aging under NBTI stress for 1000 s, showing a noticeable threshold voltage shift in the device. Statistical analysis of V_{TH} values at all time points reveals the threshold voltage degradation curves of the device under various stresses, as shown in Figure 4b. From Figure 4b, it can be observed that the same device exhibits significantly different power-law exponents and degradation amounts under different stresses.

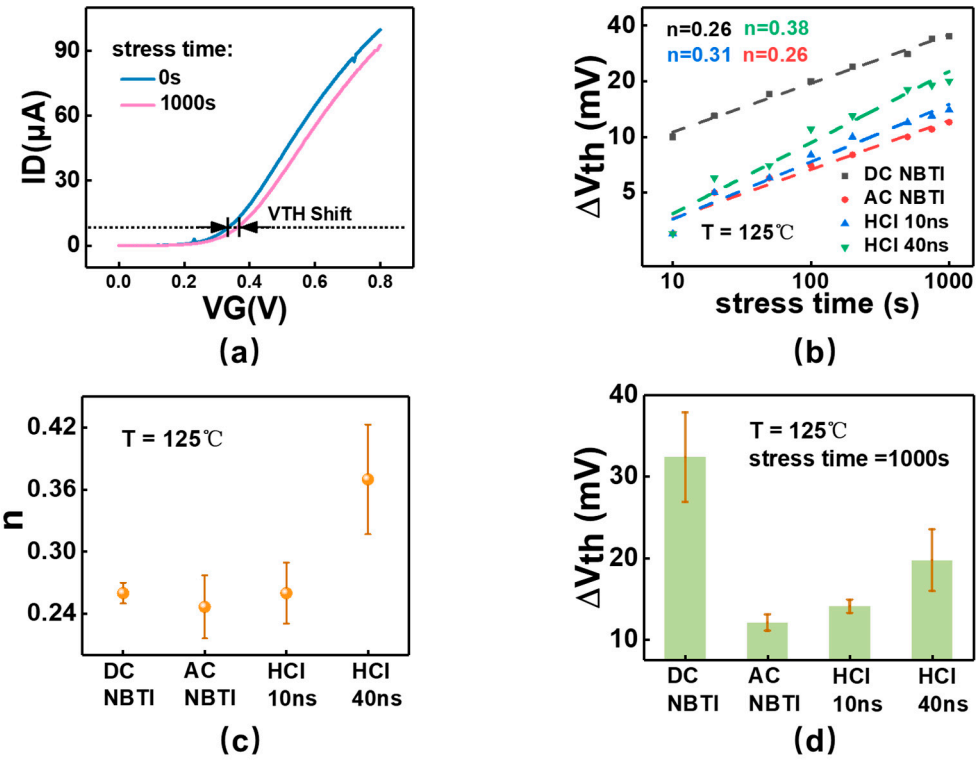

Figure 4. (**a**) The initial I_D–V_G curve of the device as well as the I_D–V_G curve after aging under NBTI stress for 1000 s; (**b**) The threshold voltage degradation curves of the device under four different stresses and the time power-law exponent n; (**c**) The average time power-law exponent n and its variation range for device aging under each stress; (**d**) The average threshold voltage shift and its variation range for device aging under each stress.

Figure 4c presents the range and mean of the N index for multiple data sets under four stress conditions. The positions of the circular markers indicate the mean values, while the vertical lines represent the maximum and minimum values of the data. It can be observed that with an increase in the proportion of HCI stress, the N index noticeably increases. Even compared to the group including 10 ns HCI stress, the AC NBTI group generally exhibits a decrease in the N index. According to the test results, as the duration of pulse stress increases, the N index tends to increase in the direction of the power-law exponent caused by HCI, which suggests that the impact of HCI on aging in FinFETs begins to increase.

Additionally, in Figure 4d, the degradation of the DC NBTI condition is larger due to the longer duration of stress application. Under the other three stress conditions, while keeping the proportion of NBTI stress constant, the variation in V_{TH} is noticeably positively correlated with the proportion of HCI stress. In the absence of HCI stress, the degradation amount at 1000 s is only around 12 mV, whereas in the group with 10 ns of HCI stress, the degradation amount increases to 14 mV. When the HCI stress time is added to 40 ns, the degradation in V_{TH} significantly increases, reaching a maximum of 24 mV. Therefore, during the operation of the latch comparator, the transient currents experienced by the input transistors will also introduce a certain degree of HCI aging, and the resulting degradation effects cannot be ignored. This is consistent with the results obtained from

our simulations based on the QSA model. Hence, in circuit design, it is essential to allocate sufficient margin for aging caused by HCI, while at the same time, efforts can be made to reduce the impact of HCI effects by minimizing the duration of the current, thus serving as a form of aging protection.

5. Anti-Aging Circuit Design and Results

From the results predicted by QSA, it is evident that both NBTI and HCI effects have a significant impact on the threshold voltage shift of the input transistors, and they both adversely affect the circuit performance. Therefore, reducing aging caused by either NBTI or HCI is beneficial for circuit design. However, aging caused by NBTI varies with the magnitude of the analog input, making it challenging to mitigate, whereas aging caused by HCI is less affected by the analog input and can be optimized more effectively.

Firstly, analyzing the structure of the circuit itself and the stress waveforms experienced by the input transistors, we can determine that the HCI effect is mainly due to the input P-type transistor's drain terminal being set to 0 after the RST is set high and the latch comparator is reset. Thus, during the falling edge of RST when the latch comparator is comparing, the input P-type transistor conducts. At this moment, there is a significant voltage difference between the drain and source terminals of the input transistor, resulting in a large current passing through the input transistor until one end of the output terminal is charged to the latch threshold.

Therefore, the key to reducing the HCI effect lies in reducing the duration and magnitude of the conduction current. One direct approach is to increase the size of the input pair transistor to decrease the width of the current pulse, but this would increase the pulse magnitude. Thus, the core idea of our proposed aging prevention method is to pre-charge the drain terminal of the input transistor after the reset stage of the comparator and before the comparison stage. This approach neither interferes with the comparison results nor increases the pulse magnitude passing through the input pair transistor, ultimately reducing both the duration and magnitude of the current in the comparison stage and thereby achieving the goal of reducing the HCI effect.

The specific improvement circuit is depicted in Figure 5a. Its core for aging protection involves constructing a delayed signal, RSTd, for the RST signal. After setting the RST input terminal low, the RST signal descends, causing the M1 to M4 transistor to conduct first and pre-charging the X and Y node. The charging rate can be adjusted by varying the size of stacked diodes. By briefly pre-charging the drain terminal of the input transistor, the potential of the input transistor's drain terminal is increased, reducing the voltage across the source and drain terminals when the input transistor conducts. As can be seen from Figure 5b, in the modified circuit, the sudden change in the source–drain voltage of the input transistor at the beginning of the comparison phase is greatly reduced. This reduces both the magnitude and duration of the current passing through the MOS transistor in the comparison stage. The results are depicted in Figure 5c, demonstrating that the circuit's improvement effectively reduces the current experienced by the input transistors.

Finally, when applying the improved comparator to the FLASH ADC and re-simulating the circuit under the same aging conditions using the same QSA model, the offset of the threshold voltage of the input transistors after improvement can be obtained, as shown in Figure 5d. Compared with Figure 2b, it is evident that the green portion representing the degradation amount of the V_{TH} caused by HCI has been effectively reduced, generally decreasing by around 80%. Additionally, the overall degradation of V_{TH} has also significantly decreased. A comparative analysis of the results is presented in Table 1.

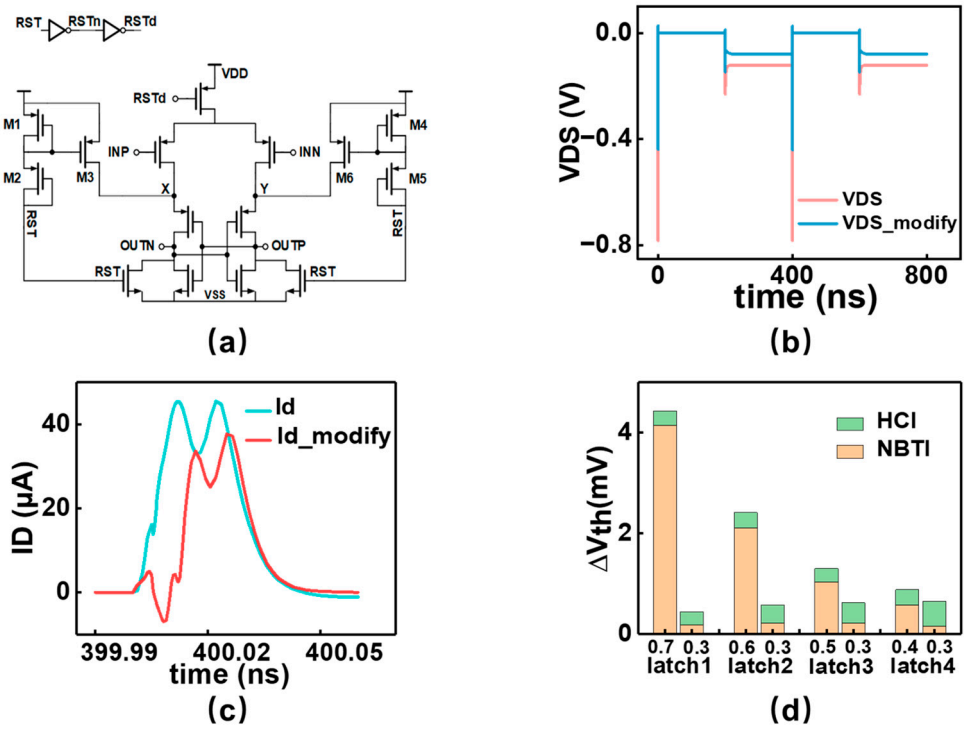

Figure 5. (**a**) A modified strong-arm latch comparator structure with a pre-charging method; (**b**) The comparison of source–drain voltage of input transistor before and after improvement; (**c**) The comparison of current pulses before and after the improvement in the comparator's comparison stage; (**d**) Under conditions of operation at 125 degrees Celsius for ten years, the threshold voltage offset of the improved comparator's input transistors.

Table 1. The reduction ratio of degradation caused by HCI stress and the overall reduction ratio of degradation in the improved circuit.

NBTI Stress (V)	Latch1		Latch2		Latch3		Latch4	
	0.7	0.3	0.6	0.3	0.5	0.3	0.4	0.3
HCI degradation decrease (%)	86.19	80.00	83.33	78.82	85.79	77.78	85.00	73.68
total degradation decrease (%)	28.55	70.67	39.75	67.78	55.17	69.00	63.33	67.50

In summary, based on the positive correlation between the degradation caused by HCI and current pulses, a latch comparator that mitigates circuit aging by reducing current pulses is proposed. Furthermore, the effectiveness of the improved circuit in alleviating HCI aging effects is verified using the QSA model.

6. Conclusions

In conclusion, this paper conducted an aging analysis on a general strong-arm latch and proposed an anti-aging improved circuit, based on the FLASH ADC architecture and combined with research into the aging mechanisms of FinFET devices. Firstly, the work simulated the degradation amount of the threshold voltage of its input transistors based on the QSA model in the actual operating scenario of the comparator, predicting that the aging effects caused by a transient conduction current-induced HCI effect and NBTI effect are comparable and cannot be ignored. Simultaneously, a series of tests were conducted on real production FinFET devices, including DC stress and AC stress tests with controlled current pulse ratios. The results showed that, under the combined stress of NBTI, HCI, and NC

modes, the presence of current pulses would also significantly contribute to the HCI effect, and the degradation of the device and the proportion of HCI are positively correlated. As the amplitude and duration of the current pulses increase, along with the increase in the proportion of HCI, the device performance degradation originating from the HCI effect will also increase, manifested as a significant increase in V_{TH} degradation and N factor results. Finally, considering that the magnitude of the NBTI stress varies with input, which is difficult to control, in this paper we chose to approach the problem by reducing HCI stress, attempting to reduce the current pulse in the comparison stage. A specific circuit improvement scheme was proposed, reducing the current pulse through pre-charging and achieving the anti-aging operation of the latch comparator.

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