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Review

Recent Advances in Electronic and Optoelectronic Devices Based on Two-Dimensional Transition Metal Dichalcogenides

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Abstract: Two-dimensional transition metal dichalcogenides (2D TMDCs) offer several attractive features for use in next-generation electronic and optoelectronic devices. Device applications of TMDCs have gained much research interest, and significant advancement has been recorded. In this review, the overall research advancement in electronic and optoelectronic devices based on TMDCs are summarized and discussed. In particular, we focus on evaluating field effect transistors (FETs), photovoltaic cells, light-emitting diodes (LEDs), photodetectors, lasers, and integrated circuits (ICs) using TMDCs.

Keywords: two-dimensional materials; transition metal dichalcogenides; heterostructures; heterojunctions; field effect transistors; photovoltaic cells; light-emitting diodes; photodetectors; lasers; integrated circuits; MoS_2; WS_2; $MoSe_2$; WSe_2; $MoTe_2$; ReS_2; $ReSe_2$

1. Introduction

The miniaturization of silicon-based transistors has led to unprecedented progress in smaller and faster electronic devices including smartphones and tablet computers. Further miniaturization of transistors is hindered by some fundamental limits including high contact resistance, short channel effects, and high leakage currents [1–3]. Tremendous efforts have been attempted to overcoming these limitations using novel device architecture [4,5]. In addition, silicon-based devices are not applicable for flexible electronics. All the shortcomings of silicon-based transistors have led to the motivation for the search of new device concepts and alternative materials. For example, "transistors without using semiconductors" have been proposed using boron nitride nanotubes functionalized with gold quantum-dots (QDs-BNNTs) [6,7] and graphene–BNNT heterojunctions [8]. All these materials are applicable for flexible electronics. On the other hand, two-dimensional transition metal dichalcogenides (2D TMDCs) offer several attractive features for next-generation transistors, including high electron mobility (up to ~1000 $cm^2\ V^{-1}{\cdot}s^{-1}$ for MoS_2), atomically thin and flexible. In addition, TMDCs can be free of dangling bonds on their surfaces, and offer many interesting optical properties for their potential application in optoelectronic devices.

Although research publication on TMDCs was started around the 1960s, publication activity has increased significantly since 2014. According to our analysis in Web of Science™, a total of 3829 journal articles were published up to 2016, with 33.8%, 21.5%, 12.5%, and 5.5% of these articles were published in 2016, 2015, 2014, and 2013, respectively. Based on these recent publications, we will discuss the application of 2D TMDCs in field effect transistors (FETs), optoelectronic devices (photovoltaic cells, light-emitting diodes, and lasers), and integrated circuits (ICs). Interested readers may refer to a recent

review on the same topics [9]. For the convenience of the readers, we summarize a series of TMDCs along with the nature of their band gaps in Table 1.

Table 1. Summary of semiconductor TMDCs materials (MX_2) and the nature of their band gaps for monolayer (1L) to bulk samples. The direct (D) and indirect (I) bandgaps are as denoted. These values are extracted from both theoretical (T) and experimental (E) study. All data are referring to optical bandgaps at room temperature without considering quasiparticle (e.g., excitons) effects.

M or X	S	Se	Te
Mo	1L: ~1.8–1.9 eV (D) Bulk: 1.2 eV (I) [10]	1L: 1.34 eV (D)(T) [11] 1L: 1.58 eV (D)(E) [12] Bulk: 1.1 eV (I)(E) [13] Bulk: 1.1 eV (I)(T) [14]	1L: 1.07 eV (D)(T) [15] 1L: 1.1 eV (D)(E) [16] Bulk: 1.0 eV (I)(E) [17] 0.82 eV (I)(T) [18]
W	1L: 1.94 eV (D)(T) [19] 1L: 2.14 eV (D)(E) [20] Bulk: 1.35 eV (I)(E) [21]	1L: 1.74 eV (D)(T) [19] 1L: 1.65 eV (D)(E) [22] Bulk: 1.1 eV (I)(D) [23] Bulk: 1.2 eV (I)(E) [21]	1L: 1.14 eV (D)(T) [19] Bulk: 0.7 eV (I)(T) [23]
Re	1L: 1.43 eV (D)(T) [24] 1L: 1.55 eV (D)(E) [24] Bulk: 1.35 eV (D)(T) [24] Bulk: 1.47 eV (D)(E) [25]	1L: 1.34 eV (I)(T) [26] 1L: 1.239 eV (D)(T) [27] 1L: 1.47 eV (I)(E) [28] 2L: 1.165 eV (D)(T) [27] 2L: 1.32 eV (I)(E) [29] 4L: 1.092 eV (D)(T) [27] Bulk: 1.06 eV (I)(T) [26] Bulk: 1.18 (I)(E) [30]	

2. Field Effect Transistors

Field-effect transistors (FETs) are among the basic devices for modern electronic circuits. A typical FET modulates the conductivity of the semiconductor channel between the source (S) and the drain (D) terminals by controlling the applied voltage on the gate (G) electrode. Some of the important figures of merit for FETs are defined here. First, a good FET should have a low subthreshold swing/slope:

$$SS = \left(\frac{d(\log I_{DS})}{dV_G} \right)^{-1}$$

which is defined as the gate voltage (V_G) required to change the source–drain current (I_{DS}) by one order of magnitude (in the unit of volt per decade). FETs are treated as switches that offer a high conductivity of the channel (ON state), and vice versa (OFF state). Hence, the on/off ratio is another crucial factor in measuring the performance of FETs. In addition, mobility is important for high-performance FETs. In 2D TMDCs, the transport of charge carriers is confined to the plane of the materials. The mobility of carriers is related to the scattering by

$$\mu = \frac{e\tau}{m^*}$$

where τ is the scattering time, and m^* is the effective mass of in-plane electron. There are following scattering mechanisms: (1) electron–phonon scattering, including longitudinal acoustic (LA), transverse acoustic (TA) [31,32], polar (longitudinal) optical (LO), and homopolar optical phonons [33]; (2) electron–electron (Coulomb) scattering [34] and charged impurities scattering [35]; (3) surface (interface) roughness Coulomb scattering [34] and phonon scattering [36]; and (4) short-range scattering, which is from the defect and dislocation of the lattice [35,37,38]. The degree to which these mechanics affect the mobility can be evaluated by Matthiessen's rule:

$$\frac{1}{\mu} = \frac{1}{\mu_1} + \frac{1}{\mu_2} + \frac{1}{\mu_3} + \frac{1}{\mu_4}.$$

Finally, Flicker noise is a factor that limits the performance of the FETs. This is a type of electronic noise with a frequency spectrum such that the power density spectrum is inversely proportional to frequency, f, and is therefore referred as 1/f noise. Flicker noise occurs in almost all electronic devices and often shows up as the resistance fluctuation. It is generally related to the impurities in the conductive channel and generation/recombination noise in transistors due to memory of the base current [39].

2.1. Transistors with Multilayered TMDCs

Although the electrical properties and electronic structures of TMDCs were studied in the 1960s [33], their device applications have been limited until 2004. One of the earliest works in which TMDCs were used for FETs was reported by comparing WSe_2 with single-crystal Si metal oxide FETs. A p-type conductivity as high as 500 $cm^2 \cdot V^{-1} \cdot s^{-1}$ was demonstrated at room temperature with a 10^4 on/off ratio at 60 K [40]. Thus, a further study based on multilayer MoS_2 FETs with back-gate configuration was conducted, but a rather low mobility (0.1–40 $cm^2 \cdot V^{-1} \cdot s^{-1}$) was demonstrated [41–43]. Apparently, the reported mobility from multilayered MoS_2 was quite lower as compared to those reported for bulk MoS_2, where mobility is often ranged from 100 to 260 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [33]. Table 2 summarizes the performances of FETs constructed by various TMDCs. It is noted that the mobility of graphene was much higher, up to 10,000 $cm^2 \cdot V^{-1} \cdot s^{-1}$, even when using SiO_2 as the gate materials [44].

Table 2. Performance of FETs based on multilayer TMDCs prepared by mechanical exfoliation and by chemical vapor deposition (as noted with CVD). Electron mobility is compiled here (or denoted by e). The hole mobility is denoted by h.

Materials	Configuration (Method)	Mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	On/Off Ratio	Subthreshold Swing ($mV \cdot dec^{-1}$)	Temperature (K)	Reference
MoS_2	Back-gated	3			300	[41]
	Back-gated	40	10^5	1000	300	[42]
	Back-gated (CVD)	2×10^{-2}	10^4		300	[45]
	Back-gated	100	10^6	80	300	[46]
	Back-gated	2.4	10^7		300	[47]
	Dual-gated	517	10^8	140	300	[48]
	Back-gated	700			300	[49]
	Back-gated (CVD)	17	4×10^8(bi-) 10^4(multi-)		300	[50]
	Four-terminal Back-gated	306.5	10^6		300	[51]
	Four-terminal Top-gated	470(e)/480(h)			300	[52]
	ZrO_2 & CNT Back-gated		10^6		3	[53]
$MoSe_2$	Back-gated	50	10^6		300	[54]
	Four-terminal Back-gated on SiO_2/parylene-C (CVD)	50(Si) 160(parylene-C) 500	10^6(e) 10^3(h)		295/100	[55]
	Four-terminal Back-gated (CVD)	200(e)/150(h)	10^6		275	[56]
	Back-gated (CVD)	10	10^3		300	[57]

Table 2. *Cont.*

Materials	Configuration (Method)	Mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	On/Off Ratio	Subthreshold Swing ($mV \cdot dec^{-1}$)	Temperature (K)	Reference
$MoTe_2$	Back-gated	0.03(e)/0.3(h)	2×10^3		300	[58]
	Four-terminal Back-gated	20(h)	10^5	140	300	[59]
	Ionic Liquid Top-gated	30(e)/10(h)		140(e)/125(h)	300	[60]
	Back-gated	6(h)	10^5		300	[61]
	Solid Polymer Electrolyte Back-gated	7(e)/26(h)	10^5	90	300	[62]
	Back-gated	25.2(e)/1.5(h)	2.1×10^5(e)/ 5.7×10^4(h)		280	[63]
	Back-gated	2.04(h)			300	[64]
WS_2	Iodine-transport Back-gated (PVD)		10^5		300	[65]
	Ionic Liquid Top-gated	20(e)/90(h)		90	300	[66]
	Ionic Liquid Top-gated	19(e)/12(h)	10^6	63(e)/67(h)	300	[20]
	Back-gated	234	10^8		300	[67]
	Four-terminal Back-gated	20	10^6	70	300	[68]
WSe_2	Four-terminal Top-gated	500(h)			300	[40]
	Ionic Liquid Top-gated	200(e/h) 330(e)/270(h)	10		170/160/77	[69]
	Back-gated (CVD)	350(h)	10^8		300	[70]
	Back-gated (CVD)	650(h)	10^6	250/140	150/300/105	[71]
	Back-gated (CVD)	10(h)	10^4		300	[72]
	Back-gated	92(h)	~10		300	[73]
ReS_2	Dual-gated	12/26	10^5	148	300/77	[74]
	Dual-gated	1/5	10^6	750	300/120	[75]
	Back-gated	15.4	10^7	100	300	[76]
	Back-gated	1.5	10^5		300	[77]
	Back-gated	11	3×10^5		300	[78]
	Back-gated (CVD)	7.2×10^{-2}	10^3		300	[79]
$ReSe_2$	Top-gated	0.1			300	[27]
	Back-gated	6.7	10^5	1300	300	[80]
	Back-gated (CVD)	1.36×10^{-3}(h)			300	[81]

Later, by using high-k dielectrics (50-nm-thick Al_2O_3), FETs with a back-gate configuration were reported with relatively high mobility (>100 $cm^2 \cdot V^{-1} \cdot s^{-1}$) and on/off ratio (>$10^6$) based on multilayer MoS_2 (Figure 1a). The width and length of the device were 4 μm and 7 μm, respectively. Thirty-nanometer-thick multilayer MoS_2 was deposited on a silicon substrate that was coated with a 50-nm-thick Al_2O_3 layer. As shown in Figure 1b,c, the near-ideal subthreshold slope/swing of 80 mV/dec and robust current saturation over a large voltage window are demonstrated [46]. Accumulation mode occurred at a positive gate bias, and the window of depletion mode occurred at

negative gate bias. At large negative gate biases, the drain current recovers and forms an inversion mode. Furthermore, FETs with Schottky contacts and Al_2O_3 gate oxide (15-nm-thick) on the top of MoS_2 channel with back-gated configuration was shown to have mobility as high as 700 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature [49]. Liu et al. have further demonstrated that the field effect mobility of multilayer (20 layers) MoS_2 FETs exceeds 500 $cm^2 \cdot V^{-1} \cdot s^{-1}$ due to the smaller bandgap (thus a smaller Schottky barrier) [48], compared with monolayer MoS_2 FET within the same top-gated configuration [82].

The dependence of carrier mobility on temperature in multilayer MoS_2-based FETs is due to different scattering mechanisms as shown in Figure 2. At low temperature, the carrier mobility is limited by charged impurity scattering. The mobility is determined by the combined effect of the homopolar phonon and the polar-optical phonon scatterings at room temperature [46]. Although the high-κ dielectric materials (e.g., Al_2O_3 and HfO_2) may screen Coulomb scattering from charged impurities [49], the complete recovery of the intrinsic phonon-limited mobility has not been observed in high-κ dielectrics encapsulated TMDCs devices at room temperature.

Another limiting factor of mobility is the substrates. It was shown that trapped charges in the interface of MoS_2–SiO_2 would lead to carrier localization in the bilayer and trilayer MoS_2 channel [83]. Considerable mobility improvement was reported in multilayer MoS_2 on PMMA dielectric in comparison with MoS_2 on SiO_2, which was attributed to the reduced short-range disorder or long-range disorder at the MoS_2/PMMA interface [52]. Other phenomena, such as thickness-independent SS and hysteresis as the gate swept, have been attributed to the interface traps between the bottom layer of WS_2/$MoTe_2$ and SiO_2 substrate [64,68]. Besides, the presence of a low-energy optical phonon mode in SiO_2 (∼60 meV) may also cause non-negligible surface polar optical scattering. A two to three times mobility improvement is consistently observed in $MoSe_2$ FETs on parylene-C substrates compared to SiO_2 [55]. WSe_2 FETs with parylene top-gate dielectric have demonstrated high room-temperature mobility up to 500 $cm^2 \cdot V^{-1} \cdot s^{-1}$ [40].

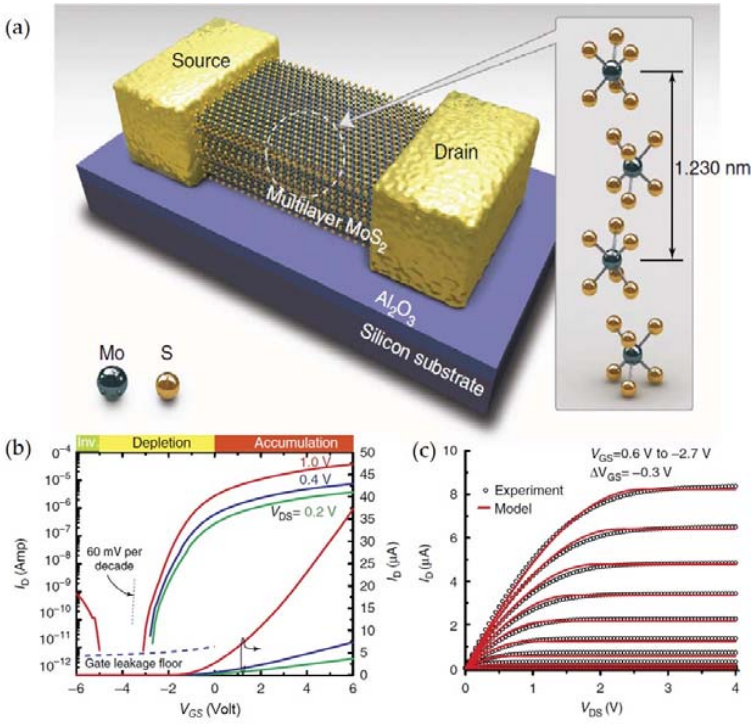

Figure 1. (**a**) A MoS_2 thin film transistor and its transport properties. (**b**) Drain current (I_D) versus back-gate bias (V_{GS}) with different drain bias (V_{DS}). (**c**) Drain current (I_D) versus drain bias (V_{DS}) showing current saturation, including a long-channel model (red lines) showing excellent agreement with measured device behavior. Reproduced with permission from [46], Nature Publishing Group, 2012.

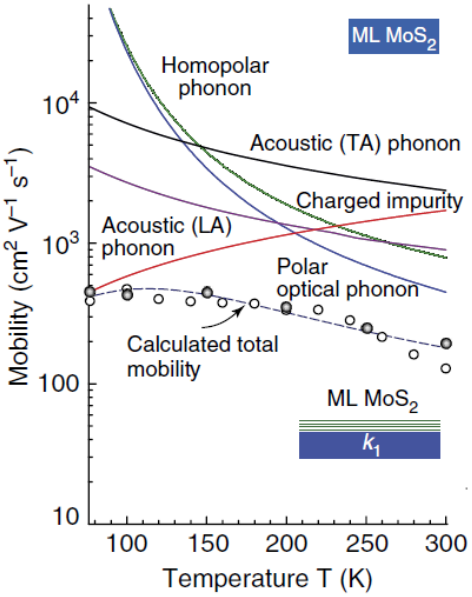

Figure 2. Charge transport properties of the multilayer MoS_2 channel. Measured temperature-dependent mobility of MoS_2 field effect transistors (FETs). Reproduced with permission from [46], Nature Publishing Group, 2012.

Low carrier mobility in TMDC devices might be due to the shortcomings of two-terminal measurements. A mobility of 306.5 $cm^2 \cdot V^{-1} \cdot s^{-1}$ was extracted from the same multilayer MoS_2 device when using a four-terminal configuration, which is considerably greater than 91 $cm^2 \cdot V^{-1} \cdot s^{-1}$ measured by a two-terminal configuration [51]. This results indicated that the intrinsic carrier mobility on the SiO_2 substrate is significantly greater than the values previously reported in MoS_2 FETs [42]. The analogous configuration also applied to FETs based on MoS_2 [52], $MoSe_2$ [55], $MoTe_2$ [59], WS_2 [68], and WSe_2 [40]. Therefore, future studies of TMDCs devices should use the four-terminal measurement.

Table 2 summarizes the performances of FETs constructed by various multilayered TMDCs. By comparing the carrier mobility, the on/off ratio, and the subthreshold swing of these devices, we found that devices constructed by CVD MoS_2 [45], ReS_2 [79], and $ReSe_2$ [81] exhibited very low mobility, which are two or three orders of magnitudes less than those based on exfoliated TMDCs. The relatively low mobility reported in these earlier literatures is likely due to structural defects, such as grain boundary [84]; these grain boundaries act as short-range scattering centers to suppress the carrier transport [85]. After the CVD synthesis conditions were optimized to reduce the grain boundary, the mobility increased to a level similar to that based on exfoliated TMDCs [50,55,70,71]. It was reported that the threshold voltage for devices with exfoliated MoS_2 was higher than that based on CVD MoS_2 [86]. The possible reasons could be the density of unintentional doping and the Scotch tape residue-induced charges in the exfoliated samples.

Furthermore, as compared to the low-resistance ohmic contacts, the Schottky contacts between the TMDCs and gates are one of the reasons for low carrier mobility. It is believed that the nature of contact is more important than the properties of the TMDCs [87]. By using a non-contact method based on THz-probe spectroscopy, an intrinsic mobility of MoS_2 was found to be approaching 4200 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at 30 K, which is an order of magnitude greater than any other previously reported values in multilayer TMDCs devices [88].

The intrinsic current distribution in FETs based on multilayer MoS_2 has been investigated. Here, the 13-layer MoS_2 FETs (8 nm in total thickness) were treated as consecutive resistors in a resistor network model that is based on the Thomas−Fermi charge screening and interlayer coupling effects. The authors map the current distribution among the individual layers of the multilayer 2D systems. Result suggests the existence of a centroid of current distribution or the so-called "HOT-SPOT" in

multilayer MoS_2 FETs [89]. Figure 3 shows the current distribution in the multilayer MoS_2 FETs at different gate bias conditions. As shown, the current mainly travels through the upper layer that is closer to the source and the drain electrodes. The "HOT-SPOT" still moved toward the top layers even when the gate bias was increased. Hence, the large effective interlayer resistance and charge screening effect will limit the carrier concentration of multilayer FETs.

Recently, FETs based on multilayer MoS_2 with an intrinsic gain over 30, an intrinsic cut-off frequency up to 42 GHz (F_t), and a maximum oscillation frequency up to 50 GHz (F_{max}) were fabricated based on optimum contacts and device geometry [90]. These performances are better than those reported so far for MoS_2 transistors [91]. Multilayer MoS_2 FETs with a 1 nm physical gate length using a single-walled carbon nanotube (SWCNT) as the gate electrode were demonstrated. These ultrashort devices exhibit excellent switching characteristics with a near-ideal subthreshold swing of 65 mV/dec and an on/off current ratio of 10^6. Simulations show an effective channel length of ~3.9 nm in the off state and ~1 nm in the on state [53].

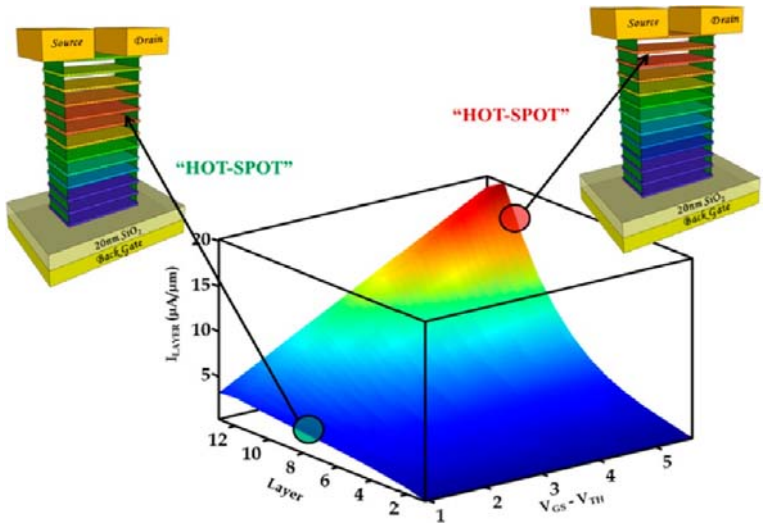

Figure 3. Current distribution among the individual layers of a 13-layer thick MoS_2 FET at different gate bias conditions derived using the resistor network model. The illustrations show the location of the "HOT-SPOT" and the associated current spread schematically corresponding to two different gate bias conditions. The red and blue colors representing the highest and lowest current, respectively. Reproduced with permission from [89], American Chemical Society, 2013.

Finally, while MoS_2 FETs are one of the most studied TMDCs, $MoSe_2$ FETs have been reported to have a low noise characteristic with a Hooge parameter of 3.75×10^{-3} [92], which is similar or lower than MoS_2 FETs [93,94]. On the other hand, WS_2 was once predicted to offer the best transistor performance (the highest on-state current density and mobility) among all TMDCs [95]. However, only a few WS_2 FETs have been reported to have a performance comparable to that of MoS_2 [62]. In addition, $MoTe_2$ offers a favorable bandgap (Table 1) in the near-infrared range. Therefore, $MoTe_2$ FETs are an appropriate candidate to substitute Si and has great potential for high-performance optoelectronic devices [59,63,64]. Finally, ReS_2 and $ReSe_2$ are TMDCs with a direct bandgap in monolayer, multilayer, and bulk forms, as summarized in Tables 1 and 2. They have recently attracted much interest and have been applied to optoelectronic devices.

2.2. Transistors with Monolayer TMDCs

Table 3 summarizes performances of FETs based on monolayer of TMDCs in various gate configurations. As shown, the electron mobility is highest for devices based on exfoliated MoS_2.

Apparently, other TMDCs offer much lower mobility. In addition, the mobility of CVD MoS_2 is also significantly lower.

Table 3. Performance of FETs based on monolayer, exfoliated TMDCs, and CVD TMDCs. Electron mobility is compiled here (or denoted by e). The hole mobility is denoted by h.

Materials	Configuration (Method)	Mobility ($cm^2 \cdot V^{-1} \cdot s^{-1}$)	On/Off Ratio	Subthreshold Swing ($mV \cdot dec^{-1}$)	Temperature (K)	Reference
MoS_2	Top-gated	217	10^8	74	300	[82]
	Simulation Top-gated	350	10^{10}	60	300	[96]
	Back-gated	12			300	[83]
	Top-gated	320	10^6		300	[97]
	Back-gated (CVD)	0.04			300	[98]
	Back-gated	10	10^6		300	[99]
	Polymer Electrolyte Top-gated	10	10^6	60	300	[100]
	Ferro-electric polymer Top-gated	220	10^5	300	300	[101]
	Top-gated	380	10^6	500	300	[102]
	Top-gated	1090	10^8	178	300	[103]
	Back-gated (CVD)	8	10^7		300	[84]
	Multi-terminal Back-gated	1000	10^6		4	[104]
	Back-gated (CVD)	6	10^5		300	[105]
	Top-gated On SiO_2/Si_3N_4 (CVD)	55(Si_3N_4) 24(SiO_2)	10^7(SiO_2)		300	[106]
	Top-gated (CVD)	42.3	10^6		300	[107]
	Dual-gated (CVD)	190	10^8	170	300	[108]
$MoSe_2$	Back-gated (CVD)	0.02(e)/0.01(h)	10^2		300	[109]
	Back-gated (CVD)	50	10^6		300	[110]
	Back-gated (CVD)	23(e)/17(h)	10^5		300	[111]
WS_2	Ionic Liquid Top-gated	44(e)/43(h)	10^5	52(e)/57(h)	300	[20]
	Back-gated	50/140	10^6		300/83	[112]
	Back-gated (CVD)	4.1	10^5		300	[113]
	Back-gated	83/337			300/25	[114]
WSe_2	Top-gated	250(h)	10^6	60	300	[115]
	Ionic Liquid Top-gated	90(e)/7(h)	10^4(e) 10^5(h)		300	[116]
	Polymer electrolyte Back-gated	30(e)/180(h)			300	[117]
	Back-gated (CVD)	100(h)	10^8		300	[70]

Theoretical simulation was applied to predict the performance limits of transistors based on monolayer MoS_2. It is known that optical phonon scattering is the intrinsic scattering mechanism that dominates at room temperature. On the other hand, acoustic scattering is dominated at lower temperature (T < 100 K) [118,119]. Figure 4 shows the temperature dependence of electron mobility in freestanding monolayer MoS_2 as predicted by first principle calculations. As reported, the mobility (μ) is expected to follow the $T^{-\gamma}$ temperature (T) dependence with $\gamma = 1.69$. It was predicted that the mobility of monolayer MoS_2 can reach 410 $cm^2 \cdot V^{-1} \cdot s^{-1}$ at room temperature [120]. This theoretical limit has become the reference for experimental efforts. Indeed, among the TMDCs, the mobilities of $MoTe_2$ (2526 $cm^2 \cdot V^{-1} \cdot s^{-1}$), WS_2 (1103 $cm^2 \cdot V^{-1} \cdot s^{-1}$), and WSe_2 (705 $cm^2 \cdot V^{-1} \cdot s^{-1}$) were predicted to be greater than the room-temperature phonon-limited electron mobility in the monolayer [121], as a result of low effective mass. However, as shown in Table 3, the reported experimental mobility to date is much lower than that found via theoretical prediction.

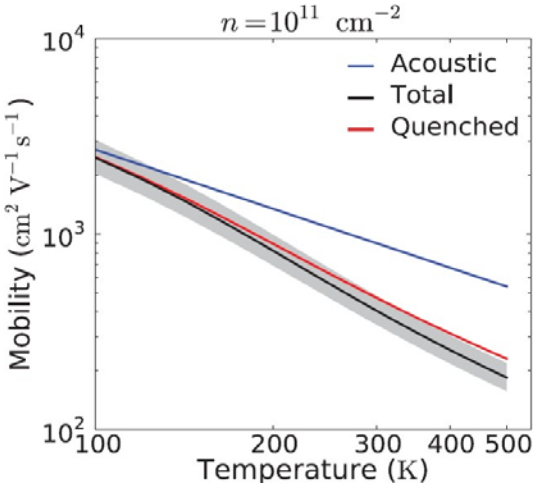

Figure 4. The temperature dependence of the mobility at carrier density $n = 10^{11}$ cm^{-2} calculated with the full collision integral. For comparison, the mobility in the presence of only acoustic deformation potential scattering with the temperature dependence is shown by blue line. The (gray) shaded area shows the variation in the mobility associated with a 10% uncertainty in the calculated deformation potentials. Reproduced with permission from [120], American Physical Society, 2012.

The pioneer work on FETs based on monolayer MoS_2 was demonstrated by Radisavljevic et al. in 2011, as shown in Figure 5 [82]. The reported performance includes an excellent on/off current ratio (~10^8), greater mobility (>200 $cm^2 \cdot V^{-1} \cdot s^{-1}$), an ideal low subthreshold swing (74 mV/dec), and smaller off-state currents (25 fA/μm). Here, a mechanical exfoliated monolayer MoS_2 (0.65 nm) was used as the transport channel and was covered by 30-nm-thick HfO_2, which served as the top-gated dielectric layer. The same configuration was also used in FETs with channels made of monolayer WSe_2 covered by ZrO_2 dielectrics. These FETs also exhibited high room-temperature mobility (~250 $cm^2 \cdot V^{-1} \cdot s^{-1}$), a good subthreshold swing of ~60 mV/dec, and a high on/off ratio of 10^6 [115].

It is believed that the encapsulation of 2D-TMDCs by using high dielectric materials (e.g., Al_2O_3 and HfO_2) is critical for achieving high mobility. Authors have suggested that the introduction of high-k dielectrics would strongly dampen the Coulombic scattering in 2D materials due to the dielectric screen [122]. This mobility increase in conjunction with dielectric deposition was also observed in multilayer MoS_2 [46] and monolayer MoS_2 with polymer electrolytes [100]. The scattering rate is related to the scattering mean free path and the impurity density (i.e., the impurity spacing). Therefore, the charge impurity must be appropriate such that the scattering mean free path is on the same or small order of the phonon mean free path. Therefore, a minimum impurity concentration of 5×10^{11} cm^{-2} is need to dominate phonon scattering [120], which corresponded to the heavy doping by using top-gated

dielectric materials. The similar mobility improvement due to such dielectric engineering has been reported earlier for graphene [123–125].

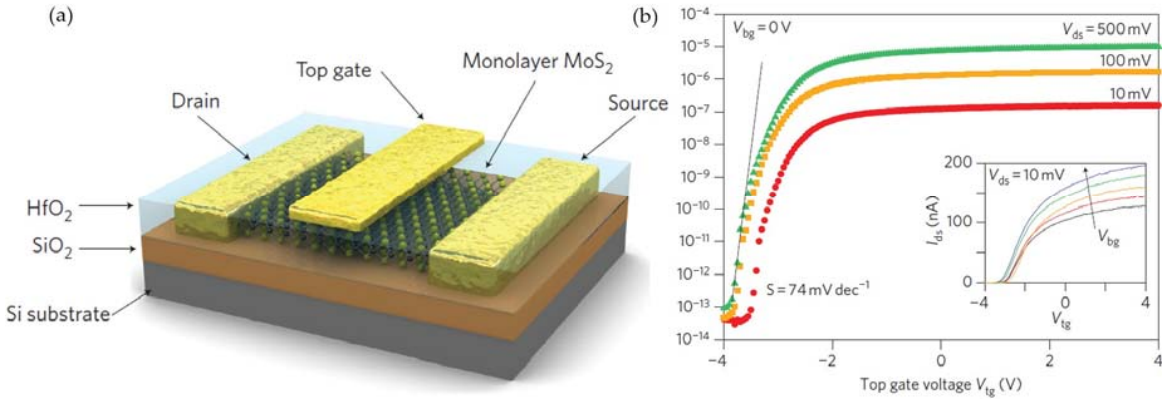

Figure 5. (**a**) Three-dimensional schematic view of the monolayer MoS_2 transistors. Top gate width and length are 4 um and 500 nm, respectively. (**b**) I_{ds}–V_{tg} curve recorded for V_{ds} ranging from 10 to 500 mV. Measurements were performed at room temperature with the back-gate grounded. The device can be completely turned off by changing the top gate bias from −2 to −4 V. For V_{ds} = 10 mV, the I_{on}/I_{off} is > 1×10^6. For V_{ds} = 500 mV, the I_{on}/I_{off} is > 1×10^8 while the subthreshold swing 74 mV/dec. Inset: I_{ds}–V_{tg} for values of V_{bg} = −10, −5, 0, 5, and 10 V. Reproduced with permission from [82], Nature Publishing Group, 2011.

On the other hand, the effects of gate configuration on charge mobility were also studied for FETs based on monolayer MoS_2. Top-gated geometry allows for a lower turn-on voltage, and the integration of multiple devices on the same substrate. Top gate configuration also had the effect of quenching the homopolar phonon mode, which has contributed to a mobility enhancement of 70 $cm^2 \cdot V \cdot s^{-1}$ at room temperature [120]. However, the measured exponent γ factors in the temperature dependence mobility, $\mu = T^{-\gamma}$, are between 0.3 and 0.78 for top-gated devices [126]. These values are much smaller than the theoretically predicted value of 1.52 for monolayer MoS_2 [120] or 2.6 for TMDC bulk crystals [33]. These results suggest that other mechanisms, rather than the quenching of the homopolar phonon, such as the surface roughness scattering created during synthesis, exfoliation, and transferring processes, are affecting the mobility of monolayer MoS_2 in the top-gated devices [127].

In addition, the Schottky barrier height between the electrodes and 2D TMDCs is known to affect carrier mobility of devices. The metals used for electrodes are claimed to define the height of the Schottky barrier associated with their work function. However, Theoretical calculations have shown 2D-TMDCs tend to form high Schottky barriers (0.03 eV to 0.8 eV) with common metals [128–131]. Several experimental practical attempts by inserting 2D layers (Graphene [132,133], hBN [134], Nb doped TMDCs [135], MoO_3 [136]) or thin film (MgO [137], TiO_2 [138]) between TMDCs and metals have been made to reduce Schottky contacts. Besides the handling of TMDC/metal junctions, chemical/electostatic-doping [69,115] and phase-patterning [139–142] are two successful methods of modifying the electrical properties of channel by reducing contact resistance. It was also reported that in situ annealing at 120 °C for 20 h in vacuum (~10^{-6} mbar) could increase the mobility due to the reduction of Schottky barrier. By this approach, an intrinsic mobility of 1000 $cm^2 \cdot V^{-1} \cdot s^{-1}$ were observed for both monolayer and bilayer devices based on MoS_2 [104].

Theoretical simulation has been investigated for the performance limits of an FET with a 15-nm-long MoS_2 gate length [96]. It has been reported that FETs based on MoS_2 can offer a subthreshold swing as low as 60 mV/dec and a current on/off ratio as high as 10^{10}. The ballistic regime of this device can be as high as 1.6 mA/μm, and the drain-induced barrier lowering (DIBL) is as small as 10 mV/V even with a very short channel length [96]. Thus, TMDCs transistors have the potential to overcome the short-channel effects because of the enhanced gate effect due to their

atomic-scale thickness. A similar simulation was reported based on a two-gate MOSFET model with 2D-Silicon and different 2D-TMDCs. Among them, only the monolayer WS_2 transistor outperform the 2D silicon and other monolayer TMDC devices in terms of ON-current by about 28.3% [95]. However, these predictions did not consider the effects of edges on the transport properties and therefore require experimental verification.

It should be noted that high transconductance FETs based on monolayer MoS_2 with full-channel gates were demonstrated experimentally [103]. As shown in Figure 6a, at low bias V_{ds} = 1 V, the drain–source conductance is close to 0 (g_{ds} < 2 μS/μm, $g_{ds} = \frac{dI_{ds}}{dV_{ds}}$), which means the channel current saturation occur. As shown in Figure 6b, these FETs offer high transconductance $g_m = \frac{dI_{ds}}{dV_{tg}}$ (maximum transconductance g_m = 34 μS/μm for V_{ds} = 4 V). Furthermore, it was demonstrated that the electrical breakdown of the monolayer MoS_2 was recorded at a current density of 5×10^7 A/cm^2, exceeding the current-carrying capacity of Cu by 50 times.

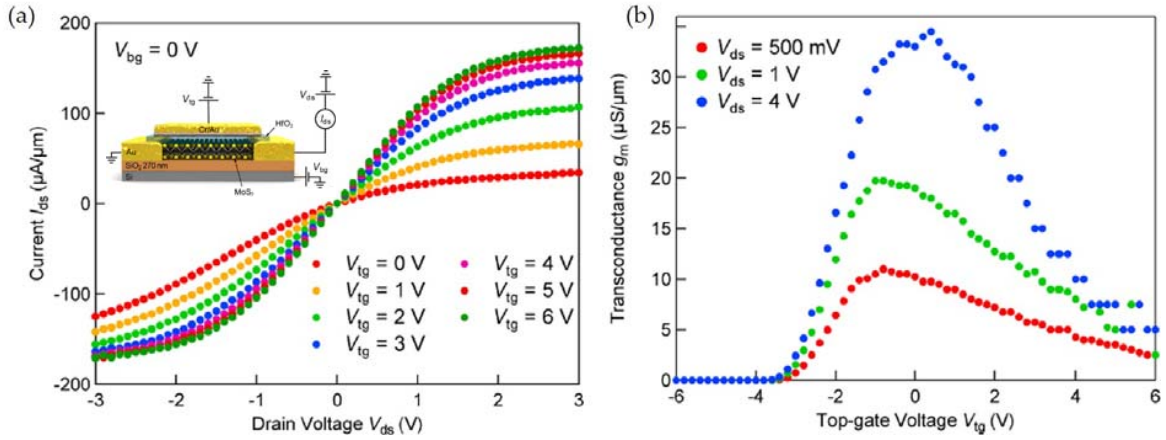

Figure 6. Performance of a high-transconductance MoS_2 FET. (**a**) I_{ds}–V_{ds} characteristics measured for different top-gate voltages V_{tg} from 0 to 6 V. Inset: Three-dimensional representation of the monolayer MoS_2 FET (**b**) Transconductance derived from I_{ds}–V_{ds} characteristics at V_{ds} = 0.5 V, 1 V, and 4 V. Reproduced with permission from [103], American Chemical Society, 2012.

The performance of monolayer TMDCs are also sensitive to random perturbations in the local environment. Current hysteresis under different ambient condition and light illumination was reported for FETs based on monolayer MoS_2. It was reported that current hysteresis increase steadily with the increase in humidity (RH), as shown in Figure 7a. It was proposed that such a hysteresis is due to the trapping states induced by the adsorption of water molecules on the surface of MoS_2. Similar hysteresis was observed when the device was under white light illumination, as shown in Figure 7b. This is attributed to the improvement of carrier concentration in the conduction channel due to photosensitivity [99]. This work indicates that controllable hysteretic behavior in MoS_2 FETs has the potential for humidity sensors and non-volatile memory devices.

The sensitivity of 2D TMDCs to the local environment has also contributed to flicker noise. The $1/f$ noise from un-encapsulated FETs based on monolayer MoS_2 was explained by the Hooge parameter ranging between 0.005 and 2 in vacuum (<10^{-5} Torr) [143]. The noise amplitude was reported to reduce by an order of magnitude after annealing, revealing the significant influence of atmospheric adsorbates on the charge transport [144]. On the other hand, high-k dielectric for top gate configuration is known to reduce the drain current noise in both monolayer and multilayer MoS_2 FETs [94,145]. Additionally, the observation of low frequency generation-recombination noise at low temperature could be due to charge traps in the underlying SiO_2 substrate or mid-gap states in the monolayer MoS_2 [143,146]. On the other hand, FETs based on layered 2H-$MoTe_2$ flakes were investigated for their low frequency noise in both vacuum and air [147]. Similar experiments were also performed using

as-fabricated and aged MoS_2 transistors [148]. The measurements demonstrate that the flicker noise is determined by an intrinsic TMDCs conducting channel rather than the contact barriers. As a result, these noise metrics are expected to provide a unique diagnostic tool for researchers as they develop high-performance sensing applications.

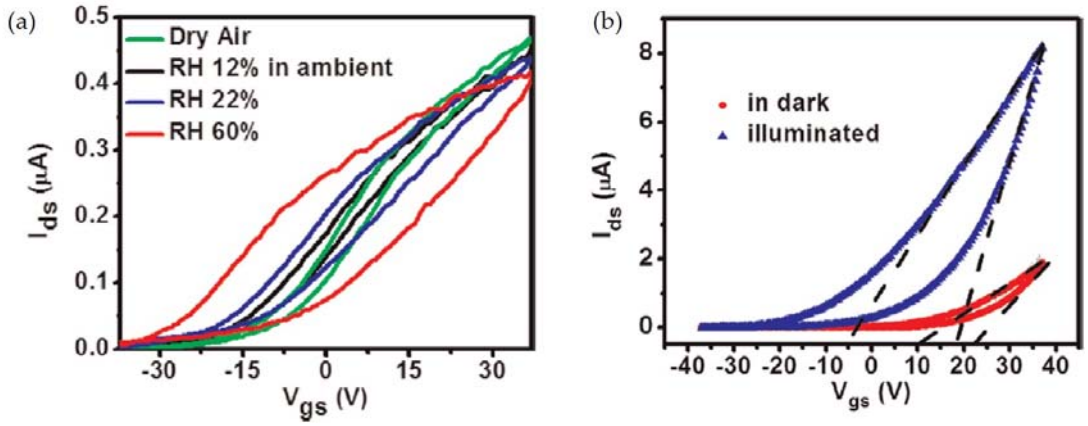

Figure 7. (**a**) Hysteresis in the monolayer MoS_2 transistor with controlled humidity under the sweeping rate of gate voltage at 0.5 V/s and V_{ds} = 0.5 V. (**b**) Hysteresis with different illumination conditions in a monolayer MoS_2 transistor. Blue dots are under global white illumination (0.7 mW/cm^2), and red dots are in the dark. The intersections between the dashed lines, and y = 0 show the threshold voltages. Reproduced with permission from [99], American Chemical Society, 2012.

The effects of substrates on the performance of FETs constructed by monolayer CVD TMDCs were investigated [70,106,108]. Results suggest that these FETs offer similar electrical performance to devices based on exfoliated TMDCs. This may imply that FETs based on CVD TMDCs can be fabricated on flexible substrates, enable their applications in flexible, transparent, 2D electronic devices. The development of CVD synthesis methods for obtaining large areas of TMDCs has become important for wafer-scale device fabrication.

Finally, FETs based on monolayer TMDC alloys were also investigated. These FETs were based on an $MoWSe_2$ monolayer ($Mo_{1-x}W_xSe_2$, $0 \leq x \leq 1$), mechanically exfoliated by Scotch tape. It was demonstrated that these FETs exhibit n-type transport behavior with on/off ratios >10^5 [149].

2.3. Ambipolar Transistors with TMDCs

Ambipolar transport was demonstrated in electric double-layer transistors (EDLTs) based on thin-flake MoS_2 (10 nm) using an ionic liquid as the gate to reach extremely high carrier densities of 1×10^{14} cm^{-2} [150]. The charge transfer curves of such ambipolar devices are shown in Figure 8b. For EDLTs using bulk and thin MoS_2, the I_{DS} was increased with positive V_G, corresponding to the behavior of an n-type semiconductor transistor. In contrast to its commonly known property as an n-type semiconductor in Table 2, when the V_G turn to negative bias, an obvious p-type transport was observed to start at -1 V in the EDLT made of thin flake MoS_2. There was no significant change in current in the EDLT made of bulk MoS_2. This phenomenon indicates that hole transport is comparable to electron transport in thin-flake MoS_2. Hall effect measurements also revealed the mobility of 44 and 86 cm^{-1}/V^{-1}s^{-1} for electron and hole, respectively. The hole mobility is even twice the value of the electron mobility. However, the on/off ratio in this device was just >100, much lower than those reported for FETs based on monolayer MoS_2 [82], mainly because of the finite off-current passing through the thin flakes. The greater hysteresis at lower temperature (220 K) in Figure 8a was attributed to the slow motion of ions. A stable p–n junction was also found in the MoS_2 EDLTs [151].

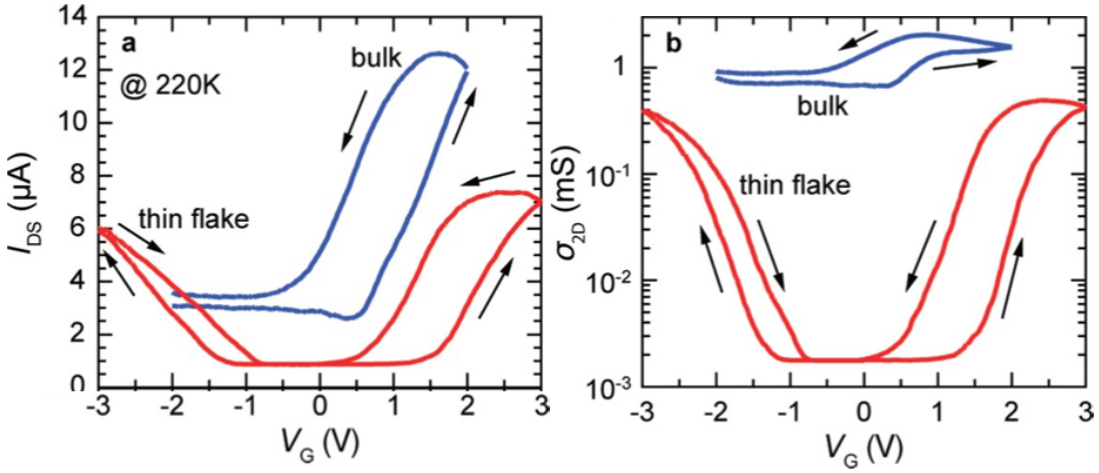

Figure 8. Transfer curve of bulk (1000 μm × 500 μm × 10 μm) and thin-flake (20 μm × 20 μm × 15 nm) MoS_2 EDLTs. (**a**) Change in the channel current (I_{DS}) as a function of gate voltage (V_G). (**b**) Change of sheet conductivity (σ_{2D}) as a function of gate voltage (V_G). Channel voltage (V_{DS}) is 0.2 V for both devices. Reproduced with permission from [150], American Chemical Society, 2012.

The electrical double layers (EDLs) consist of a narrow spatial charge doublet that simulates a capacitor to accumulate carriers. The use of EDLTs help to investigate the ambipolar transport in TMDCs, such as WS_2 [20,66], $MoSe_2$ [152], WSe_2 [69,116,117], and $MoTe_2$ [62]. In addition, the EDLT channel was shown to form at the interface of TMDC/ionic liquid, where the trapping state between the TMDCs and the substrates was reduced. As a result, the similar ambipolar behavior were also reported in conventional FETs based on TMDCs on dielectric materials (e.g., MoS_2 on PMMA [52], WS_2 on Al_2O_3 [65], and WSe_2 on hexagonal boron nitride (h-BN) [153]).

Ambipolar EDLTs based on multilayer WSe_2 with a high on/off ratio $>10^7$ at 170 K and large carrier mobility (electron mobility to 330 $cm^2 \cdot V^{-1} \cdot s^{-1}$ and hole mobility to 270 $cm^2 \cdot V^{-1} \cdot s^{-1}$) at 77 K were reported [69]. As shown in Figure 9, it was obtained by using a low-resistance ionic liquid gate with hBN encapsulation and graphene contacts on the WSe_2. It was suggested that a drastic reduction of the Schottky barriers between the channel and the graphene contact electrodes by ionic liquid gating is needed in order to observe the intrinsic, phonon-limited conduction in both the electron and hole channels. However, the EDLTs still require much effort in atomic 2D-TMDC devices due to the integration, reliability, and low operating speed.

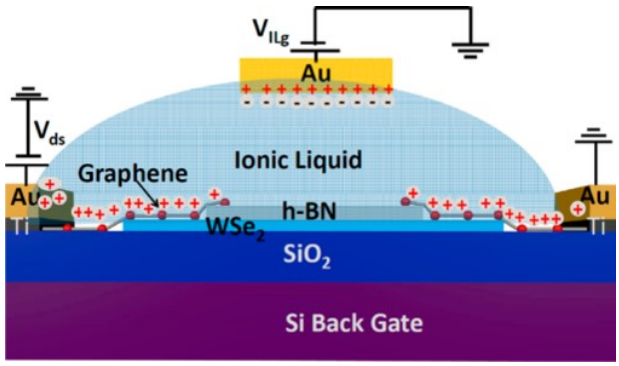

Figure 9. Schematic illustration of the structure and working principle of a hexagonal boron nitride (h-BN)/WSe_2 FET with ionic-liquid-gated graphene contacts. Reproduced with permission from [69], American Chemical Society, 2014.

In the case of conventional FETs, another method is using electrode metals with different work functions to control the transistor polarity. If the Fermi level of the electrode is close to the conduction band of the semiconductor, the electron injection becomes predominant. While the Fermi level is close to the valence band of the semiconductor, it translates into a hole injection. For example, due to the Fermi level of most metals close to the conduction band of MoS_2, the carrier of MoS_2 FETs were dominated by electrons [49]. With the exception of Pd [154] and Pt [131], which acted as both source and drain electrodes, MoS_2 transistors show p-type behavior. Furthermore, WSe_2 was found to exhibit ambipolar behavior by using different metals as the source and drain electrodes [155]. Alternatively, chemical doping on the surface of TMDCs (e.g., NO_2 on WSe_2 [115], K on WSe_2 [156]) by thinning the Schottky barrier width for carrier injection was also performed to study ambipolar behavior. However, the polarity of FETs was fixed after device fabrication.

The ambipolar transport were also discovered in $MoSe_2$ [56], $MoTe_2$ [58], and WSe_2 [153,157–159] under different electrostatic fields. This phenomenon was attributed to the formation of two back-to-back Schottky barriers rather than only the channel conductance. Thus, transistors can function as ambipolar transistors, and the transistor polarity can be reversed by an electric signal. A doping-free ambipolar transistor made of multilayer $MoTe_2$ is proposed in which the transistor polarity (p-type and n-type) is electrostatically controlled by dual top gates as shown in Figure 10. One of the gates was used to determine the transistor polarity, while the other gate was used to modulate the drain current [160].

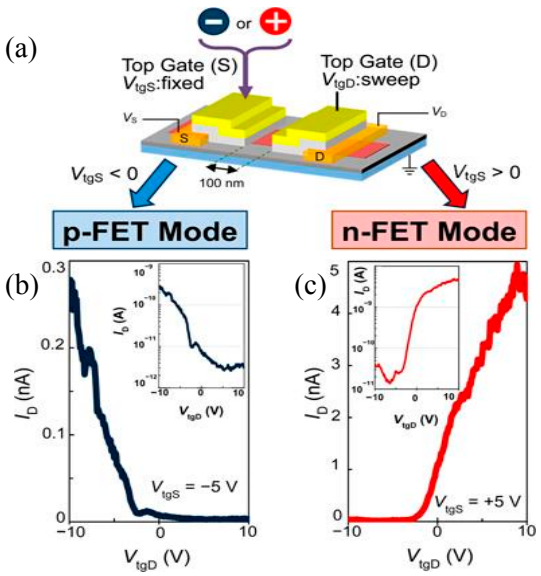

Figure 10. (**a**) Schematic of the $MoTe_2$ ambipolar transistor structure. The gap between the two top gates is 100 nm. (**b**) Experimental results for on/off operation in the p-FET mode (V_{tgS} = –5 V). The inset is a logarithmic plot. (**c**) Experimental results of an on/off operation in the n-FET mode (V_{tgS} = 5 V), with a logarithmic plot provided in the inset. Reproduced with permission from [160], American Chemical Society, 2015.

Overall, the demonstration of both n-type and p-type transport will be useful for applications that are more complicated such as CMOS logic circuits and p–n junction optoelectronic devices.

2.4. Transistors with Vertical Hetero-Structures

Due to the relatively weak van der Waals bonding between layers of TMDCs, and the absence of surface dangling bonds, the stacking of TMDCs layers and other 2D materials multilayers can energetically form heterostructures or heterojunctions [161,162]. Actual devices have been demonstrated as summarized in Table 4. For example, vertical heterojunction devices consisting

of graphene (Gr) and 2D-TMDCs with appropriate bandgaps were suggested to resolve the low on/off-current ratio of graphene FETs and to achieve a high on–current density at extremely low operating voltage, which is difficult to accomplish in TMDC FETs. The use of graphene in vertically stacked devices was demonstrated as allowing electric field to penetrate through the heterostructures [163]. These vertical heterojunctions created Schottky barriers at the interfaces, where the TMDCs functioned as semiconductor instead of insulator (e.g., hBN) tunneling [164], which achieved a greater channel current while retaining a high on/off ratio [165–168].

As summarized in Table 4, vertical Gr/TMDCs heterostructures have been fabricated since 2012 [165–181]. For example, vertical Gr/MoS_2 FETs can achieve a high on/off ratio above 10^5 with on–current density as high as 5×10^4 A/cm^2 [171]. In addition, a similar vertical FET based on Gr/WS_2/Gr structure was reported with an on/off ratio as high as 10^6 even at room temperature [166]. At lower temperature (180 K), an extremely high on/off ratio of 5×10^7 was obtained in Gr/WSe_2 FETs [175].

Unlike n-type semiconductors, MoS_2, $MoTe_2$, and WSe_2 show p-type behavior, as summarized in Tables 2 and 3. Hence, multiple MoS_2/WSe_2 vertical heterostructures have been reported as p–n junctions [182–184]. A heterojunction based on p-type black phosphorus (BP) and n-type monolayer MoS_2 has also been demonstrated [185].

Although the study of transistors with vertical heterojunctions is still in its infancy, unique electrical and optical junction properties are expected to be found by combining various 2D materials with different work functions, bandgaps, and electron affinities. In fact, in addition to FETs, various TMDCs and other 2D materials heterojunction-based devices have recently been reported, including solar cells, photodetectors, LEDs, and memory devices, which will be discussed in following chapters.

Table 4. Summary of transistor performances with different vertical heterostructures. Graphene and boron nitride nanosheets are represented as Gr and hBN, respectively. APTES: (3-aminopropyl) triethoxysilane.

Materials and Structure	On/Off Ratio	On-Current Density (A/cm^2)	Off-Current Density (A/cm^2)	Source–Drain Voltage (V)	Reference
Gr/MoS_2/Ti	60 (290 K) 10^4 (150 K)	60	0.5	0.1	[165]
hBN/Gr/WS_2/Gr/Au	10^6	200	0.001	0.2	[166]
Gr/MoS_2/Ti/Au	10^2	150	<1	0.01	[169]
Gr/MoS_2/Ti/Au	10^3	5000	12.5	7	[170]
Gr/MoS_2/Ti/Au	10^5	5×10^4	0.1	0.5	[171]
Gr/MoS_2/Ti/Au	3	50	1.5	0.05	[172]
Gr/$MoSe_2$/Ti/Au	10^5	1000	0.05	0.5	[167]
Au/Gr/MoS_2	10^6	1000	0.0014	0.5	[173]
Gr/WSe_2/Provskite/Gr	10^6	<1	$<10^{-5}$	–1	[174]
Gr/MoS_2/Au	10^4	3000	0.3	0.5	[168]
Gr/WSe_2/Au	10^4	3100	0.31	0.5	
APTES/Gr/WSe_2/Pt	3×10^4 (300 K) 5×10^7 (180 K)	11	0.001	0.1	[175]

3. Optoelectronic Devices

Optoelectronic devices are important to generate, detect, and control light, including photovoltaic devices (solar cells), light-emitting diodes (LEDs), photodetectors, and lasers. The electronic band structures of semiconductors decide for their possibility to absorb and emit light. For indirect bandgap semiconductors, additional phonons must be absorbed or emitted to conserve the momentum, which is much less efficient. Almost all MoX_2 and WX_2, TMDCs (X is a chalcogen atom) are expected to follow a similar indirect to direct bandgap transformation with decreasing layer thickness. The bandgap of

these TMDCs covering an energy range of 1–2.1 eV, as shown in Table 1, are therefore especially suitable for optoelectronic applications [186]. Because of their atomically thin and strong stiffness [187], TMDCs are promising for flexible and transparent optoelectronics. As summarized in Figure 11, TMDCs offer good mobility in between those of organic materials and III–V semiconductors. A band gap near the Shockley–Quessier limit (~1.3 eV) and high mobilities are expected to lead to high-efficiency photovoltaic devices [188].

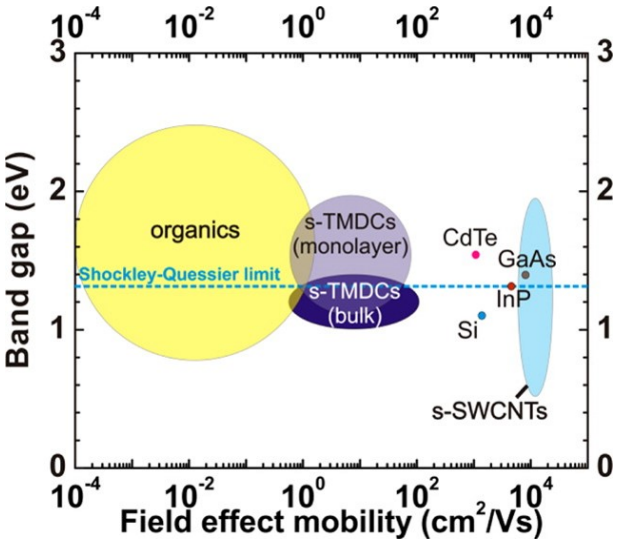

Figure 11. Bandgap vs. field-effect mobility of some important semiconductors used in optoelectronic devices. The dashed line is the band gap at ~1.34 eV while efficiency reach the Shockley-Quessier limit (~33.7%). Reproduced with permission from [188], American Chemical Society, 2014.

When irradiated with photons with an energy greater than that of the band gap, free electron/hole or bound electron–hole pairs (excitons) will be generated in the depletion region of semiconductors. The applied voltage or built-in electrical field could separate the bound excitons to generate flows of charge carriers that are called photocurrents. Hence, the p–n junction is the functional element of many optoelectronic devices, including solar cells, LEDs, and photodetectors. Devices with a combination of p-type Si and n-type MoS_2 were studied [189,190]. A p–n junction diode has been realized in MoS_2 EDLTs [151]. Similarly, the p–n junctions based on monolayer WSe_2 by electrostatic tuning were also reported [153,157–159].

3.1. Solar Cells

In Figure 12, TMDCs (MoS_2, $MoSe_2$, and WS_2) can absorb up to 5–10% incident sunlight in monolayer (thickness less than 1 nm). The sunlight absorption is one order of magnitude greater than general semiconductors such as GaAs and Si [176]. Early to 1997, Gourmelon et al. first reported the use of MoS_2 and WS_2—nanostructure absorbers in solar cells [191]. Photosensitization of TiO_2 were sensitized with WS_2 nanosheets (5 nm thick), which act as a stable absorber material [192]. Similarly, a bulk heterojunction (BHJ) solar cell made of TiO_2 nanoparticles and composites of monolayer/multilayer MoS_2 nanosheets with poly(3hexylthiophene) (P3HT) was demonstrated with 1.3% photo conversion efficiency [193]. The asymmetric Schottky junctions were demonstrated in a metal/MoS_2/metal structure, which resulted in photovoltaic devices with 0.7~2.5% power conversion efficiency (PCE) [154,194]. A greater work function difference between metals and n-type MoS_2 would generate a greater electric field in the depletion region of MoS_2. Recently, the p–n junction diodes based on TMDCs themselves were fabricated and achieved a light PCE of ~0.5%. When the device was operated as a photodiode (Figure 13), a photocurrent of 29 pA was obtained, which translates into

a photo-responsivity of 16 mA/W [157]. Furthermore, the monolayer MoS_2 on p-type Si substrates formed a p–n junction and operated in tandem mode with an external quantum efficiency of 4.4% [189].

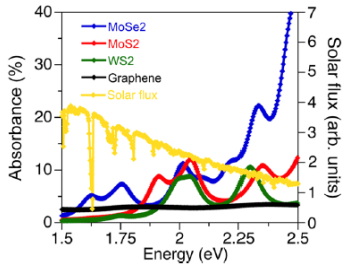

Figure 12. Bandgap absorbance of three TMD monolayers and graphene, overlapped to the incident AM1.5G solar flux. Reproduced with permission from [176], American Chemical Society, 2013.

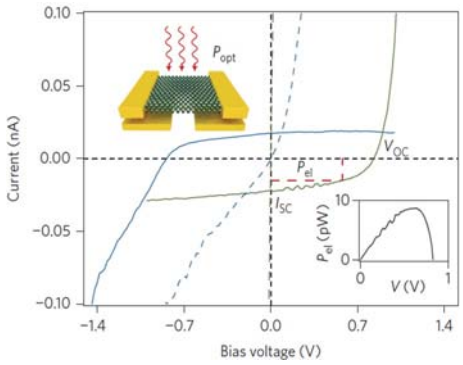

Figure 13. I–V characteristics of monolayer WSe_2 photodiode under a halogen lamp with 1400 W/m^2. The biasing conditions are p–n (solid green line; $V_{G1} = -40$ V, $V_{G2} = 40$ V), n–p (solid blue line; $V_{G1} = 40$ V, $V_{G2} = -40$ V), and p–p (dash blue line; $V_{G1} = V_{G2} = 40$ V). The red dashed rectangle in the main panel shows the maximum power conversion efficiency area (P_{el}). Top inset: Schematic of WSe_2 monolayer device with split gate electrodes. Lower inset: electrical power (P_{el}) versus voltage under incident illumination. Reproduced with permission from [157], Nature Publishing Group, 2014.

Highly efficient photocurrent generation was also demonstrated in vertical heterostructures. Studies on Schottky junction solar cells consisting of a graphene–MoS_2 stack suggested a power conversion efficiency of 0.1–1% [176], while p–n junctions of MoS_2/WS_2 [176] and MoS_2/WSe_2 [182] were 0.4–1.5% and 0.2%, respectively. In addition, a special vertical p–njunction made of p-type MoS_2 (CHF_3 plasma treated) and n-type MoS_2 was fabricated successfully. This MoS_2 heterostructure-based solar cell achieved up to 2.8% PCE under AM1.5G illumination [195].

However, the efficiency of solar cells based on ultrathin TMDCs is limited by the loss of absorption under the thickness limitation [196]. Calculations suggest that a monolayer of TMDCs could absorb as much sunlight as 50 nm of Si and generate electrical currents as high as 4.5 mA/cm^2 [176]. To improve the absorption of light, plasmonic enhancement technics were introduced by decorating Au nanoparticles on MoS_2 nanosheets [197]. The Au nanoparticles can produce an enhanced local optical field on an MoS_2 phototransistor device. A similar phenomenon was also investigated in the WS_2/graphene and WSe_2/graphene heterostructures, leading to enhanced photon absorption [177,178]. Alternatively, multi-junction solar cells with different bandgaps can convert different portions of the solar spectrum to reduce absorption loss [196,198]. On the other hand, a continuous bandgap tuning by strain was demonstrated [199]. A photovoltaic device made from a strain engineered MoS_2 monolayer will capture a broad range of the solar spectrum and concentrate charge carriers. These structures can also potentially be constructed using different TMDCs with varying bandgaps, which range from the visible to the near-infrared (NIR).

3.2. Light-Emitting Diodes

Light-emitting diodes (LEDs) is another type of application based on p–n junctions. Electrons and holes are separated by doping material into a p–n junction. They recombine to release energy as photons in response to electrical bias voltages. This effect is called electroluminescence (EL). Table 5 summarizes performances of LEDs constructed by various TMDCs. As direct bandgap materials (1–2 eV), monolayer 2D-TMDCs are ideal for ultrathin and flexible light-emitting layers. One of the earliest light emission studies on TMDCs was one in which MoS_2/Au nano-contacts were stimulated by scanning tunneling microscopy (STM) [200]. EL behavior was also found from exfoliated SnS_2 incorporated into a composite polymer semiconductor, but MoS_2 resulted in no light emission [201].

Table 5. Performance of light-emitting diodes (LEDs) with various transition metal dichalcogenide (TMDC) structures.

Materials and Structure	Type	EL Peak (nm)	EL Efficiency	Reference
Au/Cr/MoS_2/Cr/Au	Schottky junction	685	0.001%	[202]
Ti/WSe_2/Ti	p–i–n junction	740	0.06%	[203]
Au/Pd/WSe_2/Ti/Au	p–n junction	800	0.1%	[157]
Au/WSe_2/Pt	p–n junction	752	0.2%	[158]
Au/WSe_2/Au	p–n junction	750	0.1%	[159]
Ni/MoS_2/WSe_2/Au	p–n junction	800	12%	[184]
Gr/hBN/MoS_2/hBN/Gr	Tunnel junction	678	8.4%	[204]
Gr/hBN/WS_2/hBN/Gr		620	1.32%	
Gr/hBN/WSe_2/hBN/Gr		738	5.4%	

The result of EL in MoS_2 was reconfirmed by a monolayer MoS_2 FET, shown in Figure 14. A Schottky barrier between MoS_2 and Cr/Au was formed with a height of 100 to 400 meV. By comparing the absorption, photoluminescence (PL) and EL of the same MoS_2 monolayer, they all involved the same energy state at 1.8 eV (685 nm) [202]. WS_2 were also used to fabricate light-emitting transistors based on similar Schottky barrier between TMDCs and metals [20].

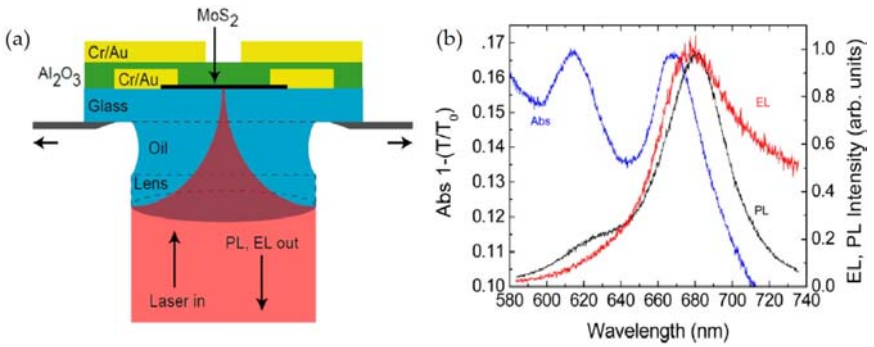

Figure 14. (**a**) Schematic of a top-gated MoS_2 FET and the optical setup. (**b**) Absorption (Abs), EL, and PL spectra on the same 1L-MoS_2. Reproduced with permission from [202], American Chemical Society, 2013.

More LEDs based on p–n junctions have been shown to have a high light emission efficiency (~1%). Homojunction-based LEDs formed by electrostatic doping of monolayer WSe_2 resulted in a maximum EL efficiency of 1% [157–159]. However, the difficulty in doping has prevented the fabrication of LEDs by monolayer TMDCs. Moreover, based on the type II heterojunction design as previous mentioned in

Section 3.1, excitonic EL was observed via a n-type monolayer MoS_2 and p-type Si heterojunction [189]. In addition, an EL spectrum in a vertically stacked MoS_2/WSe_2 heterojunction (n-type for MoS_2 and p-type for WSe_2) was also obtained with a 12% external quantum efficiency [184].

Furthermore, a new design of LEDs was introduced by stacking graphene (electrode), hexagonal boron nitride (hBN) (tunneling junction), and various semiconducting monolayers (light emitter) into complex sequences. These devices have exhibited an extrinsic quantum efficiency of nearly 10%, and the emission can be tuned over a wide range of frequencies by appropriately choosing and combining 2D TMDCs [204,205]. However, as compared to the commercial organic LEDs with an emission efficiency (external quantum efficiency) of 15–40% [206] and of ~50% in LED light bulbs, there are significant needs to further improve the performance TMDC-based LEDs. For example, more investigation on doping and surface engineering, encapsulation, and device design for band structure engineering are desired to further improve the efficiency of these LEDs [188].

Recently, LEDs have combined vertical tunnel junctions, and lateral p–n junctions have also been exploited. Such lateral LED devices were constructed by two graphene transparent electrodes, two hBN tunnel barriers, and one monolayer WSe_2. Two separated back-gates were utilized to electrostatically define the p–i–n junction in WSe_2 [203,207]. A single photon emitter in a WSe_2 LED based on a p–i–n junction was reported; a narrow EL peak (width < 300 μeV) at 1.704 eV (728 nm) under low current (~100 nA) and low temperature (~5 K) was observed [207].

3.3. Photodetectors

Photodetectors are light sensors with p–n junctions that convert photons into electrical current. The junction is usually covered by a window with anti-reflective coatings. The absorption of photons will create electron–hole pairs in the depletion region. Photodiodes and phototransistors are two major examples of such photodetectors. In terms of frequency response, photodiodes are much faster than phototransistors (ns vs. μs) and not sensitive to temperature fluctuation. Therefore, photodiodes usually work as solar cells and photoconductors. Phototransistors are transistors with the base terminal exposed instead of sending photocurrent into the base. Compared to photodiodes, phototransistors have a greater gain.

The application of TMDCs in photodetectors has been widely demonstrated. Basically, the metal–semiconductor–metal (M-S-M) structured photodetector is made of MoS_2 and amorphous silicon with response times of about 0.3 ms and a photoresponsivity of 210 mA/W when irradiated with green light [190]. By using a two-pulse photo-voltage correlation technique, an ultrafast response of 3 ps was recorded in photodetectors constructed with monolayer MoS_2 [208]. A phototransistor made from mechanical exfoliated monolayer MoS_2 has also exhibited high photo-responsivity of 7.5 mA/W. By improved mobility and contact quality, an ultrasensitive monolayer MoS_2 photodetector was also fabricated [209]. The maximum external photo-responsivity was able to attain up to 880 A/W. As shown in Figure 15a, the drain current I_{ds} can increase upon light illumination. This device also showed a uniform increase in photo-responsivity as the illumination wavelength was reduced from 680 to 400 nm (Figure 15b). This suggests that monolayer MoS_2 photodetectors can be used for a broad range of wavelengths, between 400 and 650 nm. Phototransistors based on CVD-grown monolayer MoS_2 and multilayer WS_2 have also been demonstrated [210,211]. Photodetectors with high photo-responsivity (2.5×10^7 A/W) and external quantum efficiency (3168%) were fabricated by multilayer ReS_2 [75,78].

As it is a classic structure of TMDC-based photodetectors, the M-S-M configuration has been systematically studied. Schottky barrier modulation between 2D-TMDCs and electrodes is one of the promising methods of improving performance [212–214]. Phase transformation of MoS_2 (2H-1T) will also reduce the native Schottky barrier and increase photo-responsivity by more than one order of magnitude [215]. Self-assembled doping is another method of improving mobility and photo-responsivity [216]. After all, the photo-responsivity of the TMDC photodetectors

(~880 mA/W) [209] is much greater than that of graphene photodetectors (15.7 mA/W) [217], and the general response speed (~3 ps on MoS_2) [208] is relatively high (~50 ps on graphene) [218].

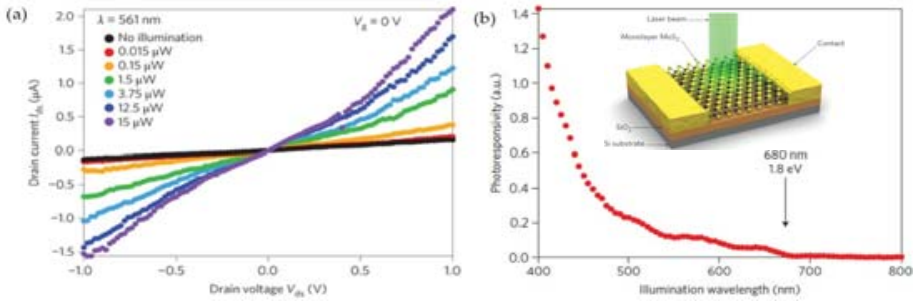

Figure 15. Performance of a monolayer MoS_2 phototransistor. (**a**) I_{ds}–V_{ds} characteristic of the device in the dark and under different illumination intensities. (**b**) Photoresponsivity of a similar monolayer MoS_2 device as a function of illumination wavelength. Inset: Three-dimensional schematic view of the monolayer MoS_2 photodetector and the focused laser beam used to probe the device. Reproduced with permission from [209], Nature Publishing Group, 2013.

The photothermoelectric effect also plays a considerable role in photo-responsivity [219]. In addition to photo-excited electron−hole pairs across the Schottky barriers at the TMDC/electrode interface, the carrier is also excited by light illumination based on temperature difference. The photovoltaic effect interface dominates in the accumulation regime, whereas the hot-carrier-assisted photothermoelectric effect prevails in the depletion regime for the multilayer MoS_2 photodetector [220]. Meanwhile, the photocurrent generation in monolayer MoS_2 is dominated by the photothermoelectric effect [221]. The photothermoelectric effect has also been studied in other TMDC-based photodetectors [153,222].

By using MoS_2 layers of different thicknesses, phototransistors can be tuned to absorb lights at different wavelengths, as shown in Figure 16 [198]. Furthermore, multilayer MoS_2 phototransistors have been demonstrated to response spectra range from ultraviolet (UV) to near-infrared (NIR) [223]. Similar bandgap tuning, by varying the number of TMDC layers, has also been applied for WS_2 [224].

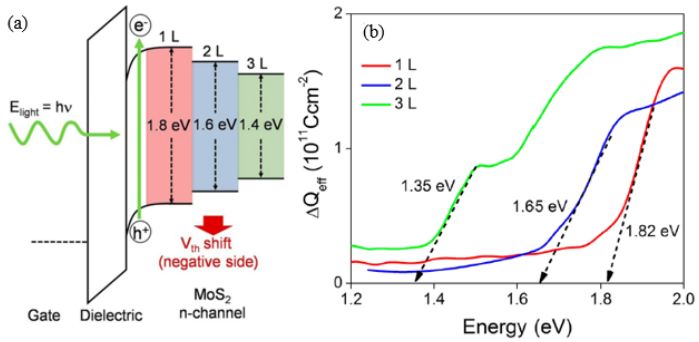

Figure 16. (**a**) The schematic band diagrams of ITO (gate)/Al_2O_3 (dielectric)/single-, double-, and triple-layer MoS_2 (n-channel) under the gate bias for carrier (electron–hole) accumulation. (**b**) Photon energy-dependent (ΔQ_{eff}) plots indicate the approximate optical energy gaps to be 1.35 eV, 1.65 eV, and 1.82 eV for trilayer, bilayer, and monolayer MoS_2 nanosheets, respectively. Reproduced with permission from [198], American Chemical Society, 2012.

Heterojunction fabrication can be performed to optimize the performance of 2D-TMDC photodetectors. Highly efficient photocurrent generation has been demonstrated in vertical heterostructures of Gr/TMDCs and Gr/hBN/TMDCs [177,225], where a maximum external quantum

efficiency was 55%, internal quantum efficiency was up to 85%, and the response speed was down to 53.6 μs [179]. The hBN/Gr/WSe_2 vertical heterostructure photodetectors have a superfast photo-response time of 5.5 ps [180]. Then, a photodetector with a WSe_2/Gr/MoS_2 heterostructure, which extends the absorption spectral range from 400 to 2400 nm [181].

In addition, atomically 2D-TMDCs still have physical limitations with light absorption, so the use of an absorption layer (e.g., R6G/PbS/perovskite) was applied on 2D-TMDC photodetectors [226–228].

3.4. Lasers

In photoluminescence (PL) devices, light emission will occur after absorbing photons at greater energy. The enhancement of PL quantum yield has been demonstrated in TMDC monolayers [16,229–232], although the yield difference between bulk and monolayer MoS_2 was relatively modest. The absolute PL intensity of the WS_2 and WSe_2 monolayers was 20–40 times greater than that of monolayer MoS_2 exfoliated from a natural crystal [22,231]. Compared to MoS_2, WS_2 and WSe_2 are better candidates for light emission devices.

However, the spontaneous emission efficiency of monolayer TMDCs is still low because the non-radiative recombination rate exceeds the spontaneous emission rate [233]. For monolayer MoS_2 on SiO_2 substrates, the non-radiative decay time is ~70 ps and the spontaneous emission lifetime is ~10 ns, as estimated at room temperature [234,235].

The enhancement of spontaneous emission could be achieved by two major strategies as shown in Figure 17a,b. One is to couple the TMDCs with a low Q-factor (~300) planar photonic crystal (PPC) [236,237]. The other one is to integrate TMDCs with distributed Bragg reflector (DBR) micro-cavities [238,239]. Recently, device performance based on monolayer WSe_2 was improved by using the former strategy. The as-fabricated PCCs had Q-factors of about 10^4. This led to a significant improvement of the Purcell factor, which is crucial for lasing. The optical pumping threshold was as low as 27 nW at 130 K [240].

Besides the Purcell enhancement of spontaneous emission, there are several critical challenges for achieving lasing using 2D TMDCs. For example, the large effective masses of charge carriers in MoS_2 result in high densities of states in both valence and conduction bands. MoS_2 with 1.8 eV bandgap requires carrier concentrations to push the quasi-Fermi levels into the corresponding bands to achieve population inversion [235]. The transition between the valence band and the conduction band-edge has a strong excitonic feature in such a monolayer TMDC system, including neutral and red-shifted charged excitons, allowing for the long-lived population inversion required, which has been studied in MoS_2 [241], WS_2 [242], and WSe_2 [243].

In addition, the limited gains and the lack of optical confinement and feedback within the monolayer TMDCs will hinder coherent light emission. There have been demonstrations that a strong optical confinement and an enhanced modal gain can be achieved by embedding 2D TMDCs at the interface between a free-standing microsphere and a microdisk [235,244], as shown in Figure 17c,d. The devices exhibited multiple resonant lasing peaks in the wavelength range of ~575–775 nm. In Figure 17d, the structure of an $S_{i3}N_4$/WS_2/HSQ microdisk with a diameter of 3.3 μm has two advantages: enhanced optical mode overlap and material protection. The lasing performance did not decay even after one year, as the sandwich structure protects the monolayer from direct exposure to air [244].

It was noted that the key to the lasing lies in the monolayer of the gain medium, which confines direct-gap excitons to within micro- or even nano-structures. The configuration allows for gain properties via external controls such as electrostatic gating and current injection, enabling optically or electrically pumped operation. These results show that the possibilities of these fabrication methods are scalable or designable, and compatible with integrated electronic circuits technologies. However, the performance of the device might be further improved by exploring surface passivation, doping, and strain engineering.

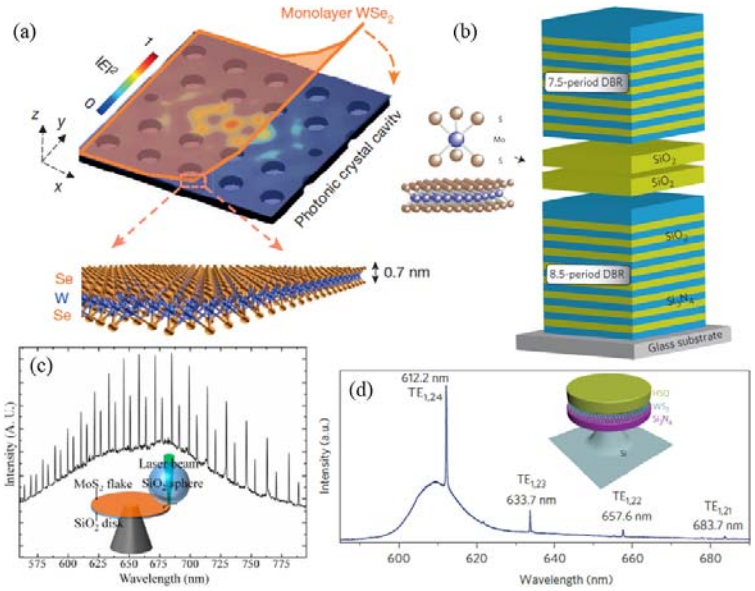

Figure 17. (**a**) Illustration of PPC architecture, where the electric-field profile (in-plane, x-y) of the fundamental cavity mode (pristine cavity before WSe_2 transfer) is embedded as the color plot. Reproduced with permission from [240], Nature Publishing Group, 2015. (**b**) Schematic of the DBR microcavity structure, a monolayer of MoS_2, sandwiched between two SiO_2 layers to form the cavity layer. Reproduced with permission from [239], Nature Publishing Group, 2014. (**c**) PL spectrum of the laser device with an excitation power of 30 mW at room temperature. Inset: Schematic configuration of the coupled SiO_2 microsphere/microdisk optical cavity with the incorporation of MoS_2 flake. Reproduced with permission from [235], American Chemical Society, 2015. (**d**) PL spectrum taken at 10 K when the pump intensity is above lasing threshold, showing whispering gallery modes (WGMs) at 612.2 nm, 633.7 nm, 657.6 nm, and 683.7 nm. Inset: Schematic image of the Si_3N_4/WS_2/HSQ micro sphere sandwich structure. Reproduced with permission from [244], Nature Publishing Group, 2015.

4. Integrated Circuits

4.1. Amplifiers and Inverters

An amplifier is a basic FET device that utilizes power from the supply to amplify the input signals to greater amplitudes. The operation of an analog small signal amplifier was demonstrated based on monolayer MoS_2 [102]. As shown in Figure 18a, the device consisted of two transistors that were integrated on a single monolayer MoS_2. The gate of one transistor (the switch) acted to provide input, while the gate of the other transistor (the load) was connected to the central lead and acted as the output/amplifier. The power supply of the amplifier V_{DD} was set to 2 V. The switch and load transistors connected in series are represented in Figure 18b. The switch transistor was first biased at a certain DC voltage to establish a desired drain current, shown as the Q-point (quiescent point) in Figure 18c. When a small sinusoidal AC signal $V_{in\text{-}AC}$ of amplitude $\Delta V_{in}/2$ was superimposed on the DC signal at the input, the output voltage ΔV_{out} oscillated synchronously with a phase difference of 180° with respect to $V_{in\text{-}AC}$. The slope of the red straight line in Figure 18c represented the gain

$$G = \frac{\Delta V_{out}}{\Delta V_{in}} > 4$$

of the amplifier at room temperature. By increasing the frequency of the AC signal, the gain was reduced to 1 at 2000 Hz, as shown in Figure 18d.

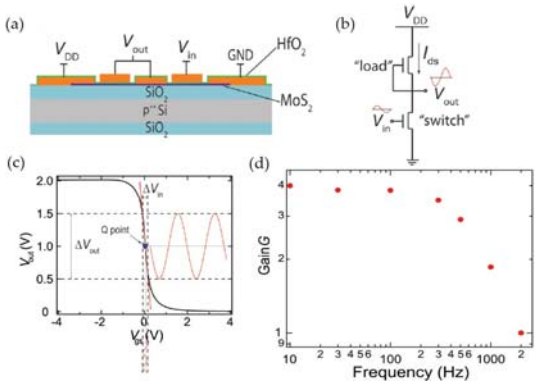

Figure 18. (**a**) Vertical cross section of the MoS_2 amplifier device. (**b**) Schematic drawing of integrated amplifier in common-source configuration. (**c**) Transfer characteristic of the integrated amplifier realized with two transistors on the same MoS_2 flake. (**d**) Voltage gain dependence on frequency of the small input signal. Reproduced with permission from [102], American Institute of Physics, 2012.

An important application of amplifiers is logic gate inverters (NOT gates). A NOT gate is designed to convert Logical 0 (low input voltage) to Logical 1 (high output voltage), and vice versa. The first monolayer MoS_2 inverter was reported in 2011 [97]. Up to six independently switchable transistors were fabricated on a single monolayer MoS_2 flake by lithographically patterning. As shown in Figure 19, an NOR-gate logic operation was also demonstrated, making them suitable for incorporation into digital circuits. A NOR gate is a universal gate that can be built in combinations to form all other logic operations.

On the other hand, radio frequency (RF) amplifiers and a logic inverter can be formed by integrating multiple MoS_2 transistors on quartz or flexible substrates. These devices have been demonstrated with an intrinsic gain over 30 and work in the GHz regime [90]. Several reports on amplifiers or inverters based on TMDCs were also reported with a voltage gain ranging from 1.45 to 27 [58,91,97,116,165,245–248]. Low-power consumption complementary inverters were also fabricated in the sub-nanowatt range [248], which is the most important advantage of CMOS inverters over single FET-type inverters.

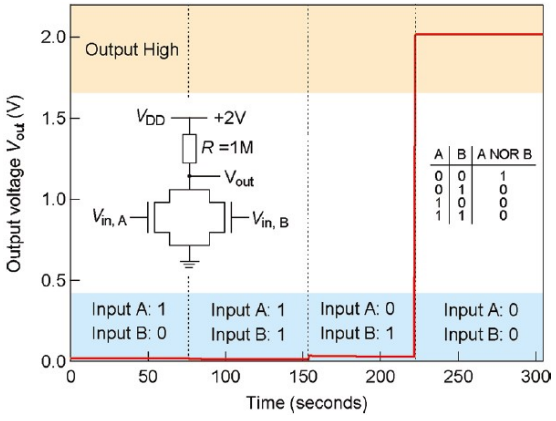

Figure 19. Demonstration of an NOR-gate logic circuit based on monolayer MoS_2 transistors. The output voltage V_{out} is shown for four different combinations of input states (1,0), (1,1), (0,1), and (0,0). The output is in the high state only if both inputs are in the low state. Left inset: The circuit is formed by connecting two monolayer MoS_2 transistors in parallel and using an external 1 MΩ resistor as a load. Reproduced with permission from [97], American Chemical Society, 2011.

4.2. Logic Circuits

Besides amplifier and inverters, more complicated devices of logic circuits have also been investigated. Wang et al. demonstrated complex integrated circuits based on bilayer MoS_2. These ICs consist of inverters, logical NAND gates, a static random access memory (SRAM), and a five-stage ring oscillator [249]. It is noted that an NAND gate is another basic logic gate with universal functionality. Any other type of logic gate can then be constructed with a combination of NAND gates. The schematic design and the optical micrograph of an NAND gate and SRAM circuit fabricated on the bilayer MoS_2 is shown in Figure 20. The SRAM was constructed from a pair of cross-coupled inverters as shown. This storage cell had two stable states (0 and 1) at the output. The flip-flop cell could be set to Logic State 1 (or 0) by applying a low (or high) voltage to the input.

The five-stage ring oscillator (Figure 21A,B) was constructed to assess the high frequency switching capability and for evaluating MoS_2 ultimate compatibility with conventional circuit architecture. The positive feedback loop in the ring oscillator resulted in a statically unstable system, and the voltage at the output of each inverter stage oscillated as a function of time as shown in Figure 21C. The output signal of the ring oscillator can also be measured in terms of its frequency power spectrum. As shown in Figure 21D, the fundamental oscillation frequency was at 1.6 MHz at V_{dd} = 2 V, corresponding to a propagation delay of 62.5 ns per stage [249].

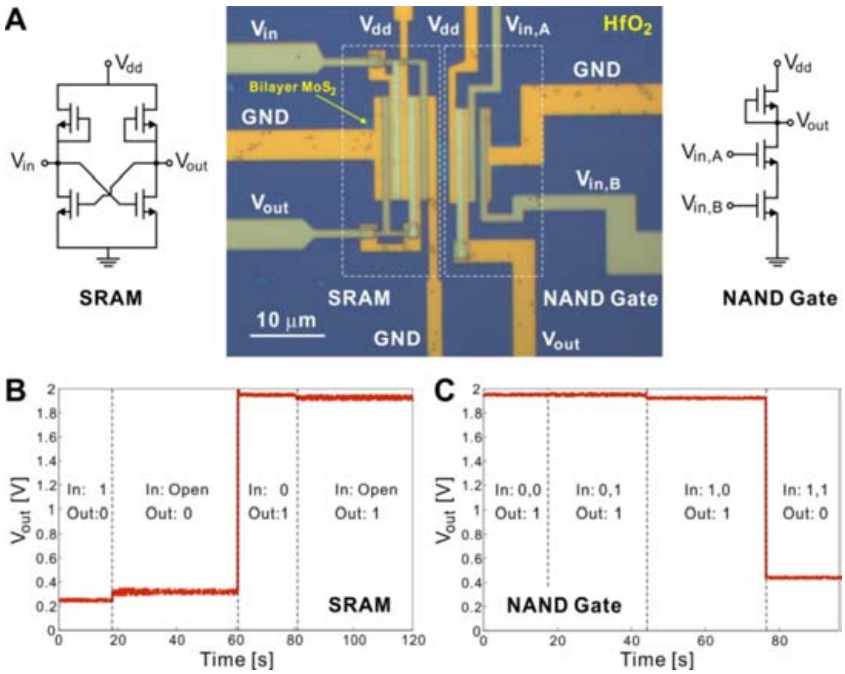

Figure 20. Demonstration of an integrated NAND logic gate and a static random-access memory (SRAM) cell on bilayer MoS_2. (**A**) Optical micrograph of the NAND gate and the SRAM fabricated on the same bilayer MoS_2 thin film. The corresponding schematics of the electronic circuits for the NAND gate and SRAM are also shown. (**B**) Output voltage of the flip-flop memory cell (SRAM). A Logic State 1 (or 0) at the input voltage can set the output voltage to Logic State 0 (or 1). In addition, the output logic state stays at 0 or 1 after the switch to the input has been opened. (**C**) Output voltage of the NAND gate for four different input states: (0,0), (0,1), (1,0), and (1,1). A low voltage below 0.5 V represents Logic State 0 and a voltage close to 2 V represents Logic State 1. Reproduced with permission from [249], American Chemical Society, 2012.

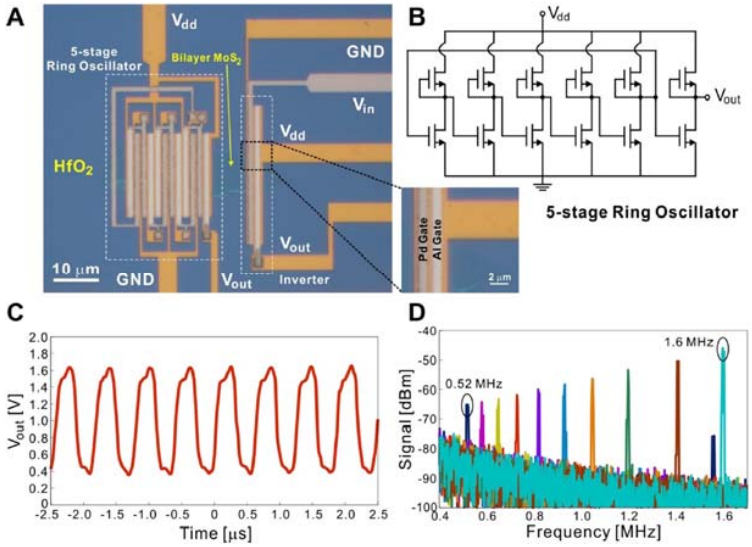

Figure 21. A five-stage ring oscillator based on bilayer MoS_2. (**A**) Optical micrograph of the ring oscillator constructed on a bilayer MoS_2 thin film. (**B**) Schematic of the electronic circuit of the five-stage ring oscillator. The first five inverter stages form the positive feedback loop, which leads to the oscillation in the circuit. The last inverter serves as the synthesis stage. (**C**) Output voltage as a function of time for the ring oscillator at V_{dd} = 2 V. (D) The power spectrum of the output signal as a function of V_{dd}. From left to right, V_{dd} = 1.15 V and 1.2 to 2.0 V in steps of 0.1 V. The corresponding fundamental oscillation frequency increases from 0.52 to 1.6 MHz. Reproduced with permission from [249], American Chemical Society, 2012.

4.3. Memory Devices

Memory cells are more basic building blocks of integrated digital electronics. In fact, graphene-based nonvolatile memory devices were studied earlier because of the high carrier mobility. However, graphene memory devices typically exhibited very low program/erase (P/E) current ratios up to 5.5 due to the absence of an energy bandgap. To overcome this limitation in graphene-based memory devices, TMDCs with a sufficient bandgap was proposed as a channel material for nonvolatile memory devices. The TMDC FETs showed a high on/off-current ratio and have the potential to enhance the P/E ratio in nonvolatile memory systems. The first nonvolatile memory cell based on TMDCs was demonstrated in 2012 with monolayer MoS_2 [101]. The P/E ratio can reach 5×10^3 at 1 V, as shown in Table 6.

Table 6. Performance of memory devices based on TMDCs and other materials.

Materials	P/E Ratio	Endurance (Cycles)	Retention (s)	Operating Voltage(V)	Reference
MoS_2 (with PZT)	5×10^3		10^3	1	[101]
	10^4	500	10^4	0.1	[250]
	10^4	120	2×10^3	0.05	[251]
Graphene/MoS_2	10^4	120	2×10^3	0.05	[252]
Graphene/hBN/MoS_2	10^5	120	1.4×10^3	0.05	[253]
	10^5	10^5	10^4	8	[254]
MoS_2/hBN/BP	50	40	10^3	0.05	[113]

Furthermore, nonvolatile memory devices that combine graphene with monolayer MoS_2, which reduced the operation voltage (V_{ds}) to 0.05 V, have been demonstrated [252]. As shown in Figure 22a, monolayer MoS_2 is used as the semiconducting channel with graphene stripes as the electrodes in FET geometry. A piece of multilayer graphene (MLG), separated by a 6-nm-thick tunneling HfO_2 layer

from the monolayer MoS_2 channel was used as the floating gate. The conductivity of the MoS_2 channel was modulated by the voltage V_{CG} applied on the top Cr/Au control gate electrode (CG). When a positive V_{CG} is applied to the device, electrons will tunnel from the MoS_2 channel through the HfO_2 and accumulate on the MLG floating gate. The application of a negative V_{CG} will deplete the floating gate and reset the device, as shown in Figure 22b. The MLG has a work function of 4.6 eV, which is not sensitive to the number of layers and results in a deep potential well for charge trapping, thus improving the charge retention. Monolayer MoS_2 was highly sensitive to the presence of charges in the floating gate MLG, resulting in a 10^4 difference between memory program and erase states in Figure 22c.

In addition, a new type of the memory device was fabricated with graphene (G) as the FET channel, hBN (B) as the tunnel barrier, and MoS_2 (M) as the charge trapping layer (denoted as GBM) [253,254]. This result confirmed that the MoS_2 layer could act as an effective charge-trapping layer. These GBM devices also showed different hysteresis characteristics, depending on the thicknesses of MoS_2 and hBN. When a thicker MoS_2 layer and thinner hBN were employed, unipolar conductance and greater hysteresis were observed due to effective electron tunneling and electric-field screening. In addition, the reversed stacking structure (MBG) was also investigated, with a high on/off current ratio and a large memory window [253]. Due to the time-dependent PL, the MoS_2–graphene heterostructure can also function as a rewritable optoelectronic switch or memory, where the persistent state shows almost no relaxation or decay within experimental timescales, indicating near-perfect charge retention [255].

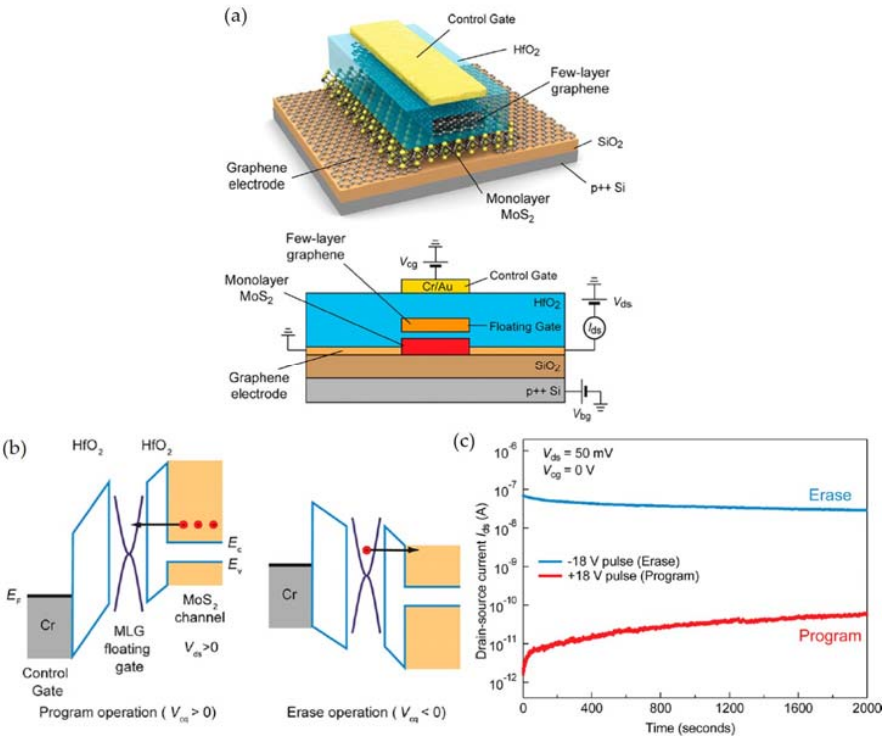

Figure 22. MoS_2/graphene heterostructure memory device layout. (**a**) Three-dimensional schematic view of the memory device based on single-layer MoS_2. Lower is the schematics of a heterostructure memory cell with a single-layer MoS_2 semiconducting channel, graphene contacts and MLG floating gate. The MLG floating gate is separated from the channel by a thin tunneling oxide (1 nm Al_2O_3 + 6 nm HfO_2) and from the control gate by a thicker blocking oxide (1 nm Al_2O_3 + 30 nm HfO_2). (**b**) Simplified band di+agram of the Cr/HfO_2/Gr/HfO_2/MoS_2 heterostructure in program and erase operation. (**c**) Temporal evolution of drain–source currents (I_{ds}) in the erase (ON) and program (OFF) states. The curves are acquired independently for the program (10^{-8}–10^{-7} A) and erase (10^{-12}–10^{-10} A) current states and plotted on a common time scale. The drain–source bias voltage (V_{ds}) is 50 mV, and the duration of the control-gate voltage (V_{cg}) pulse is 3s. Reproduced with permission from [252], American Chemical Society, 2013.

The combination of TMDCs with ferroelectric materials was also used for nonvolatile memory devices as schematically drawn in Figure 23 [101]. FETs based on monolayer or multilayer MoS_2 were fabricated on a lead zirconium titanate ($Pb(Zr,Ti)O_3$, PZT) substrates. The PZT substrate can be used as the alternative to the optoelectronic switching, to write and erase the data as shown in Figure 23. When the MoS_2 layer was illuminated by visible light, the photo-generated carrier would create an internal electric field to affect the polarization of PZT beneath the MoS_2. Only after 5 min illumination, the ON and OFF states became indistinguishable, and data was erased [250].

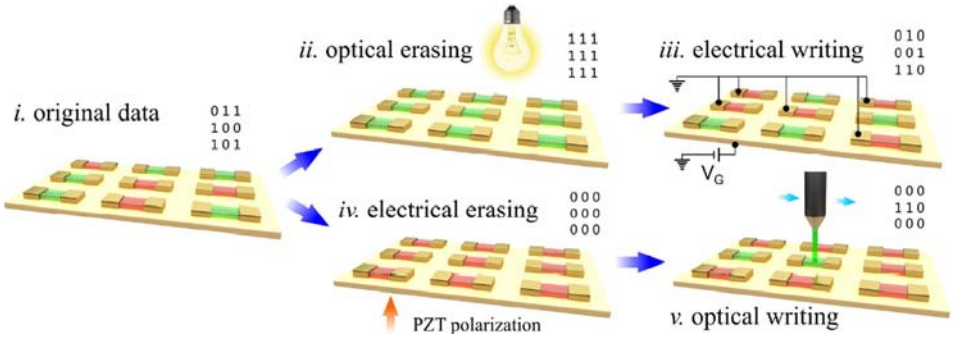

Figure 23. "Optical erase-electrical write" and "electrical erase-optical write" operation of MoS_2-PZT memories. Reproduced with permission from [250], American Chemical Society, 2015.

A type-switching memory device formed with a BP/hBN/MoS_2 heterostructure was developed based on the ambipolar property of BP memory devices [256], and the memory device operated under p-type and n-type modes according to the polarity of a gate voltage pulse, but the P/E ratio was only up to 50 [113], which is not comparable to the Gr/MoS_2-based devices. These MoS_2-based memory devices exhibited high-performance in terms of P/E ratio (10^5), long endurance, and retention (10^5 cycles) and have a low operating voltage (0.05 V). It is expected that TMDCs can be used for non-volatile, portable, and power saving memory devices.

5. Summary

In this review, we have critically evaluated the progress of electronic and optoelectronic devices based on 2D TMDCs. Apparently, the application of TMDCs for field effect transistors (FETs) has been very popular. Most efforts have focused on improving the device mobility by various approaches, including encapsulation with dielectric films, gate configurations, managing the contact barriers, and using "defect-free" substrates such as BN nanosheets. The progress in electronic devices has now involved the development of complex integrated circuits (ICs) and logic gates. Many of these are based on the layout design of the circuit on a same piece of 2D TMDC, fully demonstrating the advantage of "large-area" 2D materials for device integration. On the other hand, many advances have been demonstrated for optoelectronic devices, including solar cells, light-emitting diodes (LEDs), photodetectors, and even lasers. Overall, the efficiency of the TMDC-based optoelectronics is still low. Some of the major issues have been the difficulty in p-type and n-type doping on 2D TMDCs. Other issues are due to the atomically thin nature of the materials, which prevent sufficient light absorption, in spite of their high absorption coefficient (~10^7 m^{-1} in the visible range) [257]. "Stacked heterostructures" appear to be a potential solution, either by stacking multiple 2D TMDCs or other 2D materials (graphene and BN nanosheets), or stacking on other functional "substrates" such as photonic structures, among others. However, most of the 2D heterostructure devices were fabricated by mechanical exfoliation and transference, which is complicated and inefficient for opto-electro applications. The improvement of 2D heterostructure synthesis on a large scale is critical for developing the 2D materials.

It is noted that TMDCs are among the very few semiconducting 2D materials that are stable for device applications. The semiconducting properties in TMDCs are the important features that supplement the gapless graphene and the electrically insulating hBN for 2D devices. The emergence of TMDCs has enabled meaningful applications of vertically stacked heterostructures for novel electronics and optoelectronics devices with tailorable properties. Overall, the progress on 2D TMDC devices is still in its infancy and requires further development. The biggest issue of the TMDCs is the relatively low performance of their electronic and optoelectronic devices, as compared to those constructed by other state-of-the-art semiconductors. The major advantages of TMDC-based devices are the use of very few materials (atomically thin) and the capability of being fabricated as flexible and wearable devices. TMDCs enable energy/materials saving fabrication of highly portable devices, which meet the desired features of nanotechnology.

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