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FPGA Implementation of a Three-Level Boost Converter-fed Seven-Level DC-Link Cascade H-Bridge inverter for Photovoltaic Applications

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Abstract: This paper presents an optimized single-phase three-level boost DC-link cascade H-bridge multilevel inverter (TLBDCLCHB MLI) system to generate a seven-level stepped output voltage waveform for photovoltaic (PV) applications. The proposed TLBDCLCHB MLI system is obtained by integrating a three-level boost converter (TLBC) with a seven-level DC-link cascade H-bridge (DCLCHB) inverter. It consists of a TLBC, level generation unit (LGU) and phase sequence generation unit (PSGU). When compared with traditional boost converter-fed multilevel inverter systems, the proposed TLBDCLCHB MLI system requires a single DC source, fewer power switches and gate drivers. Reduction in the switch count and number of DC sources makes the system cost effective and requires a smaller installation area. Pulse generation for the power switches of an LGU in a DCLCHB inverter is accomplished by providing proper conducting angles that are generated by optimized conducting angle determination (CAD) techniques. In this paper two CAD techniques i.e., equal-phase CAD (EPCAD) and step pulse wave CAD (SPWCAD) techniques are proposed to evaluate the performance of the proposed system in terms of the total harmonic distortion (THD) and the quality of the stepped output voltage waveform. The proposed system has been modeled and simulated using MATLAB/SIMULINK software. Results are presented and discussed. Also, a prototype model of a single-phase TLBDCLCHB MLI system is developed using a field-programmable gate array (FPGA)-based pulse generation with a resistive load and its performance is analyzed for various operating conditions.

Keywords: three-level boost converter (TLBC); DC-link cascade H-bridge (DCLCHB) inverter; conducting angle determination (CAD) techniques; total harmonic distortion (THD)

1. Introduction

Development in power electronics lay down a widespread scope for the resourceful operation of power converters. A few setups of power converters are produced to do the sun-powered photovoltaic (PV) applications with enhanced adequacy [1,2]. PV power generation is an encouraging elective source of energy and has numerous focal points compared to the other elective energy sources like wind, ocean, biomass, fuel, geothermal, and so on. In PV power generation, boost converters and multilevel inverters (MLIs) are playing a major role in power conversion. These power converters are broadly being utilized as a connection between load and supply. As most of the renewable power source generation is DC in nature, the DC-DC boost converters are utilized to increase the voltage level, and the DC must be changed over to AC for grid connection. Therefore, MLIs are

used for DC to AC conversion [3,4]. The power generation using a traditional boost converter and inverter consists of a greater number of components, requires a larger installation area, is bulky in size, and costly. Also, the traditional boost converters are unable to produce a high boost ratio [5,6]. This paper proposes a three-level boost converter (TLBC) with a high boost ratio, based on one switch, one inductor, (2N-1) capacitors, and (2N-1) diodes for 'N' levels. It is a pulse width modulation (PWM)-controlled boost converter capable of maintaining an equal voltage in all 'N' output levels and controlling the input current.

In this paper, the structure of single-phase three-level boost DC-link cascade H-bridge multilevel inverter (TLBDCLCHB MLI) system is proposed to generate a seven-level stepped output voltage waveform for PV applications. The proposed system is obtained by integrating a three-level boost converter (TLBC) with a seven-level DC-link cascade H-bridge (DCLCHB) [7,8]. Also, the objective of the proposed work is to investigate the performance of a single-phase seven-level DCLCHB inverter [9,10] using conducting angle determination (CAD) techniques [11] in terms of the total harmonic distortion (THD) and the quality of the stepped output voltage waveform. Here, equal-phase CAD (EPCAD) based on equal-area distribution and step pulse wave CAD (SPWCAD) based on volt-second area equal to step pulse wave techniques are proposed to evaluate the performance of the DCLCHB inverter [12]. The proposed TLBDCLCHB MLI system is modeled, simulated and validated through experimental setup using field-programmable gate array (FPGA)-based pulse generation.

2. Structure of TLBDCLCHB MLI System

The block diagram of the proposed TLBDCLCHB MLI system is shown in Figure 1. The proposed TLBDCLCHB MLI system consists of single DC voltage source, TLBC, and DCLCHB inverter to generate a seven-level stepped output waveform. The DCLCHB inverter is composed of level generation unit (LGU) and phase sequence generation unit (PSGU). LGU is used to generate the required number of levels and PSGU is used to generate positive and negative sequence voltage levels [13]. The equivalent structure of TLBDCLCHB MLI system is shown in Figure 2.

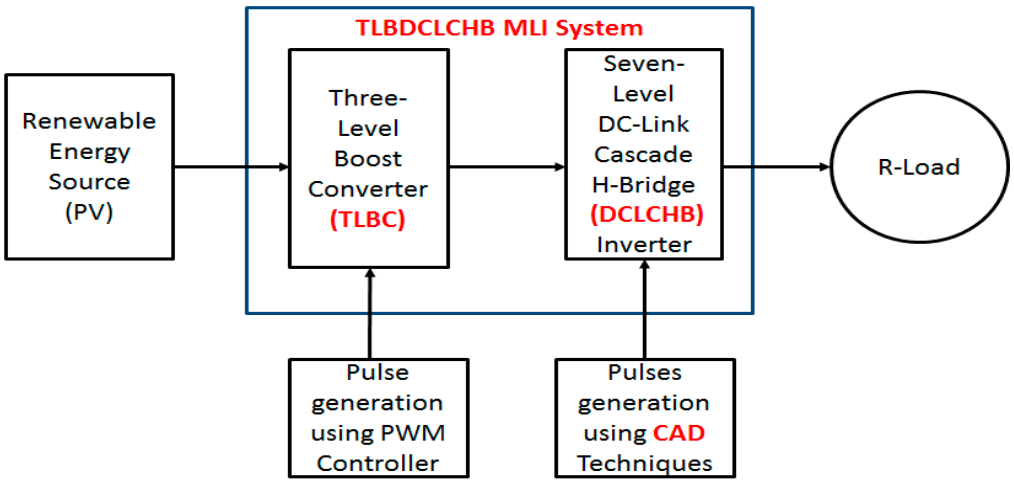

Figure 1. Block diagram of the proposed (TLBDCLCHB MLI) system.

The number of power switches '$N_{Switches}$' and the number of levels 'm' for a single-phase TLBDCLCHB MLI system are calculated using Equations (1) and (2), respectively.

$$m = (2C+1)^H \quad (1)$$

$$N_{Switches} = (m-1)+5 \quad (2)$$

where 'C' is the number of DC link capacitors integrated to a DCLCHB inverter and 'H' is the number of H-Bridge circuits.

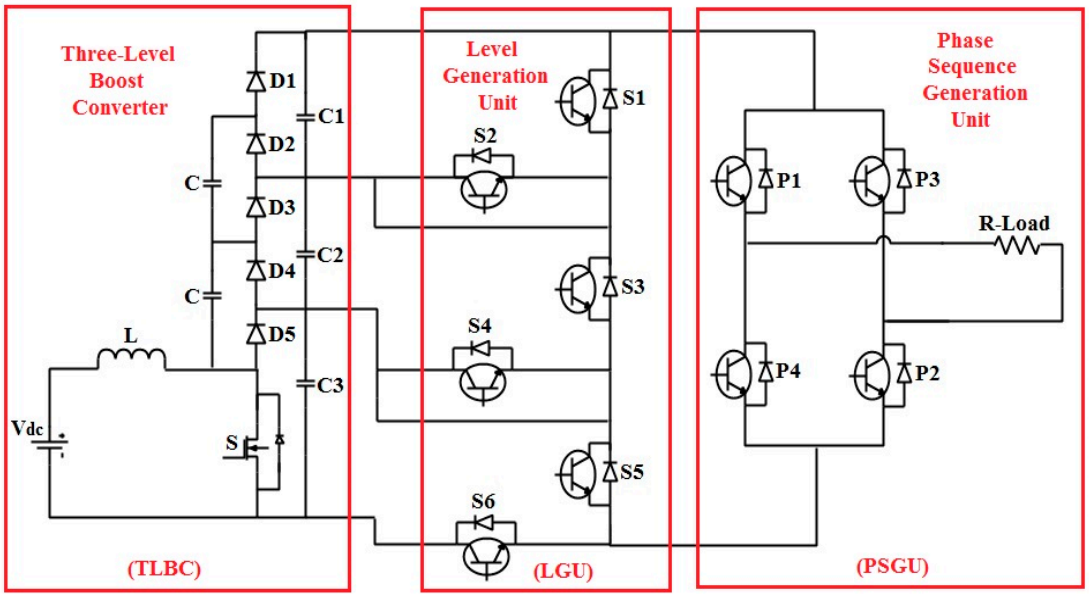

Figure 2. Equivalent structure of TLBDCLCHB MLI system.

Table 1 demonstrates the required number of power switches and DC sources for the traditional and proposed boost DC-link-based inverter to generate a stepped output waveform from seven levels to fifteen levels. From the investigation, it is gathered that the proposed TLBDCLCHB MLI system has reduced the switch count and requires just a single DC source compared to traditional boost multilevel inverter (MLI) systems [14,15].

Table 1. Component requirements for existing and proposed boost based MLI systems.

Number of Levels	Boost Cascade MLI (Conventional)		TLBDCLCHB MLI (Proposed)	
	Number of Power Switches	Number of DC Sources	Number of Power Switches	Number of DC Sources
7	15	3	11	1
9	20	4	13	1
11	25	5	15	1
13	30	6	17	1
15	35	7	19	1

3. Three-Level Boost Converter (TLBC)

The circuit configuration of DC-DC TLBC is represented in Figure 2. It consists of a traditional boost converter, (2N-1) capacitors, and (2N-1) diodes. The main advantages of using the TLBC topology are; it can be extended to any number of levels by adding only diodes and capacitors without changing the main circuit; no need of additional voltage balance circuit; and voltage gain can be increased without the use of a transformer by operating at minimum duty ratio. The TLBC circuit consists of three stages which are operated by varying duty cycles of 0.4, 0.5, and 0.6. The operation of the TLBC is explained in [16].

3.1. Analysis of DC-DC TLBC

Considering the presence and absence of inductor power loss for both traditional and proposed TLBCs gives important information to designers. From basic principles, the voltage gain or the boost factor of the traditional boost converter [14] is given by Equation (3):

$$\text{Voltage gain, } \frac{V_o}{V_{dc}} = \frac{1}{1-D} \tag{3}$$

where 'V_o' is the output voltage, 'V_{dc}' is the input voltage and 'D' is the duty cycle.

By considering the lossless system, the voltage gain for the N-level boost converter can be expressed as:

$$\frac{V_o}{V_{dc}} = \frac{N}{1-D} \tag{4}$$

For a lossless system, the input current, I_{dc}, can be expressed as:

$$I_{dc} = \frac{N\, I_o}{1-D} \tag{5}$$

From Equation (5), the input current, I_{dc}, can be controlled using duty cycle 'D' in the PWM. Now the voltage gain or boost factor expression for the N-level boost converter can be derived as follows:

Based on the condition that the average voltage across the inductor 'L' is equal to zero. The total inductor voltage during the ON—OFF condition can be expressed as,

$$V_L = D(V_{dc} - I_L R_L) + (1-D)(V_{dc} - V_C - I_L R_L) = 0 \tag{6}$$

where, 'I_L' is the inductor current which is equivalent to 'I_{dc}' and 'R_L' is the inductor resistance or parasitic resistance.

Here, the first term of Equation (6) is valid when the switch 'S' is turned ON, and the second term can write when the switch 'S' is turned OFF. From Equation (6) it can be written as,

$$V_{dc}(D + 1 - D) + I_L R_L(-D - 1 + D) = (1-D)V_C \tag{7}$$

From Equation (7),

$$V_{dc} = (1-D)V_C + I_L R_L \tag{8}$$

Therefore, from Equations (3)–(7), the input voltage, V_{dc} can be expressed as,

$$V_{dc} = (1-D)\frac{V_o}{N} + \frac{N\, V_o}{(1-D)R_O} R_L \tag{9}$$

Therefore, Equation (9) can be expressed as follows:

$$\frac{V_{dc}}{V_O} = \frac{1}{\frac{(1-D)}{N} + \frac{NR_L}{(1-D)R_O}} \tag{10}$$

Equation (10) is equal to Equation (3) if N = 1 and R_L = 0. From Equation (10), it can be observed that the voltage gain reaches a maximum before D = 1, and then becomes 0. The effect of parasitic resistance 'R_L' is responsible for the limitation in the boost factor. The actual boost factor or voltage gain against the duty cycle is analyzed by varying 'R_L' in Equation (10). Figures 3 and 4 describe the graph between voltage gain versus duty cycle for the traditional boost converter, i.e., N = 1 and for the proposed TLBC, i.e., N = 3 using different values of R_L/Ro.

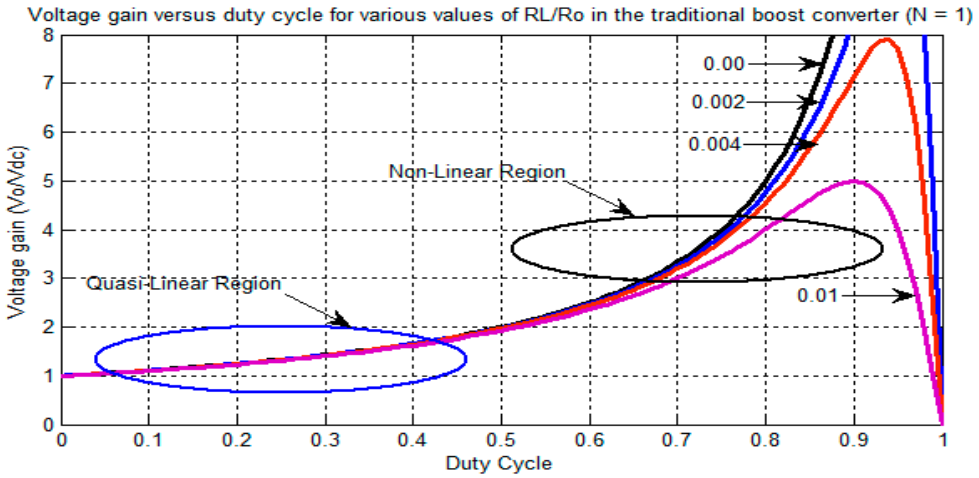

Figure 3. Duty cycle versus voltage gain of a traditional boost converter for various values of R_L/Ro ($N = 1$).

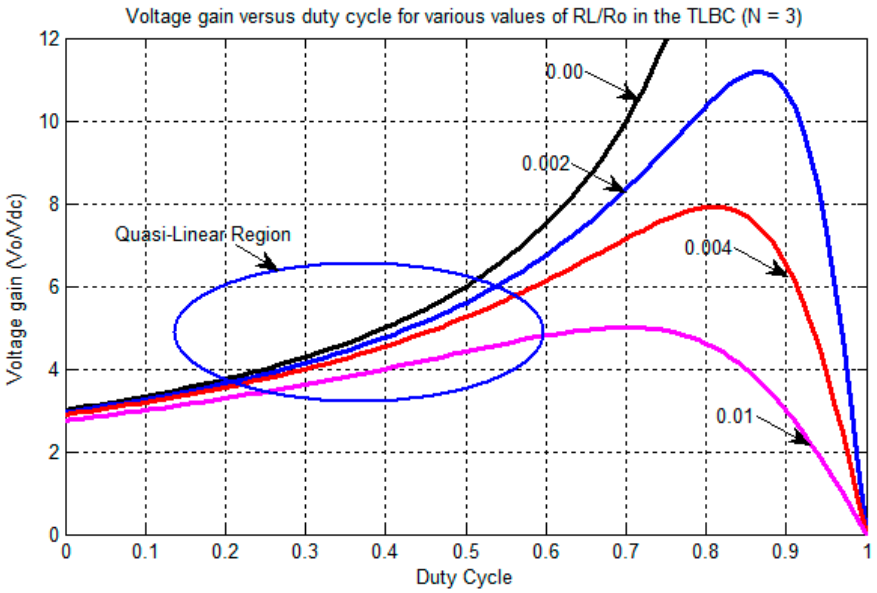

Figure 4. Duty cycle versus voltage gain of TLBC for various values of R_L/Ro ($N = 3$).

From the Figures 3 and 4, it can be noticed that the voltage gain of the traditional boost converter is quasi-linear when the duty cycle varies from 0 to 0.5, but beyond that, the boost factor of a traditional boost converter becomes non-linear; therefore, the control of a traditional boost converter is complicated.

Similarly, from Figure 4, i.e., when $N = 3$, it can be observed that the quasi-linear region is extended with a high voltage gain for the TLBC. Therefore, the TLBC achieves a high voltage gain compared to the traditional boost converter, and, also a better operating point of the duty cycle for the TLBC, which is from 0.4 to 0.6.

In the next section, the effect of the voltage drop across the switch and diodes is studied.

3.2. TLBC Voltage Drop Across Switch and Diodes

In actual operation of TLBC, the voltage drop across the switch and diodes must be considered since it avoids full charge across the capacitors [17,18]. Therefore, it reduces the conversion efficiency of the TLBC topology. In general, the voltage drop in the power switches and diodes can be around 2 V, and it can be neglected in medium- and high-voltage applications but must be considered in

low-voltage applications. Here, the voltage drop across the switch and diodes is assumed to be equal to 'V_d'.

From Figure 5, it can be noticed that the voltage across the C_5 becomes,

$$V_{C5} = V_{C3} - V_{switch} - V_{diode} = V_{C3} - 2V_d \tag{11}$$

where, '$2V_d$' is the voltage drop across the switch 'S' and diode 'D_5'.

Similarly, V_{C2} and V_{C1} can be written as,

$$V_{C2} = 2V_{C3} - 4V_d \tag{12}$$

$$V_{C1} = 3V_{C3} - 8V_d \tag{13}$$

where, V_{C2} and V_{C1} are the expressions for the voltage output of two-level and three-level boost converters, respectively. The generalized output voltage expression for the N-level boost converter can be expressed as follows:

$$V_o = NV_C - (N-1)4V_d \tag{14}$$

where, 'V_C' is the lower capacitor output voltage, and follows Equation (3).

Equation (14) gives the output voltage for the multiple stages of the boost converter. The efficiency of the proposed converter for the N-level is given by the Equation (15).

$$Efficiency,\ \eta = \frac{V_o}{NV_C} = 1 - \frac{(N-1)4V_d}{NV_C} \tag{15}$$

Form Equation (15), the efficiency of the TLBC circuit can be reduced by considering the voltage drop across the switch and diode.

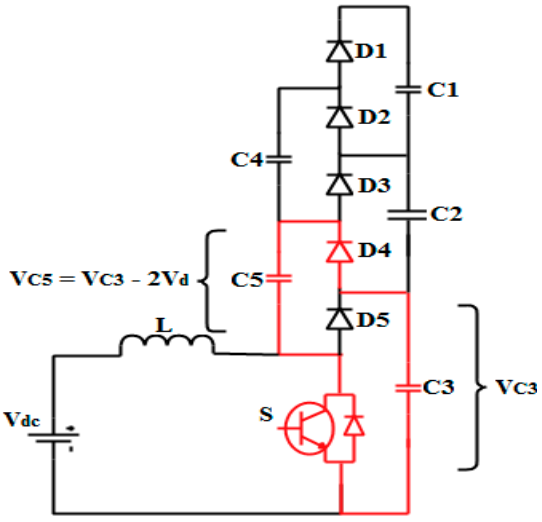

Figure 5. Charging C5 of a TLBC with switch and diode's voltage drop.

3.3. Closed-Loop Control of TLBC

From Figure 5 and Equation (10), it can be observed that the output voltage gain depends on the ratio of load resistance (R_O) and source resistance (R_L), i.e., if there is any variation between the load and source resistances, the output voltage of TLBC is not kept constant, and, from Equation (13), there will be a variation in the duty cycle to get the required amount of output voltage by considering the voltage drop across the switch and diodes. Therefore, the proposed TLBC circuit is modeled in closed-loop mode using an integral controller to maintain the constant output voltage.

Figure 6 represents the TLBC circuit in closed-loop mode. In the case of any variation in the load side or source side, the output changes, so a suitable controller is designed to change the duty cycle by comparing 'V_{ref}' with 'V_{out}' in order to maintain the required output voltage.

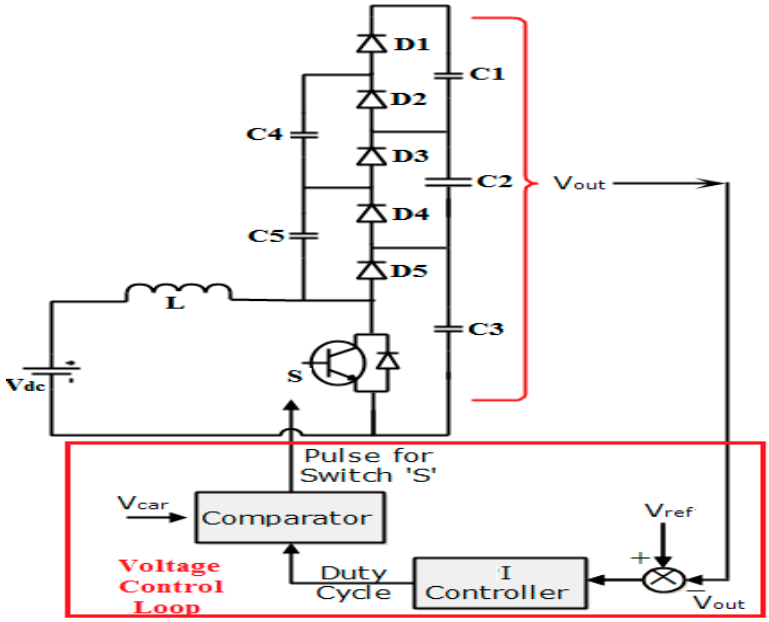

Figure 6. Model of TLBC in closed-loop mode.

4. DC-Link Cascade H-Bridge (DCLCHB) Inverter

Figure 7 depicts the DCLCHB inverter topology for the generation of a single-phase seven-level output voltage waveform. It is composed of LGU and PSGU [12].

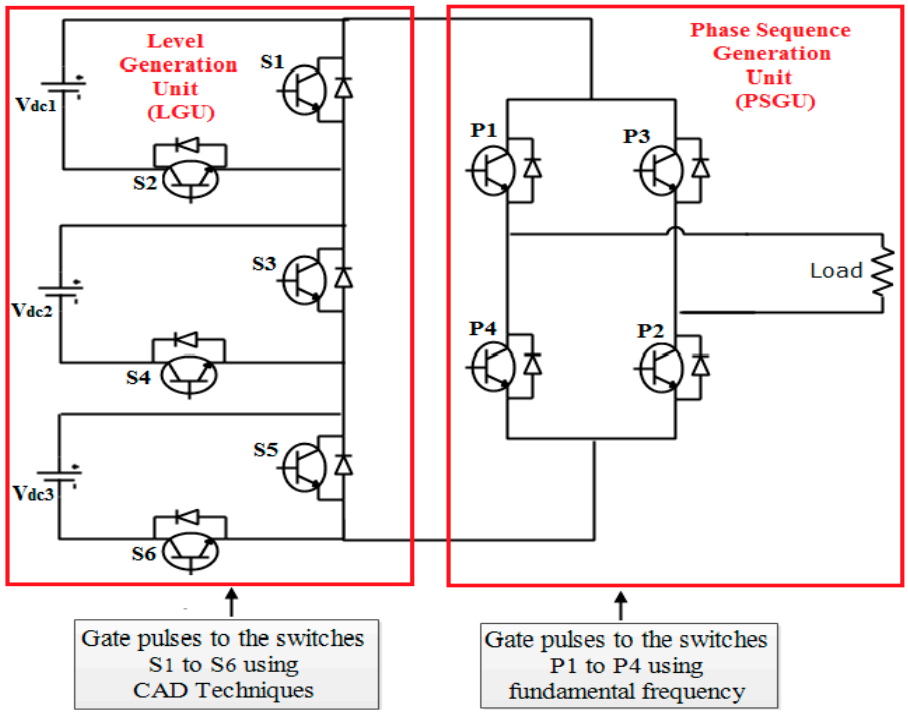

Figure 7. Single-phase seven-level DCLCHB inverter.

Switches in the LGU are used to generate the required number of levels and it is formed by connecting half-bridge cells in series. Each half-bridge cell consists of a DC source controlled by two switches. PSGU consists of an H-bridge circuit, which is used to generate the positive and negative sequence voltage levels. Table 2 gives a component requirement to generate a seven-level output voltage for the proposed and existing MLIs. It clearly shows a substantial component reduction when using a DCLCHB structure [7,8].

Table 2. Component requirements for existing and proposed cascade MLI systems.

Components	Traditional MLI	Proposed MLI
Switches	12	10
Clamping diodes	0	0
DC sources	3	3
Capacitors	0	0

In this DCLCHB inverter topology, all the magnitudes of DC voltage sources are equal ($V_{dc1} = V_{dc2} = V_{dc3}$).

$$\text{i.e., } V_{dci} = V_{dc}, \text{ where } i = 1, 2, \text{ and } 3 \tag{16}$$

The maximum value of the output phase voltage is obtained by using Equation (17).

$$V_{max} = \sum_{i=1}^{S} V_{dci} \tag{17}$$

The number of output phase voltage levels can be obtained from Equation (1). The number of power switches for the DCLCHB inverter can be calculated using Equation (18).

$$N_{Switches} = (m-1) + 4 \tag{18}$$

Equation (16) gives the output level of the LGU. By using PSGU, the positive and negative levels are obtained at the load (V_o), the synthesized stepped AC output phase voltage will be obtained by using the Equations (19) and (20).

$$V_o,\ max = \sum_{i=1}^{3} + V_{dci},\ \text{If } P_1,\ P_2 = 1 \tag{19}$$

$$V_o,\ max = \sum_{i=1}^{3} - V_{dci},\ \text{If } P_3,\ P_4 = 1 \tag{20}$$

For a single-phase seven-level DCLCHB inverter, the switching sequences to generate the required levels are given in Table 3.

Table 3. Switching sequence to generate seven-level output for a DCLCHB inverter.

S.No	LGU Switches						PSGU Switches				Voltage Levels (Volts)
	S_1	S_3	S_5	S_2	S_4	S_6	P_1	P_2	P_3	P_4	
1	1	1	1	0	0	0	0	0	0	0	0
2	0	1	1	1	0	0	1	1	0	0	100
3	0	0	1	1	1	0	1	1	0	0	200
4	0	0	0	1	1	1	1	1	0	0	300
5	0	1	1	1	0	0	0	0	1	1	−100
6	0	0	1	1	1	0	0	0	1	1	−200
7	0	0	0	1	1	1	0	0	1	1	−300

5. Conducting Angle Determination (CAD) Techniques

CAD techniques are a vital part of any inverter since they are directly related to the efficiency of the entire system [6,12]. It is used to control the proposed DCLCHB inverter output phase voltage and also for the calculation of the two main parameters such as %THD and V_{rms}. In this paper, a step pulse wave CAD (SPWCAD) technique has been employed to trigger the switches of LGU in the DCLCHB inverter and is compared with a conventional CAD technique, i.e., equal-phase CAD (EPCAD) technique. The generation of the seven-level stepped voltage waveform using CAD techniques is shown in Figure 8.

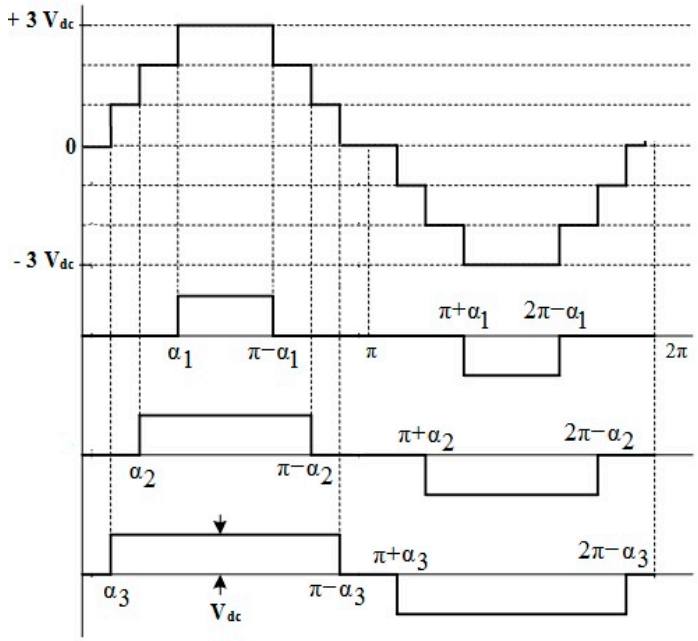

Figure 8. Generation of the seven-level stepped voltage waveform for DCLCHB inverter using CAD techniques.

In the presented EPCAD and SPWCAD techniques, for an m-level stepped waveform in the period of the first quadrant, i.e., 0 to 90°, $2(m-1)/2$ conducting angles need to be determined. From Figure 8, to generate a seven-level stepped waveform in the first quadrant, i.e., 0 to 90°, three conducting angles need to be determined. They are defined as the main conducting angles, i.e., α_1, α_2 and α_3 using the time-sequence. From Figure 8, it can be noticed that only the main conducting angles need to be determined; the rest of the conducting angles can be derived from the main conducting angles. The solution of the main conducting angles, i.e., α_1, α_2 and α_3 must satisfy the following condition:

$$0 \leq \alpha_1 \leq \alpha_2 \leq \alpha_3 \leq \frac{\pi}{2} \tag{21}$$

5.1. EPCAD Technique

In the EPCAD technique the main conducting angles are derived by taking an average distribution of the conducting angles from 0 to180°. In this technique, the main conducting angles are obtained by using Equation (22).

$$\alpha_i = i\left(\frac{180^\circ}{m}\right) \tag{22}$$

where $i = 1, 2, \ldots\ldots \left(\frac{m-1}{2}\right)$, $m =$ number of levels.

For a seven-level stepped waveform using the EPCAD technique, three main conducting angles need to be determined using Equation (22), i.e., α_1, α_2 and α_3, the values of which are 25.71°, 51.43°, and 77.14°, respectively.

5.2. SPWCAD Technique

In the proposed SPWCAD technique, conducting angles are acquired by computing the volt-second areas of the sine reference voltage waveform that is equivalent to the stepped output phase voltage waveform of the DCLCHB inverter. In the seven-level DCLCHB inverter, since three half-bridge cells are connected in series, the reference voltage 'V_{ref}' and output-phase voltage '$V_{out\text{-}phase}$' can be obtained by the Equations (23) and (24) respectively:

$$V_{ref} = 3\left(\frac{4V_{dc}}{\pi}\right)(M_i \operatorname{Sin} \omega t) \tag{23}$$

$$V_{out-phase} = i.V_{dc}\ (1 \le i \le 3) \tag{24}$$

where, 'M_i' is the modulation index, and 'i' is the integer number.

Figure 9 demonstrates the dummy conducting angles ($\alpha_i{}^1$) in the case of $M_i = \pi/4$. The areas of $A_1{}^1$, $A_2{}^1$, and $A_3{}^1$ are encompassed by the sine reference voltage wave and the stepped output-phase voltage levels in the positive half-cycle of the seven-level DCLCHB inverter.

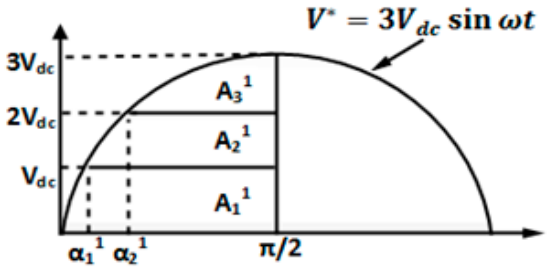

Figure 9. Reference voltage waveform with dummy conducting angles.

The generation of a step pulse wave in the DCLCHB inverter to meet the equivalent areas as $A_1{}^1$, $A_2{}^1$, and $A_3{}^1$. Here, main conducting angles (α_i) are defined as the switching timing angles of step pulse waves in the DCLCHB inverter. Figure 10 represents the main conducting angles and the stepped output phase voltage of the seven-level DCLCHB inverter during the positive half cycle.

Assuming that the areas A_1, A_2, and A_3 made by the main conducting angles in Figure 10 are equivalent to $A_1{}^1$, $A_2{}^1$, and $A_3{}^1$ made by dummy conducting angles which are obtained as follows:

Area, $A_1{}^1$ can be obtained from Equation (25):

$$A_1{}^1 = (A_1{}^1 + A_2{}^1 + A_3{}^1) - (A_2{}^1 + A_3{}^1) \tag{25}$$

Therefore, from Equation (25), $A_1{}^1$ can be written as:

$$A_1{}^1 = \int_0^{\frac{\pi}{2}} 3\ V_{dc} \sin \omega t d(\omega t) - \left\{ \int_{\alpha_1^1}^{\frac{\pi}{2}} 3V_{dc} \sin \omega t d(\omega t) - \left(\frac{\pi}{2} - \alpha_1^1\right) V_{dc} \right\} \tag{26}$$

From Figure 10, Area, A_1 can be expressed as,

$$A_1 = \left(\frac{\pi}{2} - \alpha_1\right) V_{dc} \tag{27}$$

Since ${A_1}^1$ is equal to A_1, the real conducting angle α_1 of the proposed SPWCAD technique is obtained as,

$$\alpha_1 = \frac{\pi}{2} - \left\{ \int_0^{\frac{\pi}{2}} 3\, V_{dc} \sin \omega t d(\omega t) - \left(\int_{\alpha_1^1}^{\frac{\pi}{2}} 3\, V_{dc} \sin \omega t d(\omega t) - \left(\tfrac{\pi}{2} - \alpha_1^1\right) \right) \right\} \tag{28}$$

Similarly, by equating ${A_2}^1$ to A_2, the angle α_2 can be expressed as,

$$\alpha_2 = \frac{\pi}{2} - \left\{ \int_0^{\frac{\pi}{2}} 3\, V_{dc} \sin \omega t d(\omega t) - \left(\int_{\alpha_2^1}^{\frac{\pi}{2}} 3\, V_{dc} \sin \omega t d(\omega t) - \left(\tfrac{\pi}{2} - \alpha_2^1\right) \right) \right\} \tag{29}$$

α_3 can be obtained by equating ${A_3}^1$ to A_3 or by using Equation (30):

$$\int_0^{\frac{\pi}{2}} 3\, V_{dc} \sin \omega t d(\omega t) - \left(A_1^1 + A_2^1\right) = \left(\frac{\pi}{2} - \alpha_3\right) V_{dc} \tag{30}$$

For a seven-level DCLCHB inverter, the conducting angles are calculated by using Equations (31)–(33).

$$\alpha_1 = \frac{12M_i}{\pi} \left\{ \cos\left(\sin^{-1}\left(\frac{\pi}{12M_i} \right) \right) - 1 \right\} + \sin^{-1}\left(\frac{\pi}{12M_i} \right) \tag{31}$$

$$\alpha_2 = \frac{12M_i}{\pi} \left\{ \cos\left(\sin^{-1}\left(\frac{2\pi}{12M_i} \right) \right) - \cos\left(\sin^{-1}\left(\frac{\pi}{12M_i} \right) \right) \right\} + 2\sin^{-1}\left(\frac{2\pi}{12M_i} \right) - \sin^{-1}\left(\frac{\pi}{12M_i} \right) \tag{32}$$

$$\alpha_3 = \frac{3\pi}{2} - \frac{12M_i}{\pi} \cos\left(\sin^{-1}\left(\frac{2\pi}{12M_i} \right) \right) - 2\sin^{-1}\left(\frac{2\pi}{12M_i} \right) \tag{33}$$

Therefore, for a seven-level stepped waveform using the SPWCAD technique, three main conducting angles need to determined using Equations (31)–(33), i.e., α_1, α_2 and α_3 and their values are 9.43°, 29.59°, and 55.88°, respectively, for the M_i = 0.8.

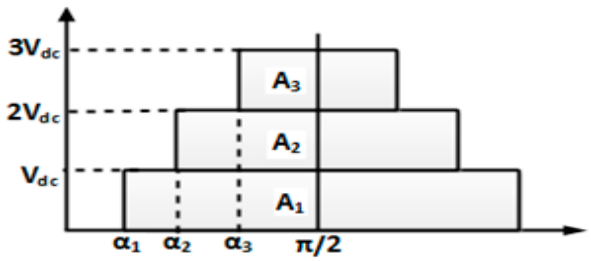

Figure 10. Output phase-voltage of a seven-level DCLCHB inverter in the positive half-cycle voltage.

5.3. Comparison of the SPWCAD and EPCAD Technique

The conducting angles acquired by the SPWCAD technique are different from those acquired by the EPCAD technique. In the SPWCAD technique, conducting angles are acquired based on the modulation index (M_i) whereas the EPCAD technique gives the same conducting angles irrespective of the M_i. The proposed SPWCAD technique method can be applied to different modulation indices. The range of M_i and the number of conducting angles are listed in Table 4. Also, the values of conducting angles for the proposed SPWCAD technique using various modulation indices are listed in Table 5 for the DCLCHB inverter.

Table 4. Number of conducting angles and steps in output waveform SPWCAD technique for various M_i.

Range of M_i	Number of Conducting Angles	Number of Steps in Output Waveform
$0 < M_i < 0.33$	1	3
$0.33 \leq M_i < 0.66$	2	5
$0.66 \leq M_i < 1$	3	7

Table 5. Conducting angles of SPWCAD technique for various M_i.

Conducting Angles (Degrees)	Modulation Indices (M_i)		
	0.3	**0.6**	**0.8**
α_1	27.17	12.7	9.439
α_2	–	41.65	29.59
α_3	–	–	55.88

5.4. THD Calculation of the Seven-Level Stepped Output Phase Voltage using CAD Techniques

The general THD expression for a periodic output phase voltage for a proposed DCLCHB inverter can be expressed as,

$$THD = \sqrt{\left(\frac{V_{rms}}{V_1}\right)^2 - 1} \tag{34}$$

where V_1 is the RMS (root mean square) value of the fundamental component and V_{rms} is the RMS value of the output phase voltage. For the proposed seven-level RV MLI, V_{rms} and V_1 can be obtained by using Equations (35) and (36).

$$V_{rms} = V_{dc}\sqrt{\left[\frac{2}{\pi}.\Big(\ (\alpha_2 - \alpha_1) + 4\ (\alpha_3 - \alpha_2) + 9\ (\alpha_3 - \alpha_2)\ \Big)\right]} \tag{35}$$

$$V_1 = \frac{4V_{dc}}{\pi\sqrt{2}}[(\text{Cos}\ \alpha_1 + \text{Cos}\ \alpha_2 + \text{Cos}\ \alpha_3)] \tag{36}$$

The output phase voltage THD expression for the proposed seven-level DCLCHB inverter can be obtained by substituting Equations (35) and (36) into Equation (34) and is given by:

$$V_1 = \frac{4V_{dc}}{\pi\sqrt{2}}[(\text{Cos}\ \alpha_1 + \text{Cos}\ \alpha_2 + \text{Cos}\ \alpha_3)] \tag{37}$$

Theoretical values of the output phase voltage THD for the seven-level DCLCHB inverter using EPCAD and the proposed SPWCAD techniques with the corresponding main conducting angles are given in Table 6.

Table 6. Conducting angles, theoretical output phase voltage THD, and V_{rms} values for a seven-level DCLCHB inverter (m = 7).

CAD Technique	Conducting Angles (in Degrees)			% THD (Theoretical)	V_{rms} (V)
	α_1	α_2	α_3		
EPCAD	25.71	51.43	77.14	31.05	165.8
SPWCAD	9.43	29.59	55.88	11.95	219.1

6. Simulation and Experimental Validation of the Proposed TLBDCLCHB Inverter System

The simulation of the proposed single-phase seven-level TLBDCLCHB inverter system is analyzed using MATLAB Simulink and validated experimentally through FPGA-based pulse generation.

6.1. TLBC Simulation Results in Open-Loop Mode

The simulation of the TLBC is carried out and analyzed in open-loop mode by considering the DC input voltage V_{dc} of 50 V, which should be boosted to a total DC-link voltage of 250 V, 300 V, and 375 V for the duty cycles of 0.4, 0.5, and 0.6, respectively, and the voltage across each of the capacitors at the output should be boosted to 83.33 V, 100 V, and 125 V for the duty cycles of 0.4, 0.5, and 0.6, respectively, as shown in Figures 11–13.

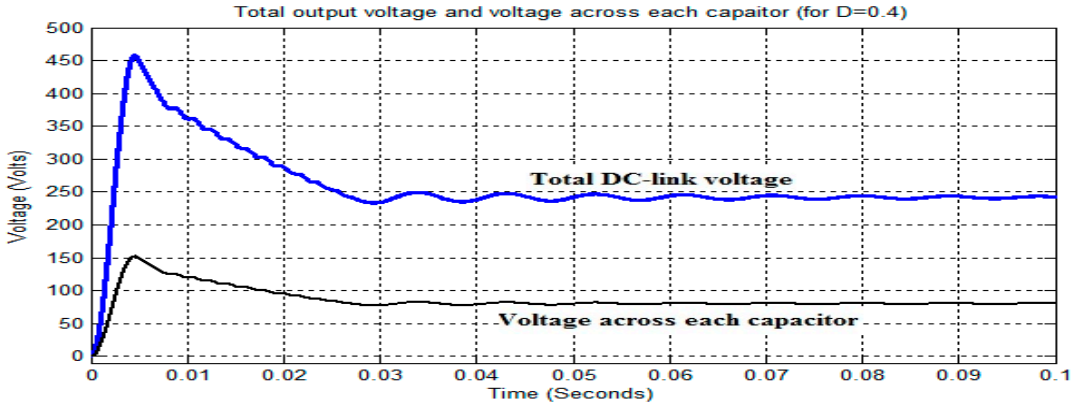

Figure 11. Output of TLBC in open-loop for D = 0.4.

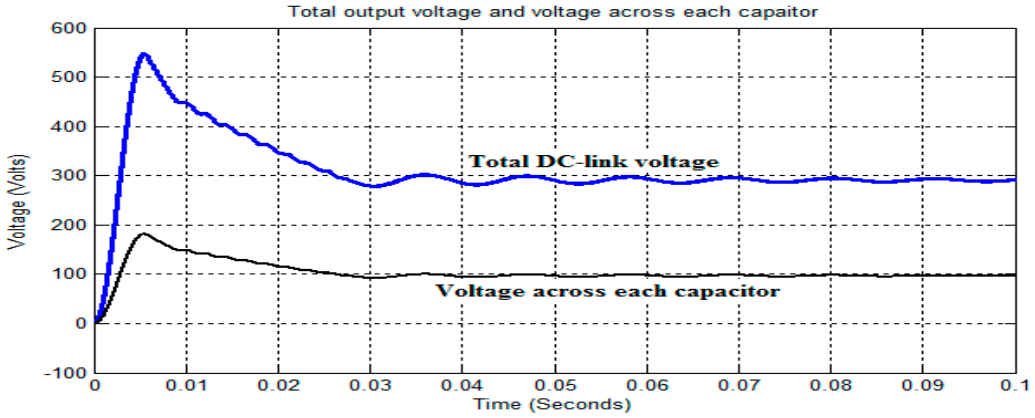

Figure 12. Output of TLBC in open-loop for D = 0.5.

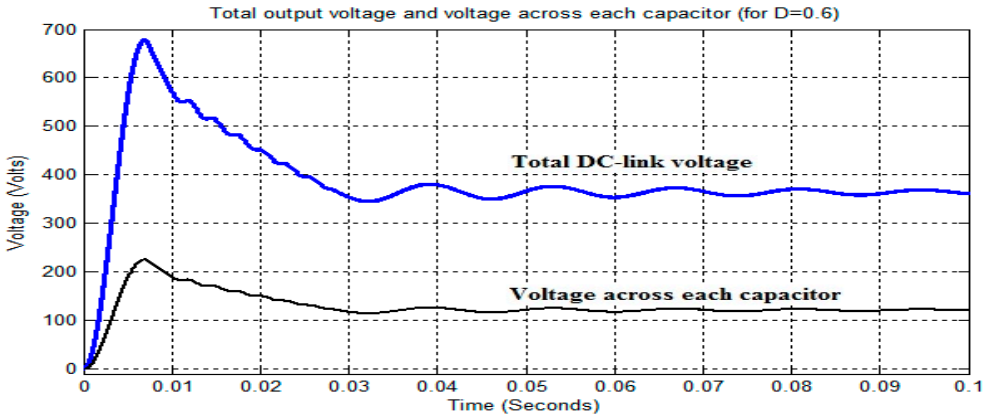

Figure 13. Output of TLBC in open-loop for D = 0.6.

From Figures 11–13, it is observed that the total DC-link output voltage for the duty cycles of 0.4, 0.5, and 0.6 has been boosted to 242.6, 291.4 V, and 361.4 V as opposed to 250 V, 300 V, and 375 V,

respectively, due to the voltage drop across the switch and diodes. Similarly, the voltage drops across each of the capacitors are boosted to 82.17 V, 98.5 V, and 121.8 V as opposed to 83.33 V, 100 V, and 125 V. Also, it is noticed that the ripple in the total DC-link output voltage and voltage across each capacitor are increased by increasing the duty cycle from 0.4 to 0.6 to achieve the maximum DC-link output voltage with minimum ripple. Further, the open-loop mode of TLBC is extended to operate in closed-loop mode to maintain the required amount of DC-link output voltage by compensating the voltage drop across the switch and diodes, and, also, to reduce the ripple.

6.2. TLBC Simulation Results in Closed-Loop Mode

The proposed TLBC is implemented in closed-loop to maintain the constant output voltage using the voltage control loop. Here, the output of TLBC is measured and fed to an integral controller by comparing with the required reference output voltage to vary the duty cycle. Figure 14 shows the total DC-link output voltage and the voltage across each capacitor of the TLBC in closed-loop mode for $D = 0.5$. The corresponding change in duty cycle due to the reference output voltage is shown in Figure 15.

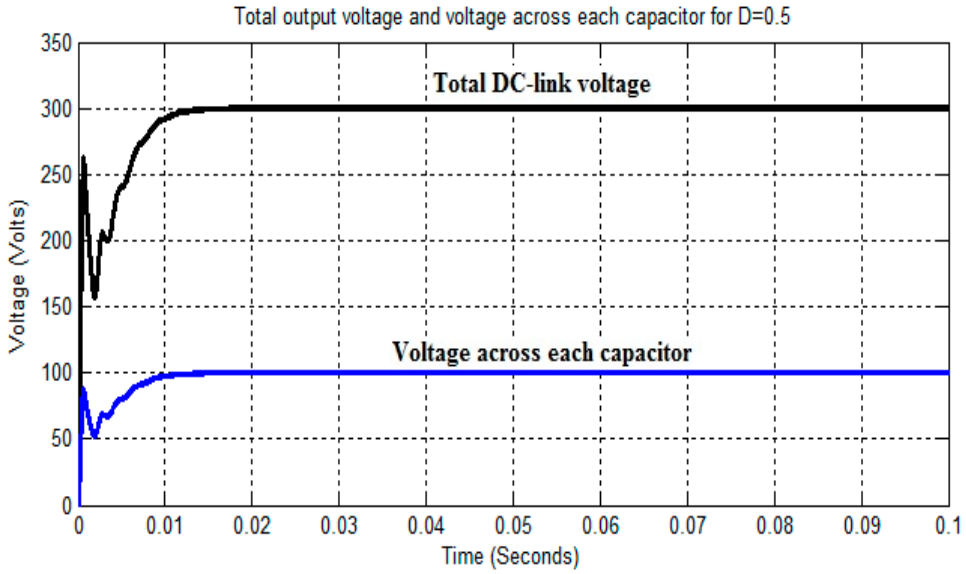

Figure 14. Output of TLBC in closed-loop for $D = 0.5$.

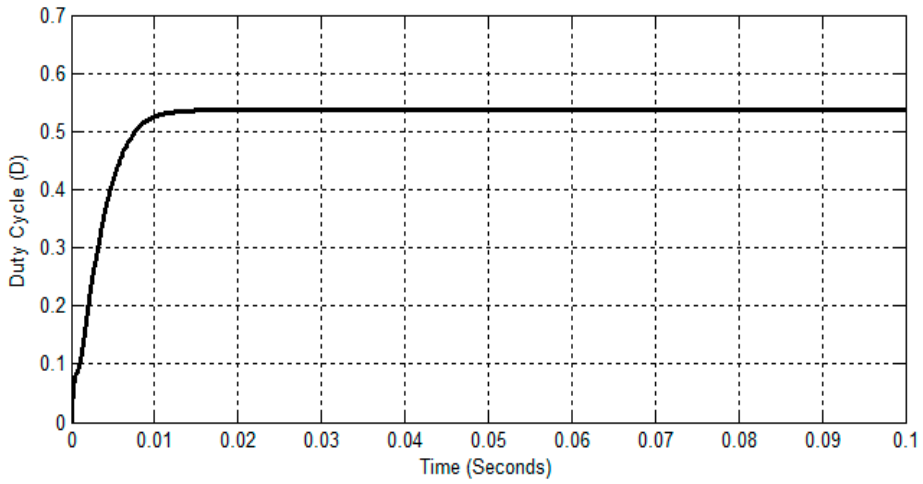

Figure 15. Change in duty cycle of TLBC in closed-loop.

From the Figures 14 and 15, it is observed that the total DC-link output voltage and the voltage across each capacitor of the TLBC is boosted to 300 V and 100 V, respectively, as per the reference output voltage by changing the duty cycle using an integral controller.

6.3. TLBDCLCHB Inverter Output using CAD Techniques

Simulation results of TLBC-fed DCLCHB inverter to generate a seven-level stepped output waveform using EPCAD and SPWCAD techniques and its THD analysis are shown in Figures 16–21 for $D = 0.5$.

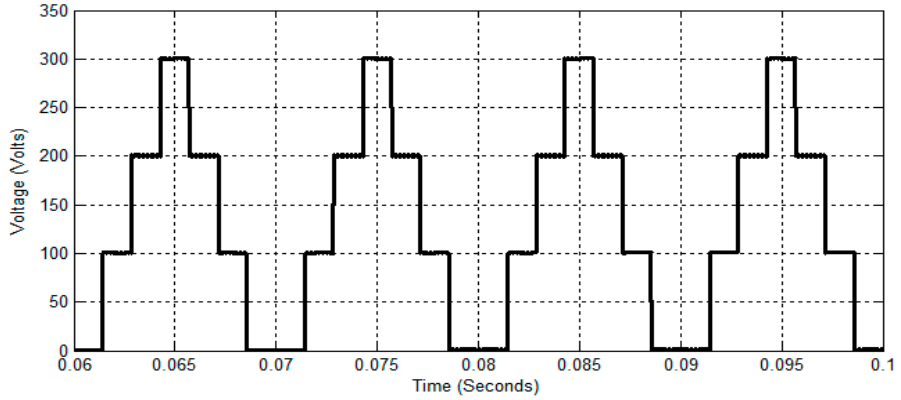

Figure 16. Inverter output across LGU using the EPCAD technique.

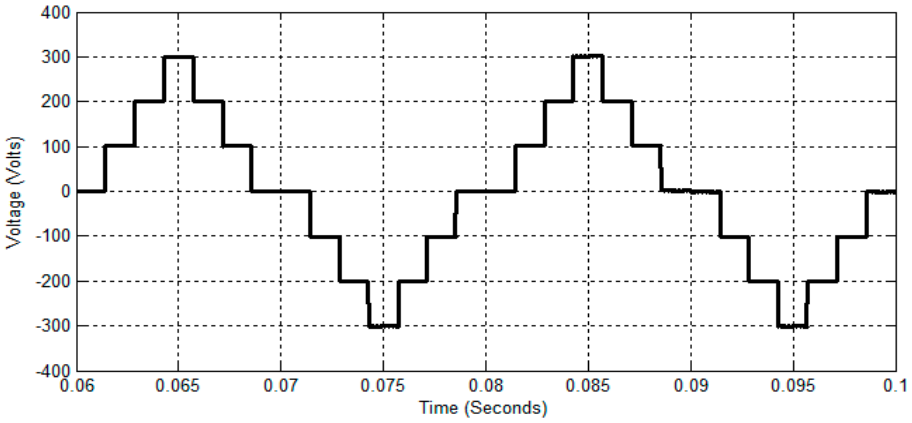

Figure 17. TLBDCLCHB inverter output using EPCAD technique.

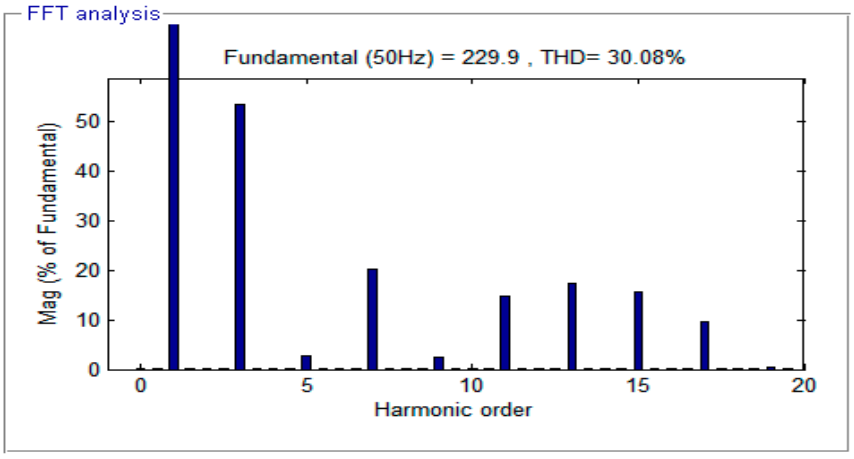

Figure 18. THD analysis of TLBDCLCHB inverter output using EPCAD technique.

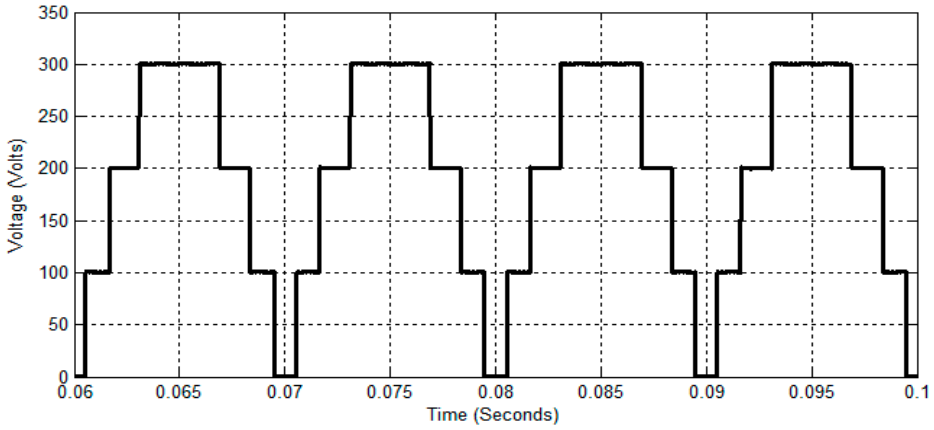

Figure 19. Inverter output across LGU using the SPWCAD technique.

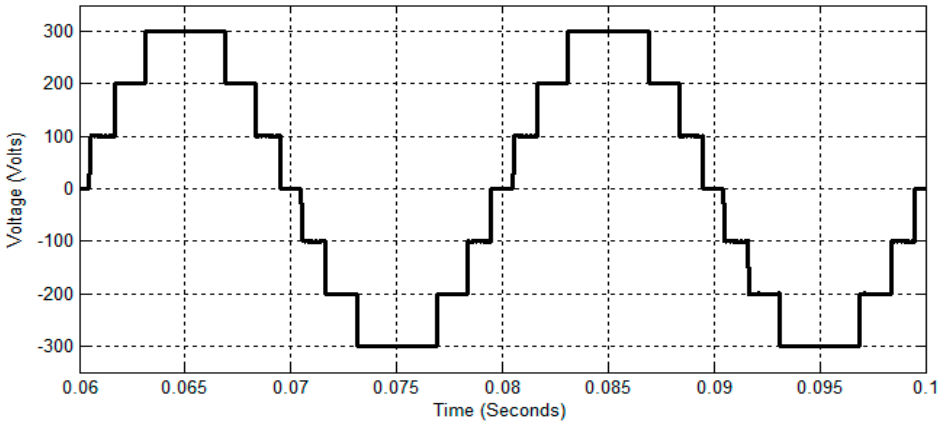

Figure 20. TLBDCLCHB inverter output using the SPWCAD technique.

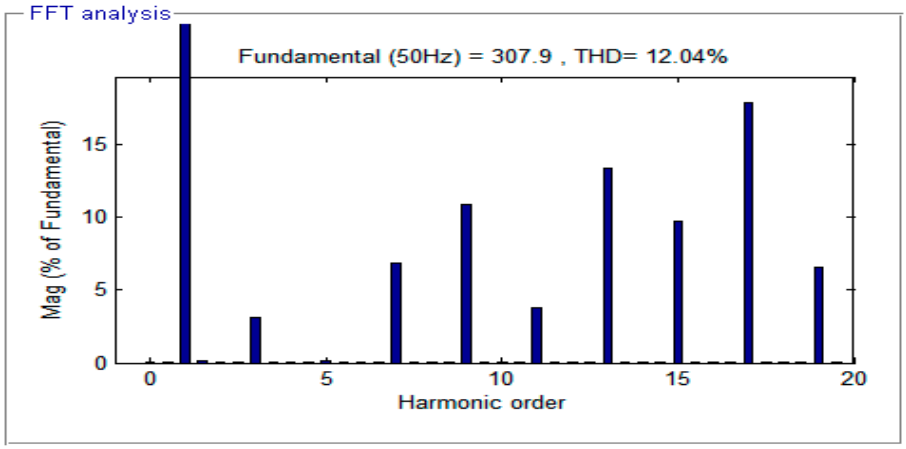

Figure 21. THD analysis of the TLBDCLCHB inverter output using the SWPCAD technique.

6.3.1. Using the EPCAD Technique

Figure 16 shows the output voltage across the LGU in the DCLCHB inverter. Referring to Figure 16, the LGU generates a unipolar stepped waveform, and it can be converted to a bipolar stepped wave using PSGU. Figures 17 and 18 show the seven-level stepped output phase voltage and its THD analysis of the TLBDCLCHB inverter using the EPCAD technique for the duty cycle of 0.5. It is observed that the magnitude of the fundamental output phase voltage and its RMS value is 229.9 V and 162.5 V, respectively. Also, the THD of the proposed TLBDCLCHB inverter output using the EPCAD technique is 30.08%.

6.3.2. Using the SPWCAD Technique

The unipolar output phase voltage across the LGU in the DCLCHB inverter using the SPWCAD technique is shown in Figure 19. Figures 20 and 21 show the seven-level stepped output phase voltage and its THD analysis of the TLBDCLCHB inverter using the SPWCAD technique for the duty cycle of 0.5 with M_i = 0.8. It is observed that the magnitude of the fundamental output phase voltage and its RMS value is 307.9 V and 217.7 V, respectively. Also, the THD of the proposed TLBDCLCHB inverter output using the SPWCAD technique is 12.04%.

6.4. Experimental Validation of the TLBDCLCHB Inverter System Using an FPGA-Based Pulse Generation

The model of the proposed TLBDCLCHB inverter system-fed R-load is implemented employing Xilinx Spartan FPGA-based pulse generation [19,20] to validate the Simulink results. The block diagram, Xilinx Spartan6 development board, and the prototype model of the TLBDCLCHB inverter system using an FPGA is shown in Figures 22–24, respectively. It consists of TLBC, the DCLCHB inverter, a personal computer (PC), an FPGA controller, R-load, buffer circuit, optocoupler, and driver circuit. The output of TLBC-fed DCLCHB inverter using an FPGA controller is shown in Figure 25.

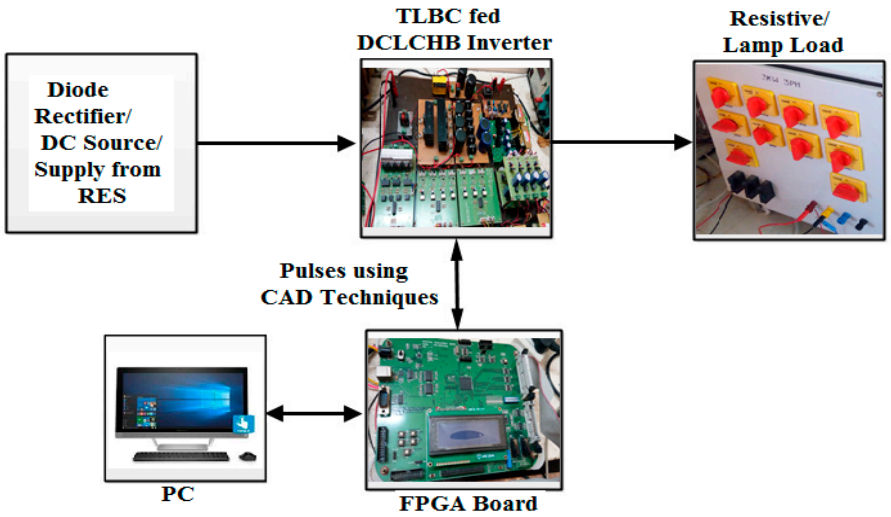

Figure 22. Block diagram of the TLBDCLCHB hardware implementation.

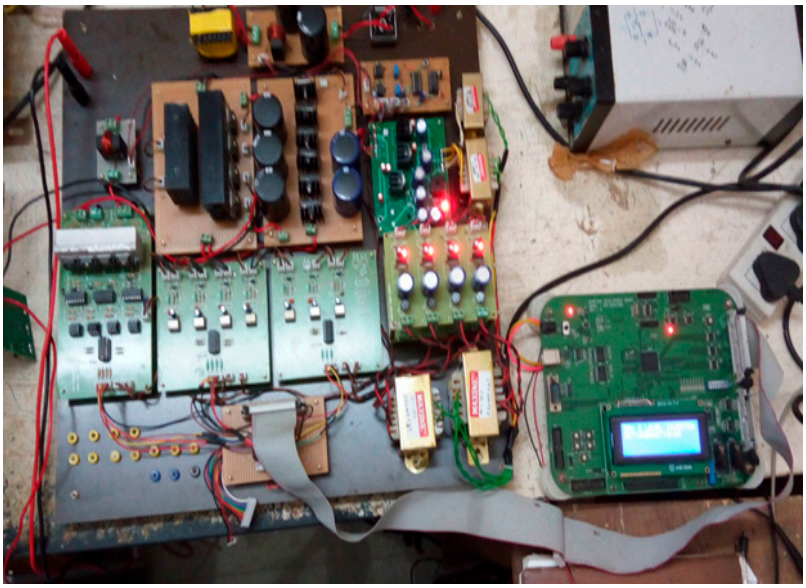

Figure 23. Hardware implementation of the TLBDCLCHB inverter system with an FPGA controller.

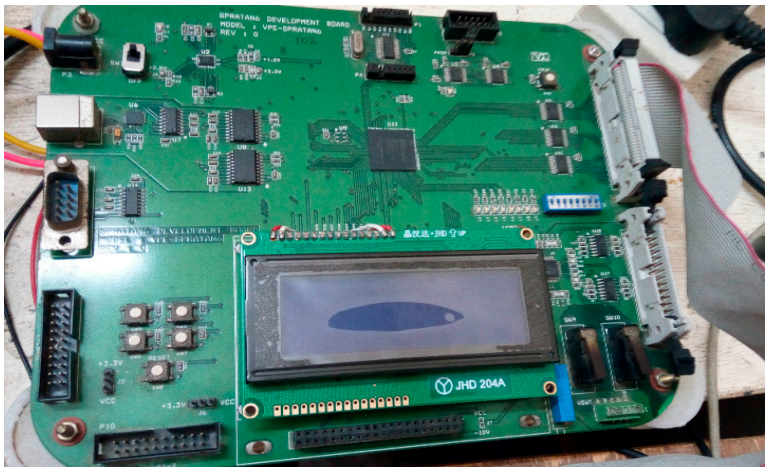

Figure 24. Xilinx Spartan6 development board.

Figure 25. Seven-level stepped output voltage of TLBC-fed DCLCHB inverter system.

Referring to Figure 26, the TLBC output voltage across each capacitor and the total DC-link voltage are shown in Channel 1 (CH1) and Channel (CH2), respectively, for D = 0.5. It is observed that CH1 and CH2 voltages are boosted to 100 V and 300 V, respectively.

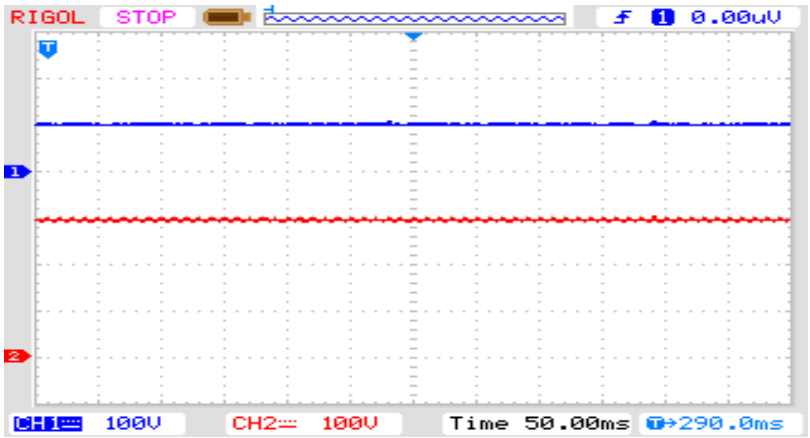

Figure 26. Voltage across the capacitor CH1 and total DC-link voltage of TLBC CH2 for D = 0.5.

Figures 27 and 28 show the generation of the pulse for the LGU switches (S_1 to S_6) in the DCLCHB inverter to generate the stepped output waveform using EPCAD and SPWCAD techniques, respectively, for the modulation index of 0.8. Figure 29 shows the generation of the pulse for the PSGU switches (P_1 to P_4) in the DCLCHB inverter to generate the positive and negative levels using an H-bridge inverter.

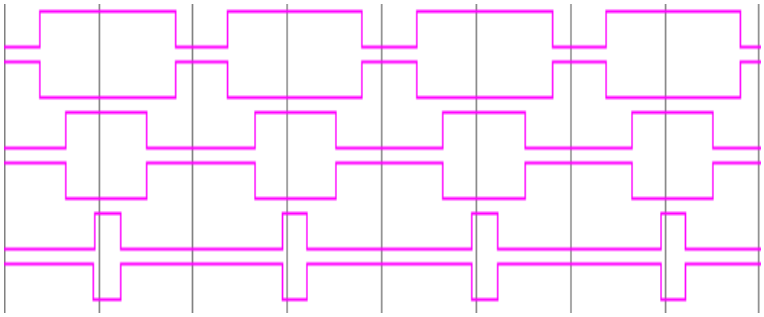

Figure 27. Generation of pulses for the LGU switches (S_1 to S_6) in the DCLCHB inverter using the EPCAD technique through Xilinx ISE.

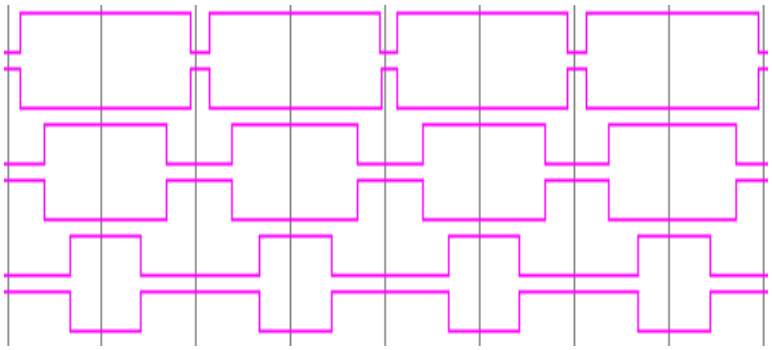

Figure 28. Generation of pulses for the LGU switches (S_1 to S_6) in the DCLCHB inverter using the SPWCAD technique through Xilinx ISE.

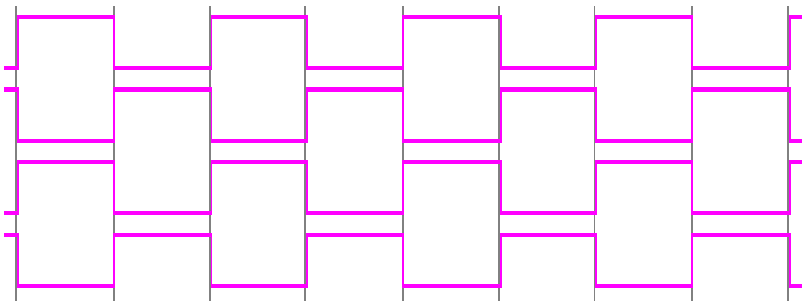

Figure 29. Generation of pulses for the PSGU switches (P_1 to P_4) in the DCLCHB inverter using a pulse generator through Xilinx ISE.

Figures 30 and 31 represent the TLBDCLCHB inverter system experimental output phase voltage and its harmonic spectrum using the EPCAD technique for the generation of a seven-level stepped output voltage. Referring to Figures 30 and 31, it is observed that the RMS value of the output phase voltage is 161.7 V and its THD is 31.5%.

Figures 32 and 33 represent the TLBDCLCHB inverter system experimental output phase voltage and its harmonic spectrum using the SPWCAD technique for the generation of a seven-level stepped output voltage. Referring to Figures 32 and 33, it is observed that the RMS value of the output phase voltage is 216 V and its THD is 11.5%.

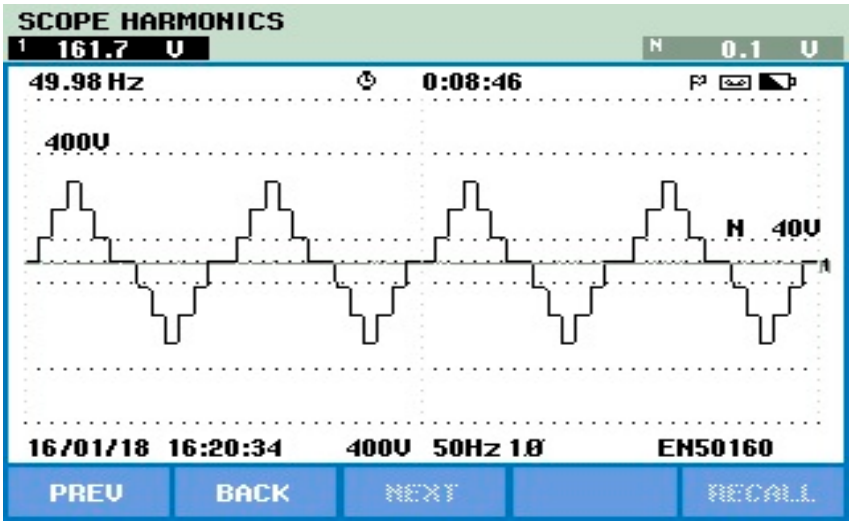

Figure 30. TLBDCLCHB inverter output using the EPCAD technique.

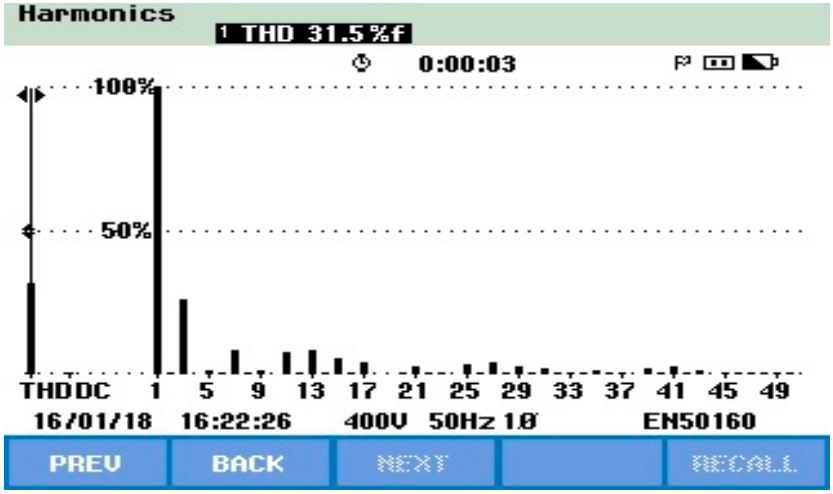

Figure 31. THD analysis of the TLBDCLCHB inverter output using the EPCAD technique.

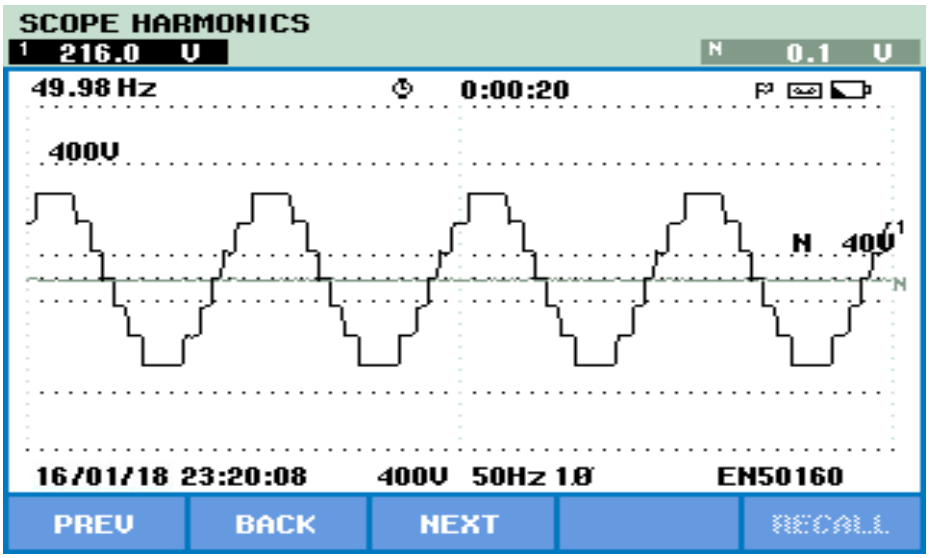

Figure 32. TLBDCLCHB inverter output using the SPWCAD technique.

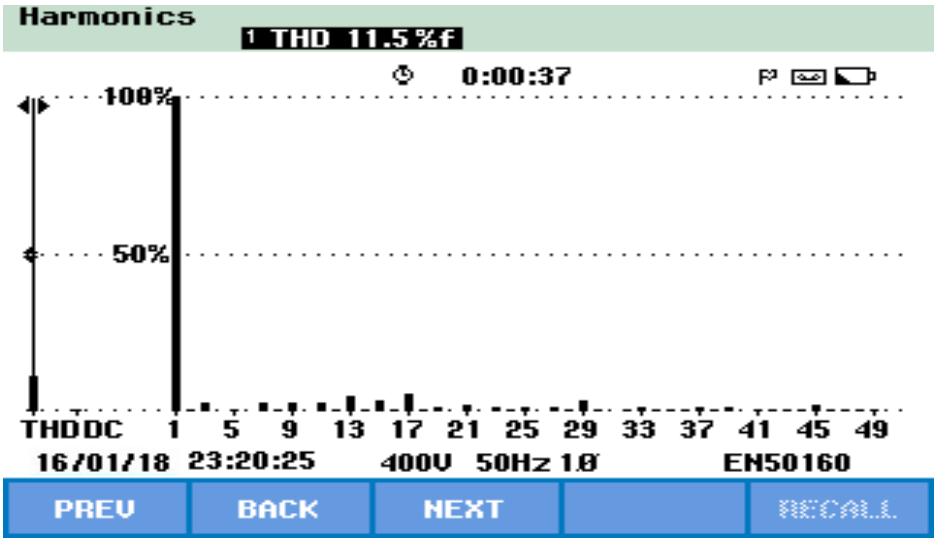

Figure 33. THD analysis of the TLBDCLCHB inverter output using the SPWCAD technique.

6.5. TLBDCLCHB Inverter System Analysis and Comparison Using CAD Techniques

In this study, theoretical and simulation results of the proposed TLBDCLCHB inverter system for the generation of a seven-level stepped output phase voltage using the EPCAD and SPWCAD techniques have been validated experimentally through an FPGA-based pulse generation. Tables 7 and 8 analyze the output phase voltage (V_{rms}) and THD of the TLBDCLCHB inverter system for different duty cycles, i.e., D = 0.4, 0.5, and 0.6. The THD of the prototype model for the proposed CAD techniques are conceded using a Fluke 435 power quality analyzer, and the results are presented in Figures 16–29 for the EPCAD and SPWCAD techniques.

Table 7. Simulation comparison of (V_{rms}) and % THD.

Duty Cycle (D)	EPCAD Technique		SPWCAD Technique	
	V_{rms} (V)	THD (%)	V_{rms} (V)	THD (%)
0.4	135.7	29.71	185.5	12.02
0.5	162.5	30.08	217.7	12.04
0.6	203.6	29.90	272	12.07

Table 8. Experimental comparison of (V_{rms}) and %THD.

Duty Cycle (D)	EPCAD Technique		SPWCAD Technique	
	V_{rms} (V)	THD (%)	V_{rms} (V)	THD (%)
0.4	134.6	31.8	184.7	11.8
0.5	161.7	31.5	216	11.5
0.6	202.1	31.5	270.9	11.7

Referring to Tables 6–8, it is inferred that the most extreme output phase voltage and lower THD are accomplished by utilizing the SPWCAD technique rather than the EPCAD technique. From the simulation, it is obtained that V_{rms} and %THD content in the EPCAD technique are 161.7 V and 31% for D = 0.5. Whereas, in the case of the proposed SPWCAD technique, V_{rms} is 216 V and %THD is only 11.5% for D = 0.5 by considering M_i = 0.8. From the experimental results, it is observed that the V_{rms} and %THD content in the EPCAD technique are 161.7 V and 31% for D = 0.5. For the proposed SPWCAD technique, V_{rms} is 216 V and %THD is only 11.5% for D = 0.5 by considering M_i = 0.8. Therefore, theoretical values V_{rms} and %THD shown in Table 6 are validated with the simulation and

experimental results with a tolerable error of ±2%. From the analysis, it is noticed that the magnitude of V_{rms} varies with respect to the duty cycle, but there is only a slight deviation in THD from 0.4 to 0.6.

7. Conclusions

In this paper, a TLBC-fed DCLCHB inverter system has been suggested to generate a seven-level stepped output phase voltage using a single DC source for better performance, efficiency, and reduced cost and size of the inverter. It also presented two control techniques for the DCLCHB inverter based on conducting angle determination, namely, EPCAD and SPWCAD techniques. Here, the SPWCAD technique gives the most extreme output phase voltage and lower THD compared to the EPCAD technique but the SPWCAD technique involves several trigonometric functions. However, same trigonometric functions are repeated; therefore, it is easy to acquire the conducting angles once the equations are derived based on the volt-second balance. In addition, TLBC has been suggested to achieve auto voltage balance and high voltage gain. Therefore, upon considering all the advantages, the proposed TLBDCLCHB inverter system is a good alternative for PV applications compared to the conventional boost-based MLI systems.

Author Contributions: A.K.D.V. and S.B.Ch. contributed to the main idea of this article. N.R.S. developed the Simulink model and performed the experiments, N.R.S., A.K.D.V. and S.B.Ch. all contributed to manuscript writing and revisions. All authors approved the final version to be published.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

CAD	conducting angle determination
DCLCHB	DC-link cascade H-bridge
EPCAD	equal-phase CAD
LGU	level generation unit
THD	total harmonic distortion
TLBC	three-level boost converter
TLBDCLCHB	three-level boost DC-link cascade H-bridge
MLI	multilevel inverter
PSGU	phase sequence generation unit
PWM	pulse width modulation
PV	photovoltaic
SPWCAD	step pulse wave CAD

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