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Comparative Analysis of Si- and GaN-Based Single-Phase Transformer-Less PV Grid-Tied Inverter

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Abstract: Recently, the interest in grid-tied PV transformer-less inverters has increased rapidly, because of their higher efficiency and lower cost compared to traditional line transformer inverters. This paper presents a new modified transformer-less topology derived from H5 inverter, and provides a detailed comparison between the use of GaN and Si devices for the proposed topology. Detailed operation modes, inverter structure and switching strategy of the proposed topology are presented. Datasheet information, conduction losses, switching losses, and heat sink requirements are studied and analyzed to provide an accurate comparison between GaN and Si power devices for the proposed topology operating at unity power factor. The results show that, GaN power devices significantly reduce the power losses in the system, which consequently allow a significant increase in either inverter power rating or switching frequency. Thus, the use of GaN power devices for the proposed inverter can be more appealing and cost-effective approach.

Keywords: GaN; transformer-less; inverter; PV; SPWM; WBG; efficiency; heatsink; power rating; thermal analysis

1. Introduction

The rising cost of energy and the environmental issues of fossil resources led to the recent interest in renewable energy. Renewable resources provide clean and sustainable energy, which will reduce the pollution emissions; hence protecting the environment. Among renewable resources, photovoltaic (PV) gained a lot of interest in recent years; the power capacity of PV system installations has grown exponentially in the past decades being increased from 5 gigawatts in 2006 to 177 gigawatts in 2014 [1].

PV inverters in residential applications are either single or three phase inverters with or without galvanic isolation. Transformer-less inverter can achieve higher efficiency and lower cost compared to inverters with transformer galvanic isolation [2–5]. In addition, omitting transformer will reduce the system complexity and volume [6,7]. However, the elimination of the transformer will remove the galvanic isolation in the system, which will cause many safety issues.

In the absence of galvanic isolation leakage current will flow through the PV parasitic capacitance due to the high frequency common mode (CM) voltage. This leakage current will lead to higher losses, PV module degradation, electromagnetic interference, and safety issues. To eliminate the leakage current, CM voltage must be kept constant for all switching states. Half-bridge inverter is the typical solution to keep the CM voltage constant [4]. However, half-bridge inverter requires double the DC input voltage of the full bridge inverter, which will require a DC-DC converter with extremely high conversion ratio. As a result, this will lead to a huge decrease in the system efficiency. Full bridge inverter is an attractive solution because it requires only half of the half-bridge input voltage. In addition, it has higher conversion efficiency and small current ripples. However, the variation of the CM voltage at the switching frequency in full bridge inverter can lead to high leakage currents.

Multiple transformer-less inverter topologies have been proposed in the literatures [8,9] to eliminate the leakage current problem in full bridge inverter. One of the solutions proposed to minimize the leakage current is to maintain a constant CM voltage for all switching states [10]. However, such solution requires a higher number of components that increase the system complexity. Another solution to minimize the leakage current is to isolate the two sources of the system (PV, grid) during the zero-state, by modifying the PWM to keep the CM voltage constant [11–14].

Multiple topologies have been developed based on this solution, such as the H5 topology [15] and H6 topology [16]. However, H5 and H6 topologies suffer from high conduction losses because of the high number of switches conducting during the active state. Another high efficient topology was proposed in reference [17] to lower the conduction losses and improve the efficiency by forming a new current path and reduce the number of conducting switches during the active state.

To enhance the efficiency and reliability of the transformer-less inverter it is necessary to choose the appropriate switching devices. WBG devices such as: SiC MOSFETs, and GaN HEMTs, have been widely employed in renewable energy to enhance the efficiency and reduce the power losses of the system. Benefits and potential performance enhancement of SiC applications in renewable energy converters have been widely discussed in the available literatures [18–20]. Besides and according to these literatures, by replacing Si IGBT by SiC MOSFET the overall losses of the system can be reduced by half. The use of GaN HEMT in renewable energy has been already discussed, the higher performance of GaN HEMT in terms of energy efficiency being described [21–23]. Using WBG power devices, PV inverter can operate at high switching frequency, which will help reduce the size and the volume of the system which will lower the system overall cost.

In this work, a comprehensive loss analysis of a new modified topology derived from H5 inverter is presented. The new topology form a new current path to reduce the conduction losses by reducing the conducting switches during the active state. Therefore, the current of the proposed topology in the active mode flow through four switches. As a result, compared to H5 topology and H6 topology the proposed topology has achieved the lowest conduction losses. Moreover, the potential benefit of using Wide Band-Gap power switching devices in PV application is analyzed. Furthermore, a detailed comparison between the use of GaN and Si devices for the proposed topology is also included. The loss comparison study uses Datasheet information, conduction losses, switching losses, and heat sink requirements to provide an accurate comparison between GaN and Si power devices. Detailed operation modes, inverter structure and switching strategy of the proposed topology are presented. Sinusoidal Pulse Width Modulation (SPWM) is applied, to keep a constant CM Voltage during all modes of operation and reduce the leakage current [17].

This paper is organized as follows. Operation modes and principle are proposed in Section 2. A theoretical modeling and calculation of the system power loss is shown in Section 3 Performance comparison between Si MOSFET and GaN HEMT is discussed in Section 4. In Section 5, the simulation results of the proposed topology are presented and two switching devices are compared in terms of power losses and efficiency. A thermal analysis of each switching device and the heat sink design and simulation is included in Section 6. Finally, conclusions are summarized in Section 7.

2. Proposed Inverter Description and Operation Principle

2.1. Proposed Topology

The proposed design is derived from H5 topology in Figure 1, by disconnecting S5 from S1 and connect it to terminal A; during positive half cycle the current will flow through switches S4 and S5. Also, an extra switch S6 is added between the DC link and terminal B which will form a new current path. So, the current during negative half cycle active mode will flow through switches S6 and S2. Thus, a new transformer-less inverter topology is derived as shown in Figure 2, where S2, S4, S5 and S6 are high frequency switches, and S1 and S3 are low frequency freewheeling switches. The new topology forms new current paths which will lower the conduction loss when compared

to H5 topology. Therefore, the current of the proposed topology in the active mode flow through four switches. As a result, compared to H5 topology and H6 topology the proposed topology has achieved the lowest conduction losses. Table 1 shows a comparison between the proposed topology, H5 topology and H6 topology in terms of the number of conducting switches during the active states.

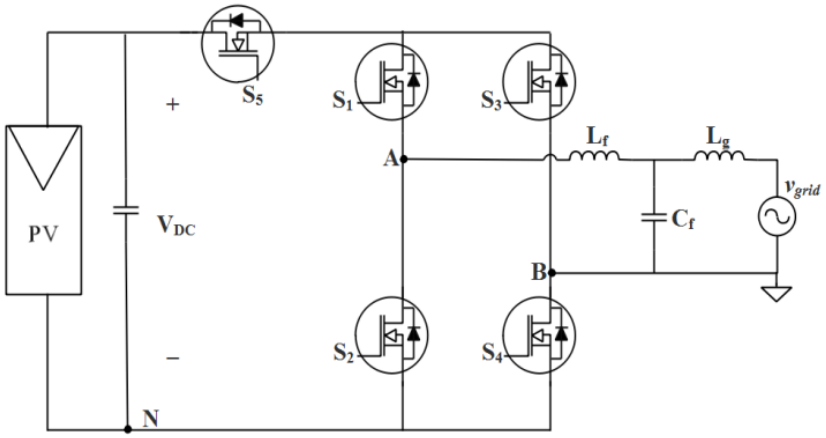


Figure 1. H5 topology.

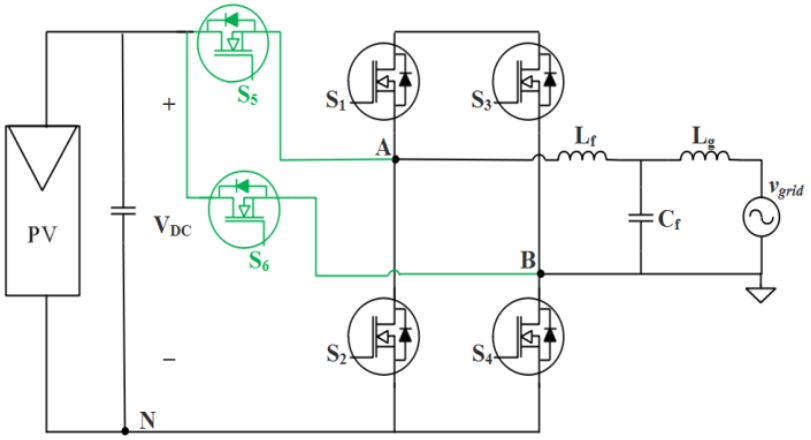


Figure 2. Proposed topology derived from H5.

Table 1. Comparison of conducting devices fro different topologies.

	H5	H6	Proposed Topology
Total number of devices	5	6	6
Number of conducting devices ($v > 0$)	3	3	2
Number of conducting devices ($v < 0$)	3	2	2
Total Number of conducting devices during active modes	6	6	4
Number of devices in freewheeling	2	2	2

2.2. Operation Modes Analysis

The gate drive signals of the proposed topology are shown in Figure 3, where vg is the grid voltage, I_{ref} is the reference current of the system, and vgs1, vgs2, vgs3, vgs4, vgs5 and vgs6 are the gate drive signals of switches S1, S2, S3, S4, S5 and S6, respectively for unity power factor. Modes of

operation of the proposed topology are shown in Figure 4. There are four operation modes to generate inverter output voltage:

$$V_{Inv} = \begin{cases} +V_{DC} \\ 0 \\ -V_{DC} \end{cases} \quad (1)$$

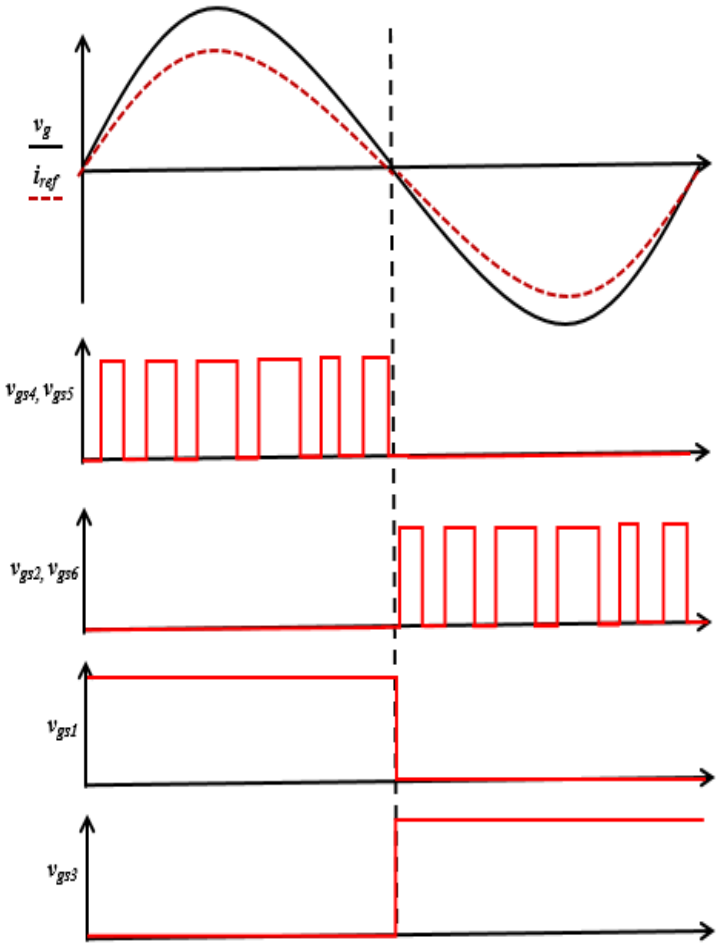


Figure 3. Gate drive signals with unity power factor.

In Mode 1, S1, S4 and S5 are turned ON, which is the positive half-period in the active state and all other switches are turned OFF. The current during this mode is flowing through S4 and S5. $V_{AB} = V_{DC}$, and the Common Mode voltage $V_{CM} = (V_{AN} + V_{BN})/2 = (V_{DC} + 0)/2 = V_{DC}\ /2$.

In Mode 2, S1 is turned ON, which is the positive half-period in the freewheeling state and all other switches are turned OFF. The current during this mode is flowing through S1, and the anti-paralleled diode of S3. $V_{AB} = 0$, and $V_{CM} = (V_{AN} + V_{BN})/2 = (V_{DC}/2 + V_{DC}/2)/2 = V_{DC}\ /2$.

In Mode 3, S2, S6 and S3 are turned ON, which is the negative half-period in the active state and all other switches are turned OFF. The current during this mode is flowing in the opposite direction through S6 and S2. $V_{AB} = -V_{DC}$, and $V_{CM} = (V_{AN} + V_{BN})/2 = (0 + V_{DC}\ )/2 = V_{DC}/2$.

In Mode 4, S3 is turned ON, which is the negative half-period in the freewheeling state and all other switches turned OFF. The current during this mode is flowing through S3, the anti-paralleled diode of S1. $V_{AB} = 0$, and $V_{CM} = (V_{AN} + V_{BN})/2 = (V_{DC}/2 + V_{DC}/2)/2 = V_{DC}\ /2$.

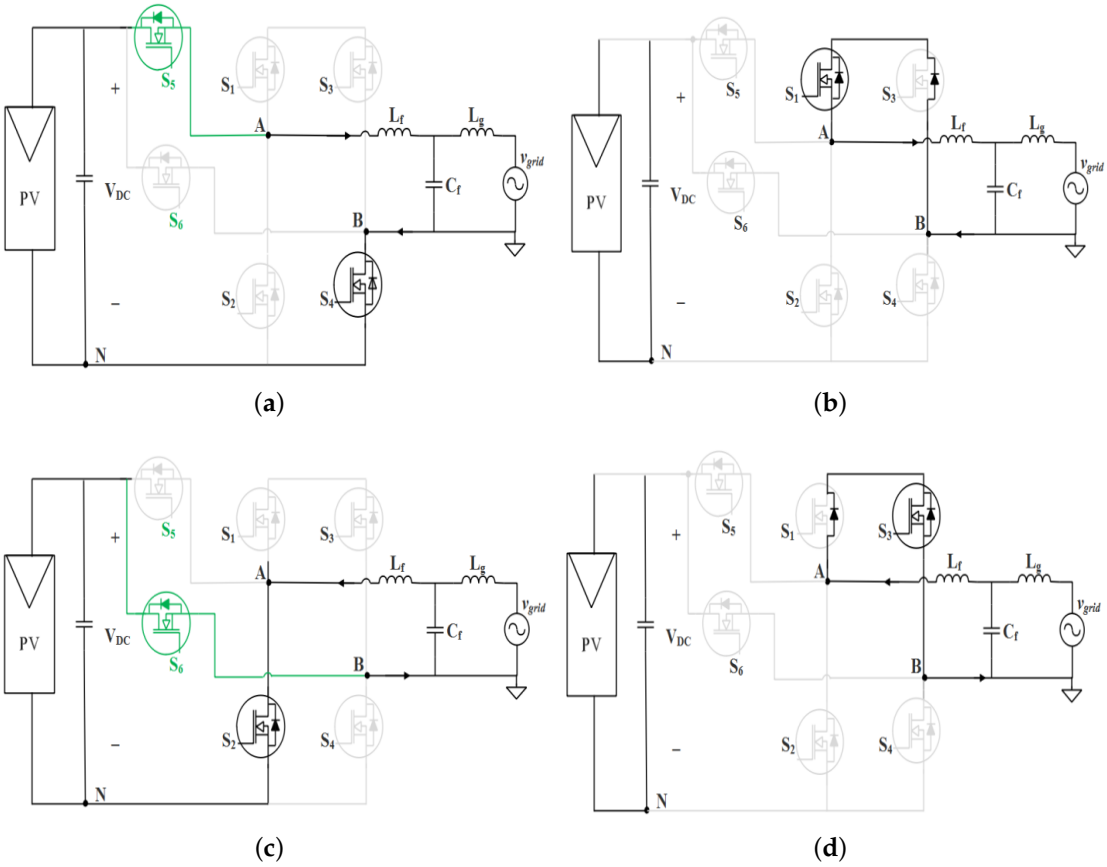


Figure 4. Proposed topology operational modes: (**a**) Active state positive half- cycle; (**b**) Zero-state positive half cycle; (**c**) Active state negative half- cycle; (**d**) Zero-state negative half cycle.

3. Theoretical Power Loss Model Calculation

The power losses of the semiconductor devices are analyzed using different power loads. The semiconductor power device losses are divided into conduction and switching losses. The switching losses can be divided to Switch-ON losses and Switch-OFF losses. The semiconductor power devices losses are explained and derived in detail in [17,24]. To calculate the conduction losses, voltage drop across each device must be identified and is given by:

$$v_{DS}(MOSFET) = i(t) * R_{DS} \tag{2}$$

$$v_{AK}(Diode) = V_f * R_{AK} \tag{3}$$

where v_{DS} is MOSFET drain to source voltage drop and R_{DS} is the MOSFET ON state resistance. V_{AK} is the voltage drop between the diode anode and cathode, V_f is diode voltage drop under zero current condition and R_{AK} is the diode ON resistance. The current that passes the device is $i(t)$. So, the conduction losses of one device during active state can be calculated as follow:

$$P_{Con_{active}} = \frac{1}{2\pi}\int_0^{\pi} v_{con} * i(t) * D_{active}(t) d(\omega t) \tag{4}$$

$$i(t) = I_m sin(\omega t + \theta) \tag{5}$$

$$D_{active}(t) = M sin(\omega t) \tag{6}$$

where I_m is the peak in the inverter output current. ω is the angular frequency, θ is the phase displacement between voltage and grid current, D_{active} is the duty ratio during active state and M can take a value between 0 and 1. The conduction losses of one device during zero states can be calculated as follow:

$$P_{Con_{zero}} = \frac{1}{2\pi}\int_0^{\pi} v_{con} * i(t) * D_{zero}(t) d(\omega t) \tag{7}$$

$$D_{zero}(t) = 1 - Msin(\omega t) \tag{8}$$

where D_{zero} is the duty ratio during zero state. The switching loss for one device during turn on and turn off are given by:

$$P_{Switch\_on} = (\frac{I_m V_{DC}}{2\pi}) \cdot f_{sw} \cdot (\frac{E_{on}}{V_{test} I_{test}}) \tag{9}$$

$$P_{Switch\_off} = (\frac{I_m V_{DC}}{2\pi}) \cdot f_{sw} \cdot (\frac{E_{off}}{V_{test} I_{test}}) \tag{10}$$

where E_{on} E_{off} are the turn on and turn off energy losses. These energy losses are measured for specific test condition (specific test voltage V_{test} and test current I_{test}).

For the proposed inverter topology in Figure 2, four devices (either HEMTs or MOSFETs) in series are conducting current during the active states, while during the zero state the current flow through two devices (either HEMTs or MOSFETs) and two diodes. The low-frequency switching losses are neglected. The conduction and switching losses of the proposed inverter can be given by:

$$P_{Con_{active}} = 4(P_{Con_{active}}(HEMTorMOSFET)) \tag{11}$$

$$P_{Con_{zero}} = 2(P_{Con_{zero}}(HEMTorMOSFET) + P_{Con_{zero}}(Diode)) \tag{12}$$

$$P_{SW_{Loss}} = 4(P_{Switch\_on} + P_{Switch\_off}) \tag{13}$$

As can be seen from the power loss calculations the proposed topology achieves lower conduction losses than that of H5 topology, while maintaining the same switching losses.

For the proposed PV system the dc link voltage is 400 V, which means, 650-V rated devices are required for the switching devices in this application. Among the numerous switching devices available in market today, Si CoolMOS and GaN switching devices are the latest advancement in power semiconductor technology. CoolMOS has been used widely in power converter systems because of their relatively low on-resistance. However, CoolMOS is limited to low switching speed, and there is a trend to increase the switching frequencies to provide small and cost effective power supplies. GaN power devices are the most effective solution to achieve this goal with lower power losses than any other power switching device because of their high electron mobility, and high breakdown field. The new introduced 650-V GaN HEMT is a promising device to be used in PV application at high switching frequency and high loads.

4. Performance Evaluation of Si MOSFET and GaN HEMT

Evaluating the performance and loss profiles of Si CoolMOS and GaN HEMT requires study and analysis of switching and conduction characteristics of each device for the proposed inverter application. Manufacturer's datasheets can be used to provide the detailed data of the conduction characteristics of each device. However, using the data sheet to determine the switching characteristics is difficult because normally, switching characteristics are determined for specific operation conditions. Therefore, to provide an accurate comparison between Si CoolMOS and GaN HEMT in terms of switching characteristics and losses, their switching characteristics and losses are measured using double pulse test circuit to provide the same operating conditions that will be used in the proposed system.

4.1. Conduction Characteristics

The voltage drop and the current that flows through the power switching devices are used to determine the conduction losses. For the selected switching devices Si MOSFET (CoolMOS) IPW60R045CP and GaN HEMT GS66516T, the forward voltage versus current at different temperature can be extracted from the manufacturer's datasheet of each device, and they are shown in Figure 5 [25,26]. These forward voltages are used to determine the conduction losses of each device. It can be noticed from Figure 5 that GaN HEMT has smaller voltage drop than Si CoolMOS over the current range of the system; thus, GaN HEMT will have lower conduction losses than Si CoolMOS.

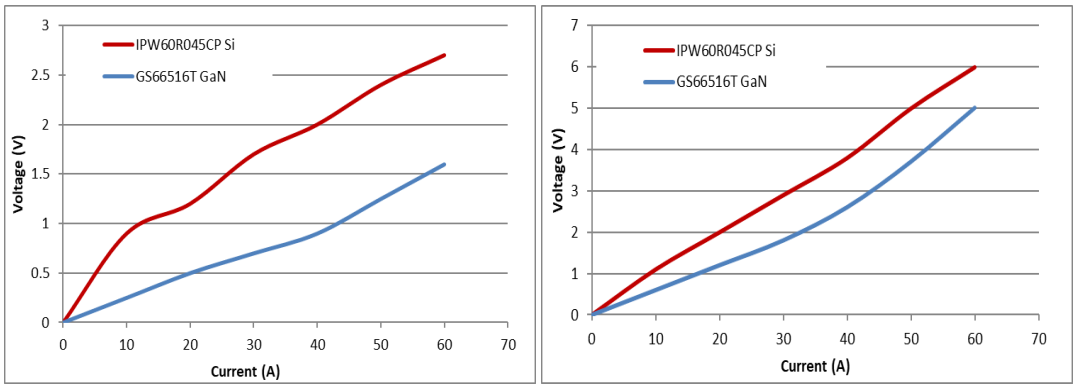


Figure 5. Forward voltages of Si MOSFET and GaN HEMT at various current and junction temperature: (**a**) Si MOSFET and GaN HEMT forward voltage at 25 °C junction temperature; (**b**) Si MOSFET and GaN HEMT forward voltage at 150 °C junction temperature.

4.2. Switching Characteristics

As mentioned previously, to provide an accurate comparison between Si CoolMOS and GaN HEMT in terms of switching characteristics and losses, their switching characteristics and losses are measured using a double pulse test circuit shown in Figure 6 to provide the same operating conditions that will be used in the proposed system. Figure 7 shows the turn-on and turn-off waveforms of Si MOSFET and GaN HEMT at 400 V and 30 A.

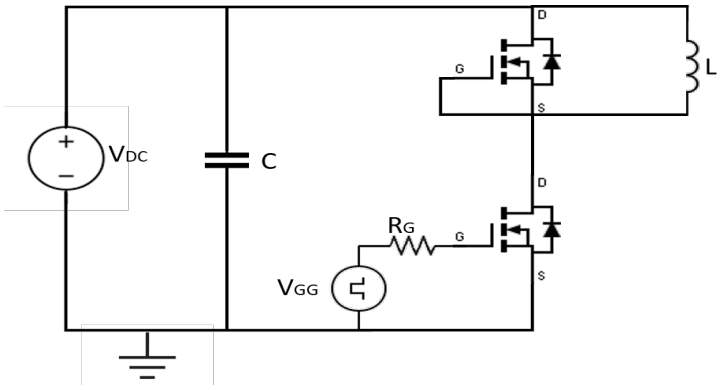


Figure 6. Double Pulse Test Circuit.

Figure 7a,b show the drain-source voltage, and drain current during turn-on transition for Si MOSFET and GaN HEMT, respectively. Figure 7c,d show the drain-source voltage, and drain current during turn-off transition for Si MOSFET and GaN HEMT, respectively. It can be seen from the figures the superior performance in the switching characteristics of the GaN HEMT in terms of di/dt and dv/dt. As an example, from Figure 7c,d, during turn-off stage GaN HEMT switches at 15.8 kV/µs

while Si MOSFET switches at 4.9 kV/µs. Table 2 presents the switching characteristics for both devices in terms of di/dt and dv/dt during turn-on and turn-off transitions.

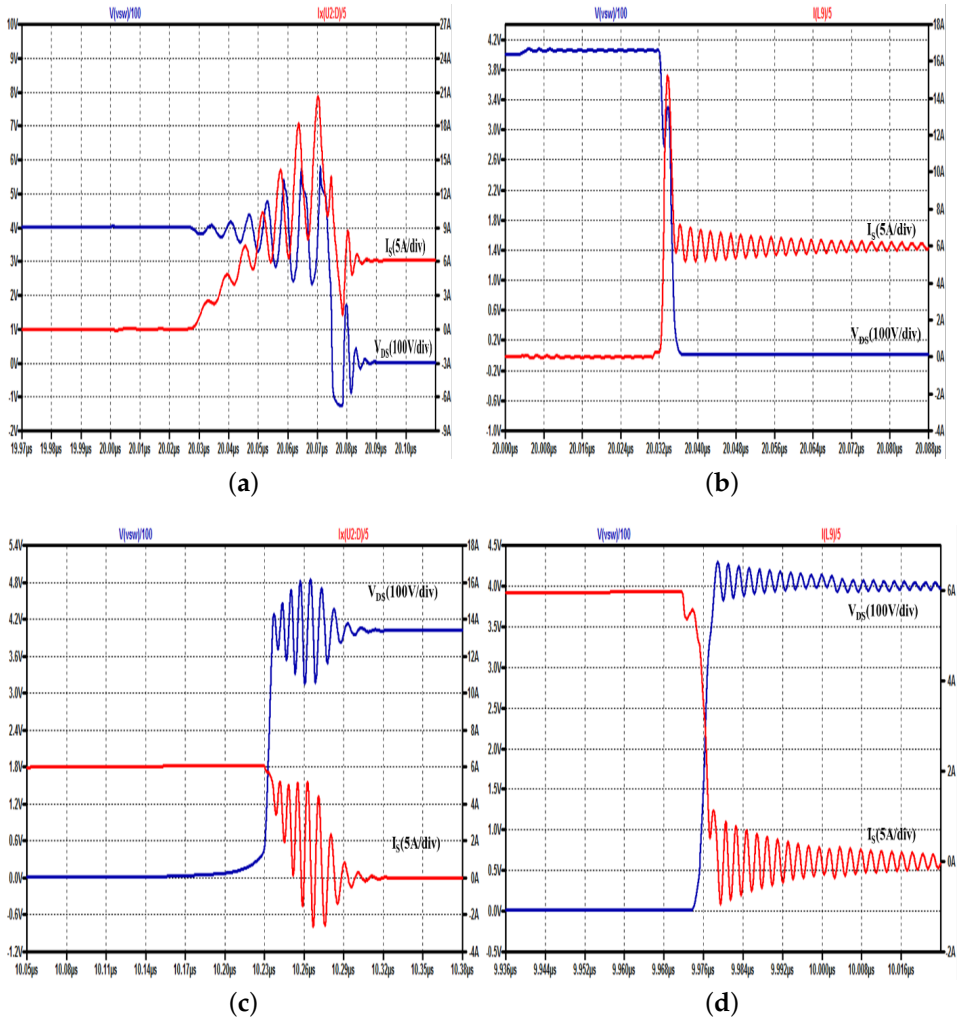


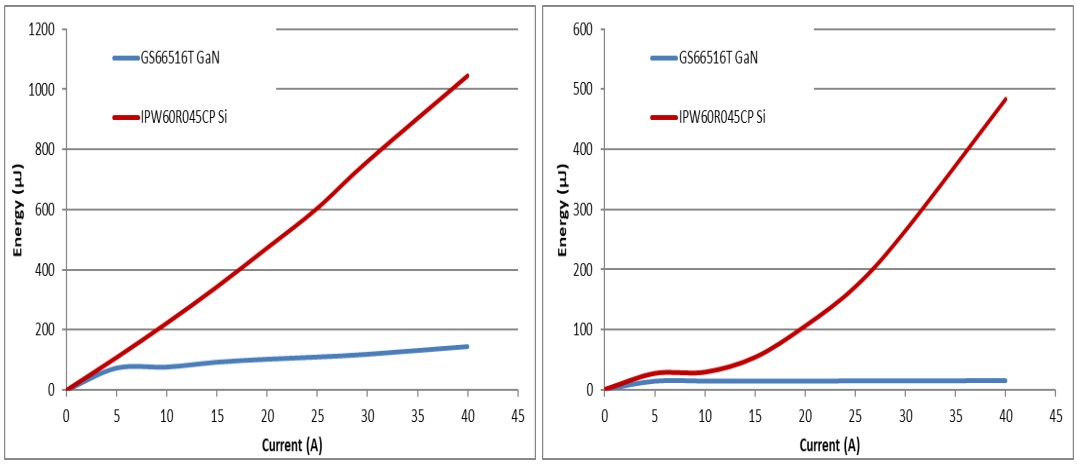
Figure 7. The turn-on and turn-off waveforms of Si MOSFET and GaN HEMT at 400 V and 30 A: (**a**) Si MOSFET Turn-on; (**b**) GaN HEMT Turn-on; (**c**) Si MOSFET Turn-off; (**d**) GaN HEMT Turn-off.

Table 2. Switching Characteristics.

	Turn-On		Turn-Off	
	Si	**GaN**	**Si**	**GaN**
dv/dt (kV/µs)	6	9.6	4.9	15.8
di/dt (kA/µs)	0.63	4	0.4	3

The switching losses can be obtained by measuring the voltage and the current at different operating conditions. Thus, the switching energy losses can be obtained by integrating the product of the collected voltages and currents. Figure 8 shows the turn-on and turn-off energy losses of Si MOSFET and GaN HEMT. Table 3 presents the values of the turn-on and turn-off switching energy losses shown in Figure 8. It can be noticed that the Si MOSFET turn-on switching energy loss is more than five times that of the GaN HEMT. The most attractive characteristic of GaN HEMTs is their significantly low turn-off energy loss which is almost constant over the current range of the system. Conversely, the turn-off energy loss of the Si MOSFET increases linearly with the current. It can be seen from Figure 8 and Table 3 that the switching energy loss of the Si MOSFET at 20 A (105.96 µJ) is

more than seven times that of GaN HEMT at 20 A (14.1 µJ) and Si MOSFET at 40 A (1045.6 µJ) is more than 30 times that of GaN HEMT at same current (14.8 µJ).



(**a**) (**b**)

Figure 8. Turn-on and Turn-off switching energy losses of Si MOSFET and GaN HEMT: (**a**) Turn-On; (**b**) Turn-Off.

Table 3. Switching energy losses.

Current (A)	Si MOSFET		GaN HEMT	
	E_{on}(µJ)	E_{off}(µJ)	E_{on}(µJ)	E_{off}(µJ)
0	0	0	0	0
5	109.16	26.86	73.1	14
10	223.17	28.92	76.5	14.1
15	343.9	53.59	92.3	14.2
20	472.86	105.69	102	14.1
25	604.8	170.94	109	14.5
30	760.32	264.29	118.3	14.6
40	1045.6	482.79	143.2	14.8

5. Simulation Results and Discussion

In order to verify the benefits of replacing Si MOSFET with GaN HEMT in the inverter; the proposed topology in Figure 2 was simulated and analyzed using co-simulation between PSIM environment and MATLAB/Simulink Platform. Table 4 shows the simulation specifications. Table 5 shows the switching power devices used in the simulation. The proposed topology power losses and efficiency are compared using two different power devices (Si MOSFET and GaN HEMT). Heatsink design and thermal analysis of the proposed inverter was simulated using COMSOL Multiphysics.

Table 4. Simulation parameters.

Parameter	Value
System Power	5 kW
Input Voltage	400 V
Grid Voltage	120 V
Grid Frequency	60 Hz
Switching Frequency	50 kHz and 200 kHz
Input Capacitance (C_{DC})	1 mF

Table 5. Switching devices parameters.

Parameter	IPW60R045CP	GS66516T
V_{DS} (V)	650	650
I_D (A)	60	60
R_{DS} (mΩ)	45	25
Q_G (nC)	150	12.1
Q_{GS} (nC)	34	4.4
Q_{GD} (nC)	51	3.4
C_{iss} (pF)	6800	520
C_{oss} (pF)	320	130
C_{rss} (pF)	-	4

The most important benefit of replacing the Si MOSFET with GaN HEMT for the proposed inverter is the reduction in overall loss by more than 60% at 50 kHz and more than that at 200 kHz as shown in Figure 9a,b. The significantly low power losses of GaN HEMTs can help improve the efficiency of the overall system and reduce the thermal stress. Moreover, GaN HEMTs can operate at high switching frequencies with lower power losses, which will consequently reduce the total volume of the system.

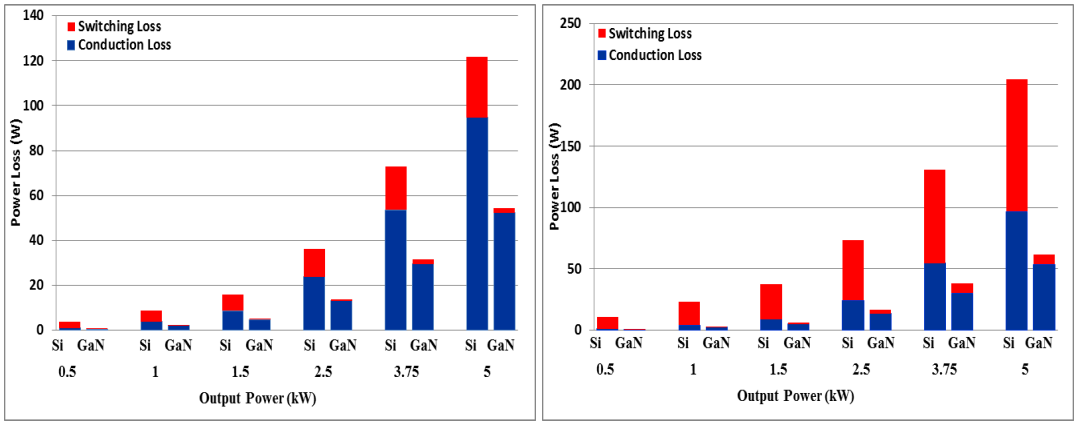


Figure 9. Power losses of Si MOSFET and GaN HEMT: (**a**) at 50 kHz; (**b**) at 200 kHz.

5.1. Efficiency Improvement

The overall efficiency of the system is directly affected by the switching device power losses. Figure 10 shows the efficiency of the proposed topology with Si MOSFETs and GaN HEMTs at different levels of rated power and different switching frequencies. The figure shows the efficiency improvement using GaN HEMTs with more than 2% of improvement at 50 kHz and more than 3% of improvement at 200 kHz. Hence, these results verify the superior performance of the GaN Switching devices over their Si counterparts.

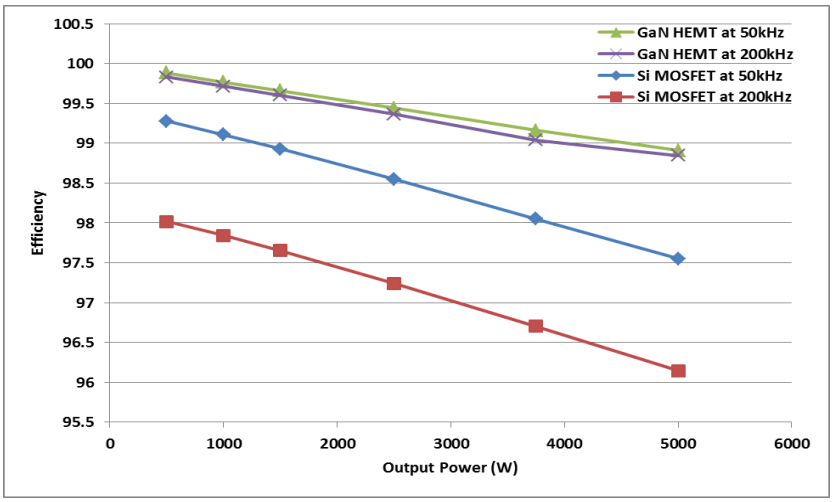


Figure 10. Efficiency comparison of Si MOSFET and GaN HEMT at different switching frequency.

5.2. Passive Component Reduction

Switching the inverter at high switching frequencies can significantly reduce the passive component size. So, by using the previously presented semiconductor loss model, the switching frequency of the inverter that is equipped with GaN HEMT has been increased until the losses of the GaN HEMT are almost equal to the losses of Si MOSFET. Figure 11 shows the results of this process for an output power of 5 kW; as can be seen from the figure, the switching frequency has been increased to 500 kHz for GaN HEMT to reach the balance point where its losses are equal to Si MOSFET losses at 50 kHz. Thus, to reach the point where both devices dissipate the same power the GaN HEMT switching frequency increased to 10 times the switching frequency of the Si MOSFET. This high switching frequency will reduce the filter inductance size significantly since the inductance size is inversely proportional to the switching frequency according to [27]:

$$L_f = \frac{V_{DC}}{4 \times f_{SW} \times 0.2 \times I_{L\_max}} \tag{14}$$

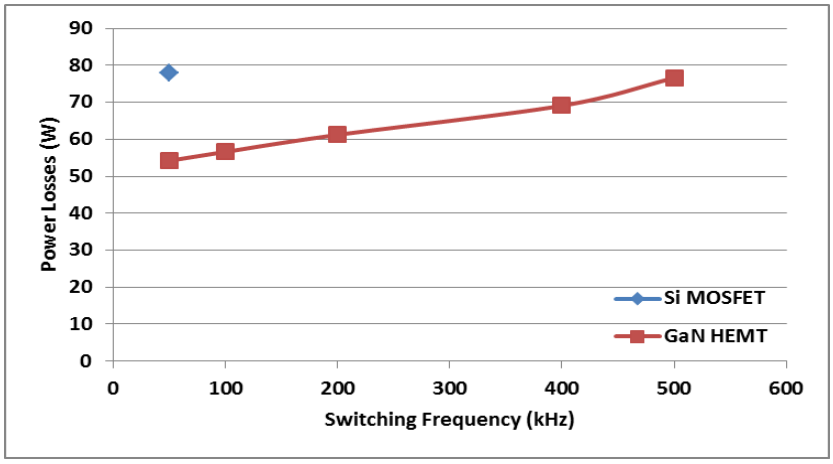


Figure 11. The balance point where GaN HEMT losses at 500 kHz is equal to Si MOSFET losses at 50 kHz.

The inductor current ripple is chosen to be 20% of the maximum output current. Figure 12 shows the effect of increasing the switching frequency on the inductance size. As can be seen from the figure, increasing the switching frequency reduced the inductance size from 600 to 40 µH. Figure 13 shows the

effect of increasing the switching frequency on the magnetic core volume. The magnetic core volume has been reduced from initially 237 to 43.1 cm^3. Accordingly, this will result in a reduction of the inductor weight as demonstrated in Figure 14. The inductor weight was reduced from 618 to 120 g.

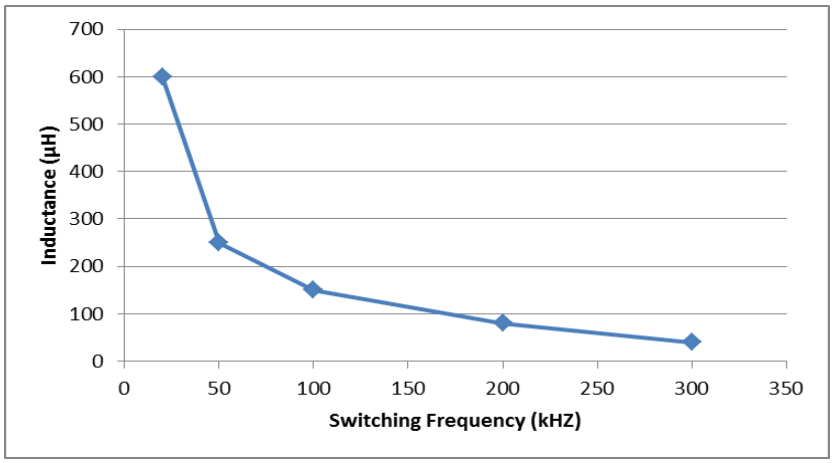


Figure 12. The effect of increasing the switching frequency on inductance size.

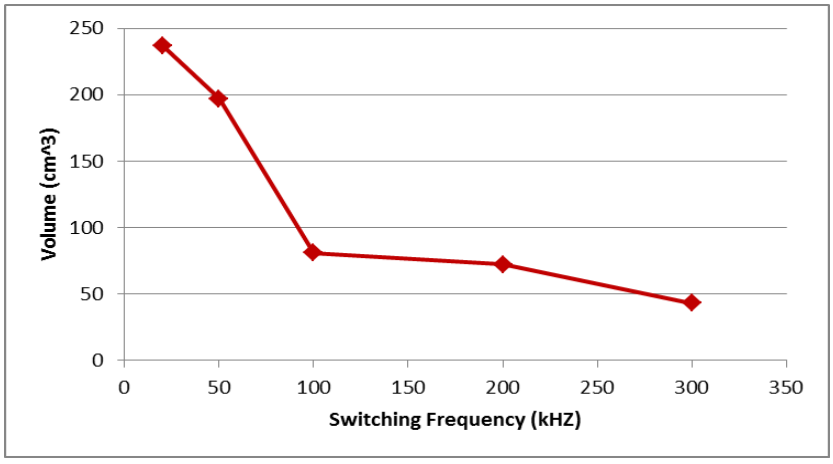


Figure 13. The effect of increasing the switching frequency on magnetic core volume.

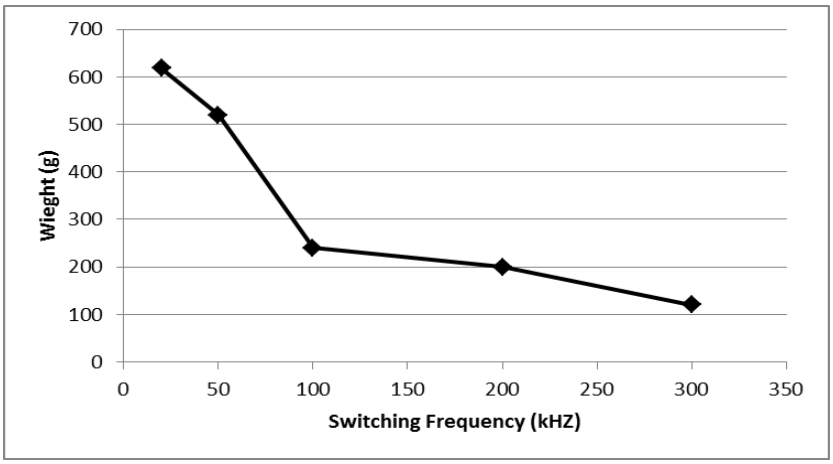


Figure 14. The effect of increasing the switching frequency on the inductor weight.

5.3. Improvement In Power Rating

As mentioned previously, the most important benefit of GaN HEMTs is their low power loss which improves the efficiency and also can be used to improve the power rating of the proposed system. Improving the power rating can be done by increasing the output power of the system using the same heatsink that has been designed for Si MOSFETs. Figure 15 presents this concept, as shown in the figure the output power increased from 2500 W using Si MOSFET to 3750 W using GaN HEMT with the same power losses at 50 kHz switching frequency. Thus, the GaN HEMT-based inverter achieves more than 60% increase in power rating without any additional cooling.

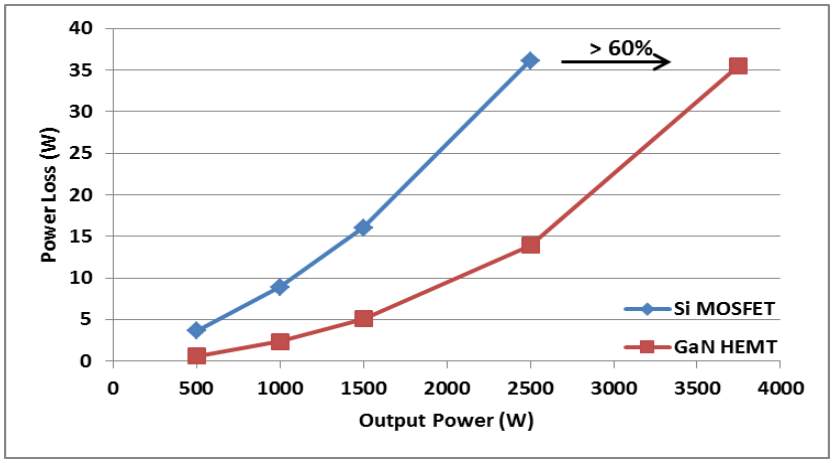


Figure 15. Power rating improvement, output power increase with same power losses.

6. Thermal Design and Simulation Analysis

6.1. Model Outline

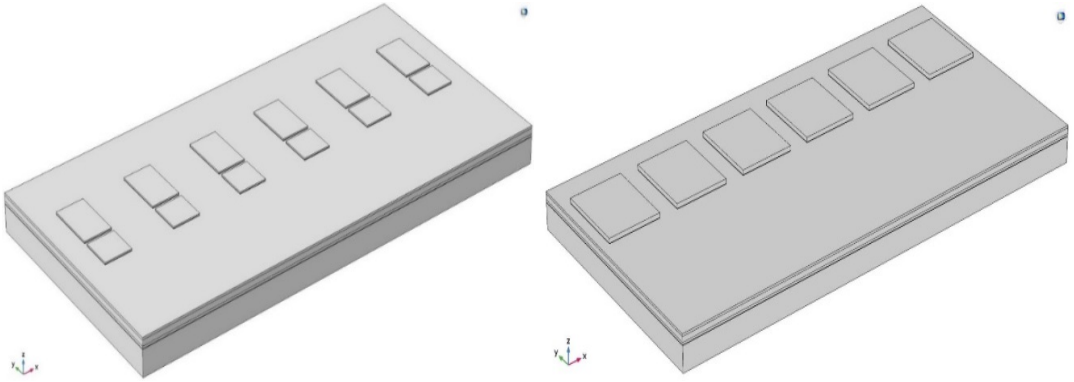
Modelling and thermal performance analysis of heatsinks using simulation platforms have been reported in several literatures [28–32]. Many simulation software are available commercially such as: COMSOL Multiphysics, FLUENT, ANSYS, Pro-MECHANICA, etc. that use numerical methods, Finite Element and Finite Volume Methods (FEM and FEV) along with Computer Aided Design (CAD) tools to model the thermal performance of heatsinks [28–32].

In this paper, COMSOL Multiphysics was used to create two 3D models of a 6-pack MOSFET module with Silicon (Si) and Gallium Nitride (GaN) as their respective semiconductor materials. To reduce the modules temperature and to compare the thermal performance of each semiconductor, heatsinks were added to the design. Finite Element Analysis (FEA) method was used to solve the temperatures of the 3D structure. Body Corp's online tool AAVID Genie was used to verify the results and select the appropriate heatsink for each structure from their commercially available heatsinks, and then simulate it in COMSOL. The Joule heating generated by electric currents passing through each of the MOSFET modules were obtained from calculations made in PowerSim which acted as the heat sources for COMSOL. A stationary study was created for each model to study the steady state effects of the Joule heating on the temperature of each structure. The dimensions of the heatsink for the GaN model were made smaller to demonstrate the superiority of the Wide Bandgap (WBG) material in terms of heatsink requirements for similar steady state temperatures. Thermal stresses and physical deformation are beyond the scope of this paper.

6.2. Model Geometry

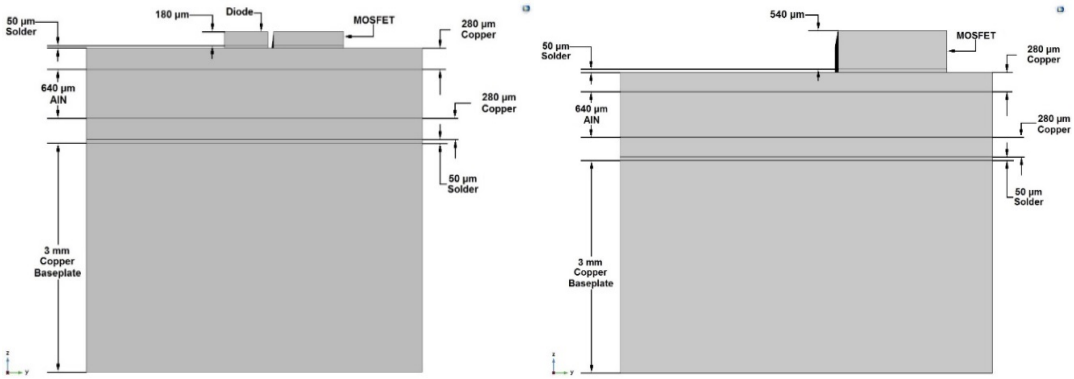
The internal structure the Si MOSFET module starts from the bottom to the top with a Copper (Cu) Baseplate, a solder layer, a Copper layer, an Aluminum Nitride (AlN) layer and a Copper layer. The module for GaN consists of all the layers as the Si module with the exception of the diode and

its corresponding solder layer. The dimensions of the MOSFETs for the GaN module were obtained from [26]. Figures 16–18 show the dimensioned 3D view, the yz-plane view and the xy-plane view of the MOSFET modules respectively. Figure 17 is scaled to make all the layers viewable.



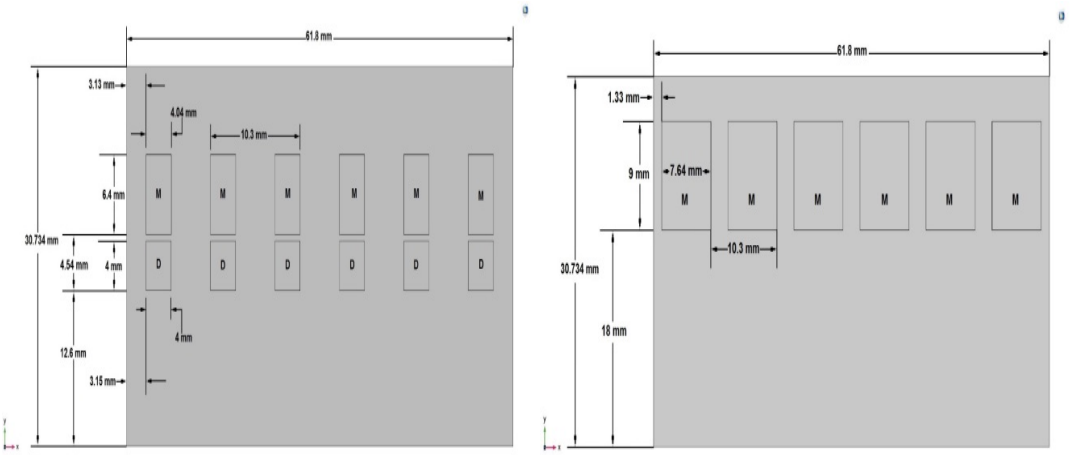
(**a**) (**b**)

Figure 16. 3D view of MOSFET modules: (**a**) for Si; (**b**) for GaN.



(**a**) (**b**)

Figure 17. yz-plane view of MOSFET modules: (**a**) for Si; (**b**) for GaN.



(**a**) (**b**)

Figure 18. xy-plane view of MOSFET modules: (**a**) for Si; (**b**) for GaN.

The final layer of each model consisted of an Aluminum (Al) heatsink which rested on top of the MOSFET and diode layers. The dimensions of the heatsinks were obtained from Boyd Corp's online tool AAVID Genie. These dimensions were based on real world heatsinks sold by Boyd Corp that would make the maximum temperatures of the module-heatsink combinations below 100 °C. Figures 19 and 20 show the heatsinks used for the Si and GaN modules respectively. Each heatsink consists of a solid Aluminum block of dimensions 141.8 mm × 104.3 mm × 6.6 mm. 16 aluminum fins of width 1.134 mm and separated by 6.8 mm were added on top of this block with heights of 33.5 mm and 10.89 mm for the Si and GaN models respectively. These height values were selected to obtain similar minimum temperatures for the two models.

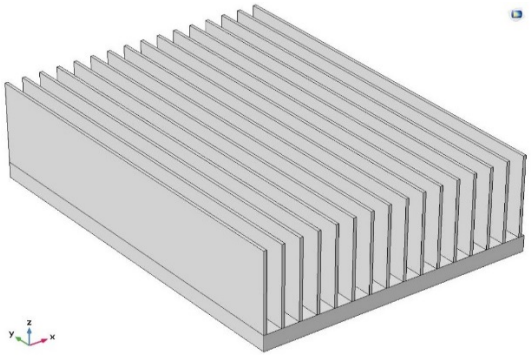


Figure 19. Heatsink for Si model.

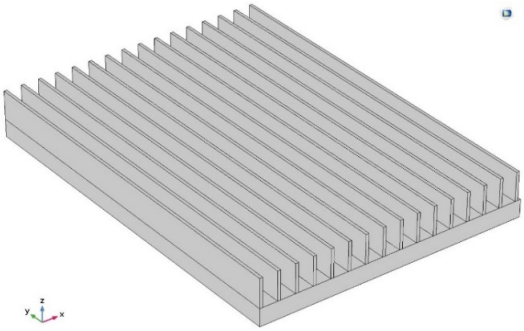


Figure 20. Heatsink for GaN model.

6.3. Material Properties

The physical material properties used for the models were the Density (ρ), the Heat capacity at constant pressure (Cp) and Thermal conductivity (k). Only these three properties were used for the simulations because heat transfer in solids was the only physics being studied. The materials were assumed to be isotropic with every property considered to be constant in all 3 directions. The properties for all materials simulated in the models except for the Solder were obtained from built-in libraries in COMSOL. SAC396 solder, an alloy of Tin, Silver and Copper, was chosen for the models and its properties were obtained from [33]. Table 6 shows all material properties that have been used in simulation.

Table 6. Thermal properties of materials used.

Property	Symbol	Unit	Cu	SAC396	AIN	Si	GaN	Al
Density	ρ	kg/m^3	8960	7400	3260	2329	6070	2700
Heat capacity at constant pressure	C_p	J/(kg K)	385	220	740	700	490	900
Thermal conductivity	k	W/(m K)	400	61.1	160	131	130	238

6.4. Heat Transfer Physics Modeling

The module of heat transfer in solids physics in COMSOL was used to simulate the thermal performance of each structure. PowerSim was used to calculate the heat losses for each MOSFET; these losses were used as heat sources for the simulations. For the Si model, these losses for the MOSFETs, going from left to right in Figure 16, were 19.9 W, 19.9 W, 19.9 W, 19.9 W, 21.3 W and 21.3 W while the losses for the GaN model in Figure 17 were 7.1 W, 7.1 W, 7.1 W, 7.1 W, 12.6 W and 13 W respectively. As the heatsinks dissipate thermal energy from the heat generated by the MOSFETs to the surrounding air, a convective heat flux boundary condition for all heatsink surfaces in contact with air was set up. The convective heat transfer coefficient was given a value of 10.45 W/m^2 K to simulate non-forced free flowing air. The initial temperature of the structures and surrounding air was set to room temperature i.e., 293.15 K or 20 °C. Using these inputs and boundary conditions, COMSOL solved the heat equation in solids to obtain the temperature profiles of each model.

6.5. Model Simulation and Results

Figures 21 and 22 show the temperature profile of the Si and GaN models with the heatsinks hidden. Figures 23 and 24 show the temperature profiles for the Si and GaN models with the heatsinks visible. The temperatures displayed on the legends are in °C.

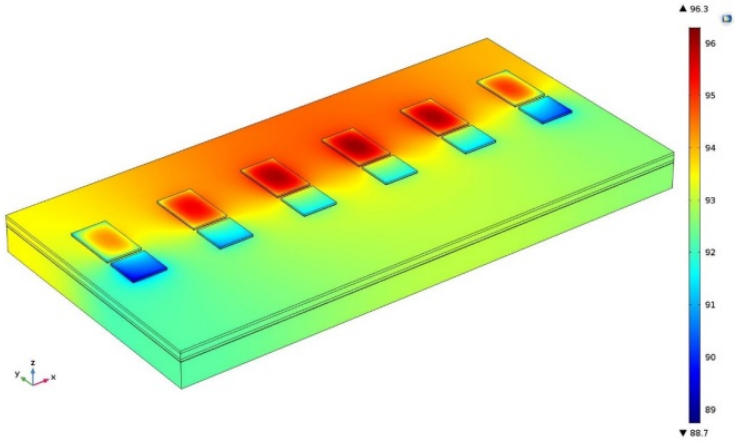


Figure 21. Temperature profile of Si model with heatsink not visible.

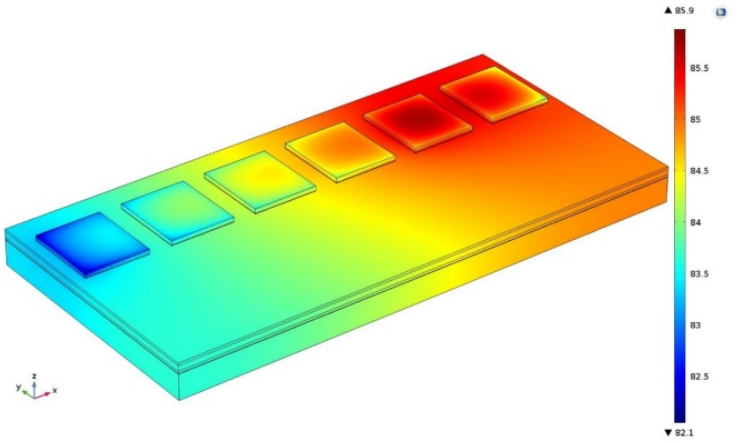


Figure 22. Temperature profile of GaN model with heatsink not visible.

The temperature profiles for the Si and GaN models with the heatsink not visible show that the highest of temperatures are concentrated around the MOSFETs that have the highest heat losses. As the heat losses for all Si MOSFETs are close to 20 W, the temperatures are fairly uniform throughout the Si

MOSFET module structure whereas for the GaN model the temperatures are higher at the right end near the MOSFETs with higher losses while the left end with lower losses has lower temperatures. The temperature range for the GaN model is within 4 °C, which is smaller than for Si. This is because the heat losses for the MOSFETs have the smallest range for the GaN model.

The temperature profiles for the two models with the heatsink visible also show similar distribution of temperatures. The Si and GaN models have higher temperatures on the heatsink fairly uniform around all the MOSFETs, but the range of temperatures for the heatsinks are much lower in the GaN model than the Si model.

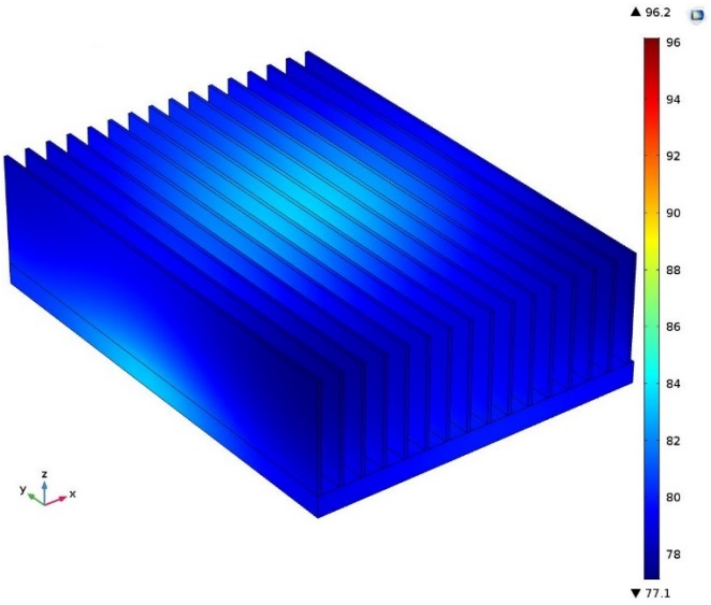


Figure 23. Temperature profile of Si model with heatsink visible.

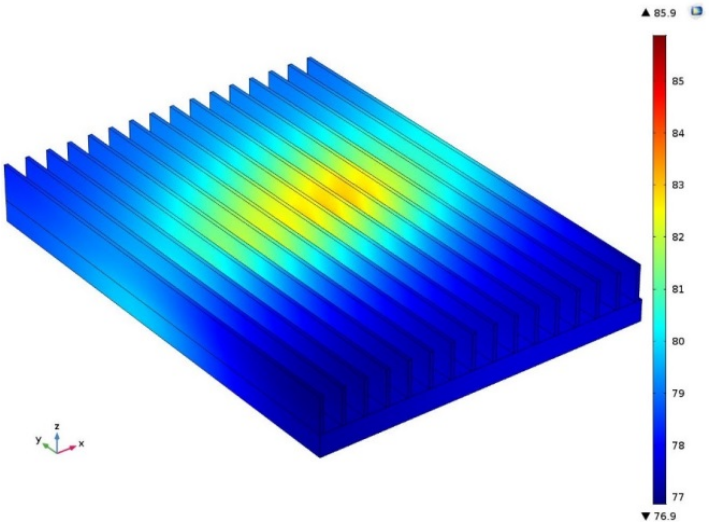


Figure 24. Temperature profile of GaN model with heatsink visible.

The maximum temperatures for the Si and GaN models were found to be 96.36 °C and 85.91 °C respectively. The minimum temperatures were 77.14 °C and 76.87 °C for the Si and GaN models respectively. The 3D model for Si MOSFETs had a volume of 183.8 cm^3 and surface area of 1861 cm^2 for the heatsink while the GaN model had a volume of 125.6 cm^3 and surface area of 826.3 cm^2. From the simulations for the two models, it is clear that the WBG GaN MOSFET module requires a smaller heatsink (by a factor of 0.444 for GaN in terms of surface area) for similar maximum temperatures. Thus, using GaN HEMT will consequently reduce the overall system volume. The thermal modelling

clearly demonstrates that the GaN module is more efficient than the Si module in terms of heatsink size and overall heat dissipation.

7. Conclusions

In this paper, an investigation of the benefits of using GaN HEMTs in transformer-less PV inverter is presented. The conduction losses, switching losses, and thermal analysis at different output power and switching frequencies verified the benefits of replacing Si MOSFET with GaN HEMTs. The use of GaN HEMTs significantly reduced the overall semiconductor power losses of the proposed inverter by 60% when compared to Si MOSFETS under the same operation conditions (load and switching frequency). This loss reduction will increase the overall efficiency of the system by more than 3%. Moreover, GaN HEMT-based inverter operating at the same switching frequency as Si MOSFET-based inverter can provide more than 60% increase in power rating while maintaining the same power losses. Furthermore, this loss reduction when operating at the same switching frequency, allows a reduction of more than 30% in heat sink volume, which will consequently reduce the overall system volume and cost. Finally, the superior switching characteristics of GaN HEMTs allow the switching frequency to be increased to more than 10 times the switching frequency of the Si MOSFETs. This increase will consequently, reduce the passive components weight and volume, which, eventually, will reduce the overall inverter cost.

Author Contributions: Khaled Alatawi and Fahad Almasoudi conceived and organized this work. Khaled Alatawi performed the energy and power simulations in the software PowerSim and acquired and analyzed the data. Mahesh Manandhar performed thermal analysis of the GaN MOSFET module in the FEA software COMSOL. Mohammad Matin provides the technical feedback and revised the manuscript. The manuscript was written by Khaled Alatawi with the thermal analysis section being written by Mahesh Manandhar. All authors proofread the manuscript.

Conflicts of Interest: The authors declare no conflict of interest.

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