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Series Active Filter Design Based on Asymmetric Hybrid Modular Multilevel Converter for Traction System

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Abstract: This paper presents a comparative analysis of a new topology based on an asymmetric hybrid modular multilevel converter (AHMMC) with recently proposed multilevel converter topologies. The analysis is based on various parameters for medium voltage-high power electric traction system. Among recently proposed topologies, few converters have been analysed through simulation results. In addition, the study investigates AHMMC converter which is a cascade arrangement of H-bridge with five-level cascaded converter module (FCCM) in more detail. The key features of the proposed AHMMC includes: reduced switch losses by minimizing the switching frequency as well as the components count, and improved power factor with minimum harmonic distortion. Extensive simulation results and low voltage laboratory prototype validates the working principle of the proposed converter topology. Furthermore, the paper concludes with the comparison factors evaluation of the discussed converter topologies for medium voltage traction applications.

Keywords: hybrid converter; multi-level converter (MLC); series active filter; power factor correction (PFC)

1. Introduction

An electrified ac railway system, being an energy-efficient and governmentally-friendly medium of mass transportation, achieved great demand in many countries. However, to maximize the traffic, it still requires developing highly efficient, reliable, and compact traction systems with reduced cost, minimum time delay and less vibrations to assure passengers comfort [1]. The efficiency of railway traction systems can be improved with a regenerative braking system which enables transforming the kinetic energy of the rail vehicle in slowing down the speed into electrical power. Using a bidirectional converter, the electric power generated due to the regenerative braking system can be harvested for reuse [2].

A high efficiency and low production cost is required mostly by industrial processes, which can be achieved by increasing the power rating of electrical components/equipment with the reduced installation size. The power can be increased either by developing semiconductor devices with a capability to withstand high voltage or by introducing multilevel converters which will allow to connect the converter system directly to medium-voltage line. Recently, continuous development in power semiconductors devices i.e., high-voltage insulated-gate bipolar transistors (IGBTs) and

integrated-gate commutated thyristors (IGCTs) and their use in self-commutated converters increases the nominal voltage and power ratings of the converter system.

Lower medium voltage high power railway traction system multi-level converters (MLC) have significant advantages over classical two-level and three-level converters due to their lower current harmonics distortion, less electromagnetic interference, increased output voltage level, and high power density. Furthermore, due to the simple layout of classical two-level converters, connecting single power semiconductor switch to medium grid voltages directly is not appropriate [3,4]. The key conventional MLC topologies i.e., neutral point clamped (NPC), flying capacitors (FC), and the cascaded H-bridge (CHB) have been reported in [4–8]. The MLC contains numerous power semiconductor switches and a dc-link capacitor which are arranged according to the required output voltage level. However, increasing the number of components accounts for attaining a high voltage level to increase the control complexity, which will affect the efficiency and reliability of the converter [6]. The requirement for MLC includes the dc-link voltage value at reference voltage level, unity power factor on the ac side and low harmonics distortion in the injected current to ac grid [9]. Therefore, an appropriate control scheme is required to track the current signal and maintain the dc-link capacitor voltages of MLC at their respective desired reference. A pulse width modulation (PWM) technique which is used by various MLC drive systems has been investigated in [10,11].

Recently, arrangement of different conventional MLC topologies known as hybrid multilevel converters has been introduced in [12,13]. In medium and high voltage range application, numerous multilevel topologies share the market for industrial applications. Hybrid MLC topologies have been a focus of interest due to substantial advantages which include, a redundant converter design, wide operating range, minimum line harmonics, and improved power factor. Some of these arrangements exist in the literature, such as NPC-H module [14], FC-H module [15], NPC-FC module [16] and H-cascaded module [17]. Furthermore, unequal dc link voltages are used which minimizes the redundant switching states and increases the output voltage level of the converter. Such converters are known as asymmetric converters in the literature [17,18].

The non-linearity of the converter injects harmonic currents in the ac grid, which adversely affects stability and the power quality of the ac grid [19]. Various techniques are available to mitigate high harmonics; a modulation scheme based on selected harmonic elimination pulse width modulation is studied in [12]. Various passive filters are introduced in [18,20,21] to overcome the harmonics issues in converters, but due to its system parameters, the performance is limited and may cause a resonance problem [22]. A compensator based on an electronics converter known as series active power filter (APF) converter is studied in the literature [23–25] to tackle the limit imposed by the high harmonics. Moreover, a converter based compensator in the existing research needs improvement in a supply system for the electrified traction system.

This paper presents a comparative study of the recently proposed MLC converter for the medium voltage-high power traction system which is examined through simulation results. Among all converters, a new topology based on an asymmetric hybrid modular multilevel converter (AHMMC), which is a series arrangement of a classical H-bridge and FCCM voltage source PWM converters, is investigated in more detail. The design of AHMMC topology, its corrective current and its voltage control methods are demonstrated. The overall system's controllability, total harmonic distortion (voltage and current), power factor and voltage stability on the dc-link capacitors is analysed through extensive simulation results. The proposed topology is practically validated through low-power laboratory prototype.

The paper is organized as follows. Section 2 includes a comparative analysis of five-level converter topologies and their output results are examined. Section 3 first investigates the proposed converter model, afterwards, its modulation strategy and control scheme are discussed. The simulation and experimental results of the proposed converter are presented and discussed in Section 4. An evaluation of comparison factors of the discussed converter topologies are examined in Section 5. Finally, the study is concluded in Section 6.

2. Comparative Analysis of 5-Level Converter Topologies

A comparative analysis of a few MLC converter arrangements i.e., NPC, hybrid NPC with H-bridge module, CHB based NPC, and HNPC with a cascaded module for lower-medium voltage application are discussed in this section.

2.1. NPC Converter

NPC converters are most widely used in industrial application from the last two decades among the other high power converters [26,27] in the range of 2.3 kV, 4.16 kV and 6 KV applications [28]. Figure 1 shows a NPC voltage source converter (VSC), is the most commonly used topology for self-commutated medium voltage converters (MVCs). The distinct features of NPC VSC ensures a better output voltage quality compared to the conventional two-level converter.

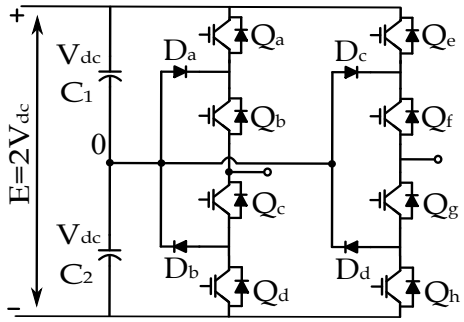

Figure 1. Five-level NPC converter topology.

The NPC converter circuit shown in Figure 1, contains eight power semiconductor switches, four clamping diodes $D_{(a-d)}$, a dc-bus voltage of E = 2Vdc and two dc-link capacitors, each of the dc-link capacitor is charged to half of the dc-bus voltage i.e., Vca = Vcb = $\frac{1}{2}$E. The output voltage of the NPC converter is set to five level $\pm 2V_{dc}$, $\pm V_{dc}$, and 0. The modulation of converter switches can be achieved by three methods: (1) Carrier Based Pulse Width Modulation (CBPWM); (2) Selective Harmonic Elimination (SHE); and (3) Space Vector Modulation (SVM). In this study a CBPWM based modulation is used for a 3L-NPC, for which the maximum current is achieved at the maximum modulation index (m = 1). Based on topological design, consider that the NPC converter half bridge is under voltage stress equal to half of the dc-bus voltage, whereas the half bridge of the H-bridge converter is stressed equal to dc-bus voltages. To correlate the system voltage and required semiconductor voltage in the three-level NPC converter, a 3.3 KV ratings devices are equipped in 2.3 kV converter without series connection of devices. Using 3L-NPC VSC, an output voltage of up to 4.16 kV can be achieved without any series connection of devices [29–31]. Currently, 3L-NPC converters are available in market with a variety of devices. Siemens^{TM}, a European manufacturer, utilizes 3.3 and 6.5 KV IGBT modules devices where higher voltage levels are attained through series connection of semiconductor devices, to cover a range of 2.3 to 7.2 kV converters [32–34]. ABB^{TM} use 4.5 kV IGCTs [35] to offer 3.3 KV converters and Converteam^{TM} recently launched a 3.3 KV NPC product using the press-pack 4.5 kV IGBT technology [36].

2.2. Hybrid NPC with H-Bridge

A hybrid modular converter based on the cascaded arrangement of NPC five level cell (having two three-level NPC leg) with a three-level H-bridge cell and H-NPC module with a H-bridge as shown in Figure 2, are investigated in [37–39] for different voltage ratios of the dc-link among the two power cells. In the study, a converter cell which gives a fundamental component support operates at low frequency, whereas a converter cell as a series active filter operates at high frequency for high harmonics minimization and coupling inductor size reduction.

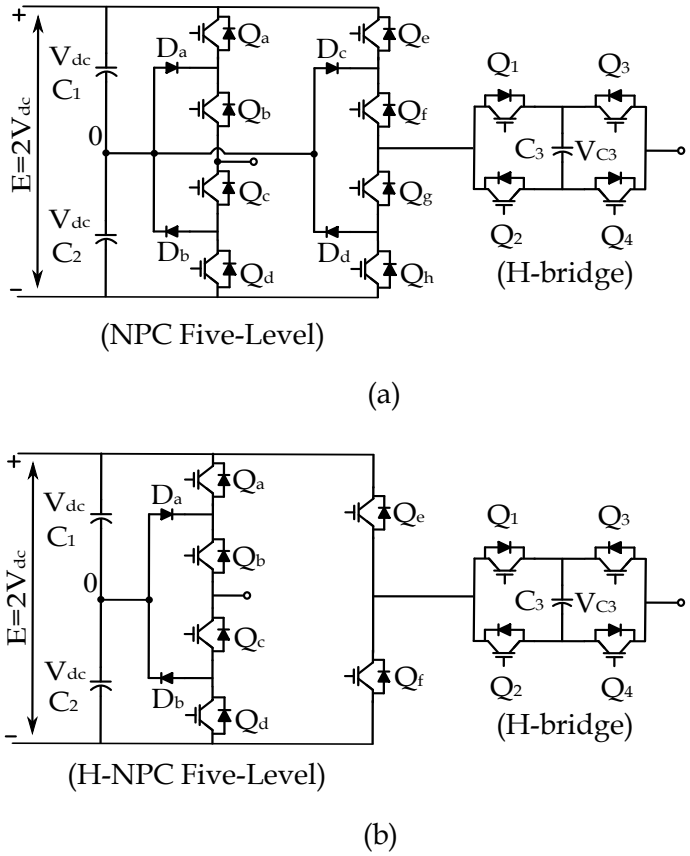

Figure 2. Five level NPC converter with H-bridge (**a**) NPC with H-bridge module, and (**b**) H-NPC with H-bridge module.

The power losses across the semiconductor switches are calculated and grouped by the power cell of each converter. The total power loss(P_t) includes, switching loss (P_{sw}) and conduction loss (P_c). The conduction losses of the H-NPC cell are less due to the minimum number of power semiconductor devices. The switching losses of the harmonic compensation converter will be higher because of the high voltage stress and high average switching frequency.

2.3. CHB Based NPC Converter

As discussed above, the hybrid NPC with H-bridge configuration will cause a high power loss in the voltage stressed power semiconductor switches because of the high average switching frequency. To overcome the said issues, the dc-link voltage is equally distributed by replacing an H-bridge cell with a five-level cascaded H-bridge (CHB) as shown in Figure 3. However, the topology with a five level CHB arrangement requires an increased number of power semiconductor switches which will cause high conduction losses and require a greater number of drive circuits.

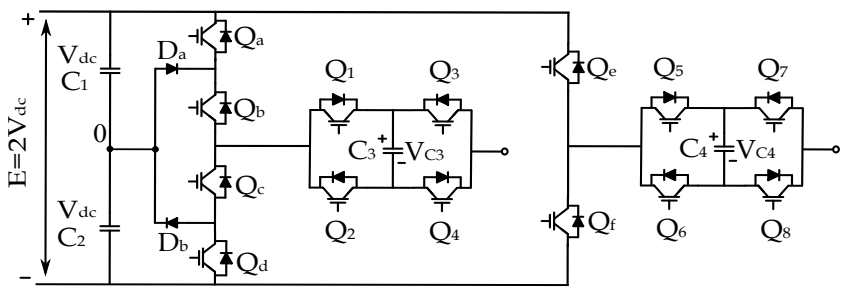

Figure 3. CHB based converter topology.

2.4. H-NPC with Cascaded Converter Module

Figure 4 depicts an arrangement for H-NPC with a cascaded module that is constructed in this study for lower medium voltage application. The topology has the benefit of a lower number of power semiconductor devices in comparison with the CHB based converter topology discussed in Section 2.3. The HNPC with cascaded module will minimise the total switch loss and number of drive circuits.

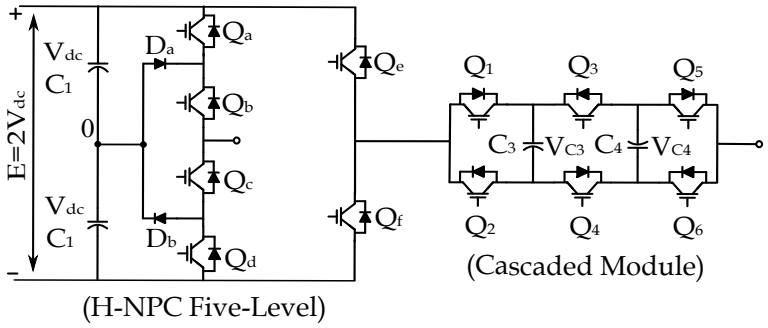

Figure 4. Five-level H-NPC with cascaded converter module.

2.5. Topological Analysis Based on Simulation Results

To verify the converter system performance, a few of these arrangements, including the NPC module, hybrid H-NPC with H-bridge module and H-NPC with cascaded converter module are simulated in Matlab/Simulink environment. A five-level and seven-level converter output voltage and the inductor current is obtained. The output voltage and inductor current of the converters are further analysed by fast Fourier transform (FFT). The simulation parameters of the NPC Converter are listed in Table 1.

Table 1. Simulation Parameters of NPC Converter.

Parameters	Value
Grid Voltage	1750 V (rms)
DC bus Voltage	3000 V
DC link Capacitor C_1, C_2	1500 V
Converter Current	70 Amp (rms)
L	0.6 mH
Modulation Depth	1
$Freq_{pwm}$	2 kHz

The simulation results of an NPC converter are shown in Figure 5. In Figure 5a,b the output voltage with its harmonics spectrum is shown using conventional PWM control technique with a modulation index m = 1. Figure 5c,d shows that the converter current is in phase with the grid voltage, ensuring the rectifier operation mode of the converter.

The simulation parameters of seven-level H-NPC with H-bridge module and H-NPC with cascaded converter module are presented in Table 2. By operating H-NPC with H-bridge module converter at maximum modulation index m = 1.06, a maximum seven-level of output voltage is achieved as shown in Figure 6a. The figure depicts the output voltage of the H-NPC, H-bridge and overall converter, whereas Figure 6b shows its respective harmonics spectrum by using conventional carrier based PWM control technique. Figure 7 shows H-NPC converter with H-bridge module operating in rectifier mode. It can be seen from Figure 7a that the converter current has the same phase with the grid voltage shown in Figure 7b. Figure 8 shows the simulation results of a 7-L HNPC with a cascaded module. Figure 8a depicts the output voltage of the H-NPC converter, cascaded module and overall converter, whereas Figure 8b shows its respective harmonics spectrum by using conventional carrier based PWM control technique with a modulation index m = 1.06. Figure 9 shows the converter

operating in rectifier mode. It can be seen from Figure 9a that the converter current has the same phase with the grid voltage shown in Figure 9b.

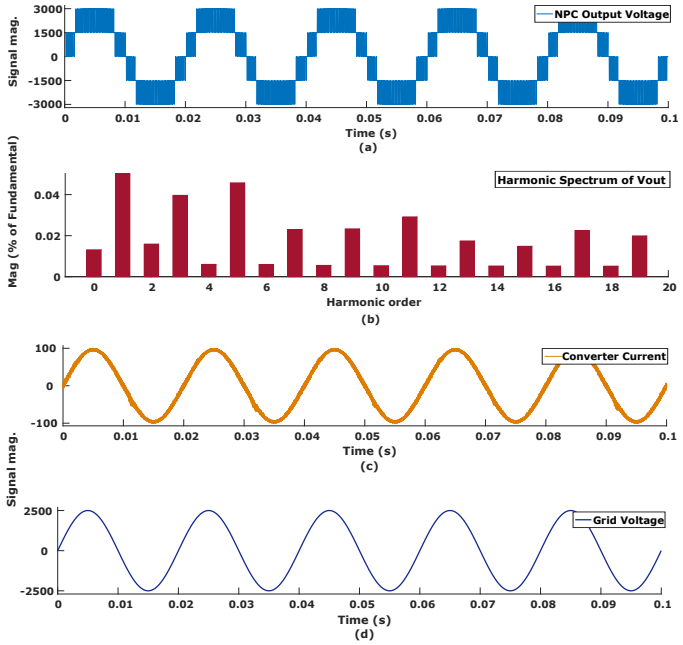

Figure 5. 5-L NPC converter topology (**a**) output voltage, (**b**) harmonic spectrum of output voltage, (**c**) converter current, and (**d**) grid voltage.

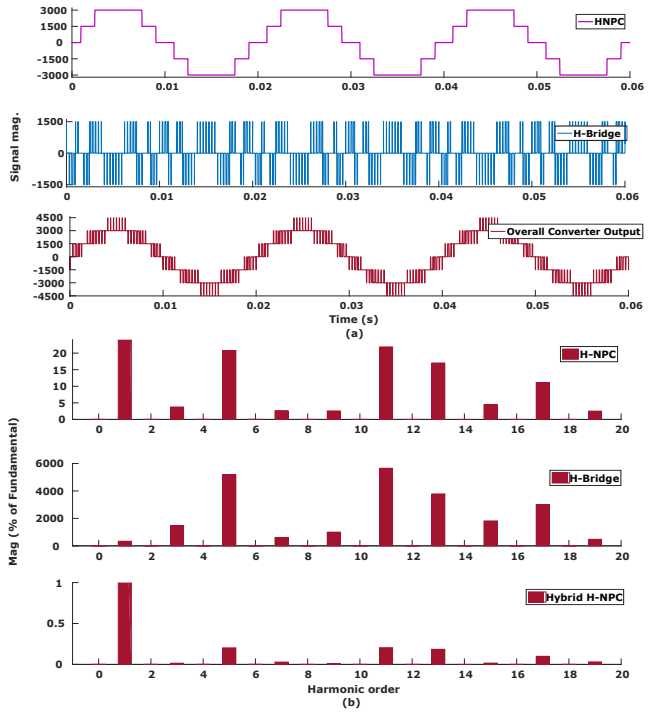

Figure 6. 7-L hybrid H-NPC with H-bridge converter topology (**a**) output voltage, and (**b**) harmonic spectrum of output voltage.

Table 2. Simulation parameters of Hybrid H-NPC converter.

Parameters	Value
Grid Voltage	1750 V (rms)
DC bus Voltage	3000 V
DC link Capacitor C_1, C_2, C_3, C_4	1500 V
Converter Current	70 Amp (rms)
L	0.6 mH
Modulation Depth	1.06
H-NPC converter $freq_{pwm}$	350 Hz
H-Bridge cell $freq_{pwm}$	2 kHz
Cascaded module converter $freq_{pwm}$	2 kHz

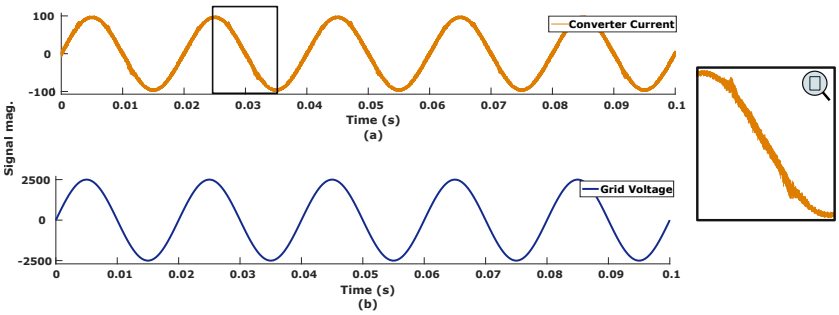

Figure 7. Converter operating in rectifier mode (**a**) converter current, and (**b**) grid voltage.

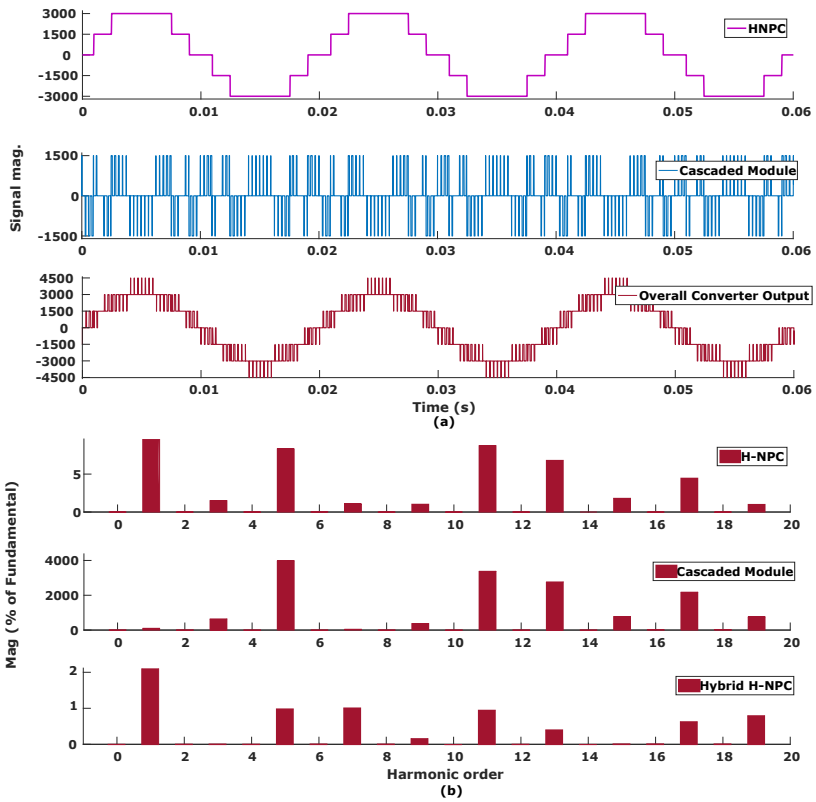

Figure 8. 7-L hybrid H-NPC with a cascaded converter topology (**a**) output voltage, and (**b**) harmonic spectrum of output voltage.

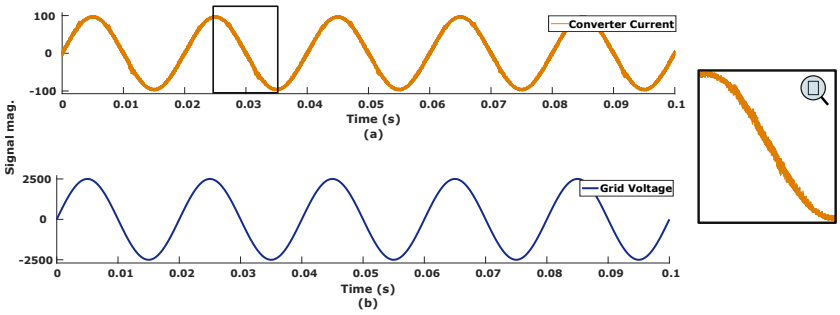

Figure 9. Converter operating in rectifier mode (**a**) converter current, and (**b**) grid voltage.

3. Proposed AHMMC Converter

3.1. Structure and Working Principle

Figure 10 shows the proposed AHMMC topology. The basic circuit configuration contains an FCCM in series with an H-bridge cell. An H-bridge converter contains four power semiconductor switches Q_{a-d}, a dc-bus voltage of $E = 2V_{dc}$, and a single dc-link capacitors C_a charged to the dc-bus voltage. The output voltage of the H-bridge converter $(V_{(AB)})$ is set to three level $\pm V_{dc}$, and 0. The FCCM which is the origin of the AHMMC topology contains six power semiconductor switches Q_{1-6} and two dc-link capacitors V_{c1} and V_{c2}, each of the dc-link is charged to $1/2\,E$ of the dc-bus voltage. The output voltage of FCCM $(V_{(BC)})$ is synthesized which generates 5-level that are $\pm 2V_{dc}, \pm V_{dc}$, and 0. The output voltage of the proposed AHHMC converter can be achieved by Equation (1):

$$V_{(AHMMC)} = V_{(AB)} + V_{(BC)} \tag{1}$$

The mathematical model of the proposed AHMMC grid tied converter can be expressed by the following set of Equations (2)–(4):

$$\frac{di_s}{dt} = \frac{1}{L}(S_x V_{c1} + S_y V_{c2} \mp S_z 2V_{dc} \pm V_g) \tag{2}$$

$$\frac{dV_{c1}}{dt} = \frac{S_x i}{C_1} \tag{3}$$

$$\frac{dV_{c2}}{dt} = \frac{S_y i}{C_2} \tag{4}$$

where $V_g = Esin(wt)$ is a grid voltage, S_x, S_y and S_z are the switching functions of the AHMMC which can be expressed by the following Equations (5)–(7):

$$S_x = Q_1 Q_4 - Q_2 Q_3 \tag{5}$$

$$S_y = Q_4 Q_5 - Q_3 Q_6 \tag{6}$$

$$S_z = Q_a Q_d - Q_b Q_c \tag{7}$$

The eight distinct operating modes of FCCM are achieved by three complementary pairs of the power switches (Q_2, Q_4, Q_6 are the complement pair of Q_1, Q_3, Q_5, respectively) are listed in Table 3. Figure 11 depicts an output of seven-level $\pm 3V_{dc}, \pm 2V_{dc}, \pm V_{dc}$, and 0 which is achieved by operating the converter modules with the combination of switching states. Table 4 summarises the seven-level output voltage of the AHMMC converter.

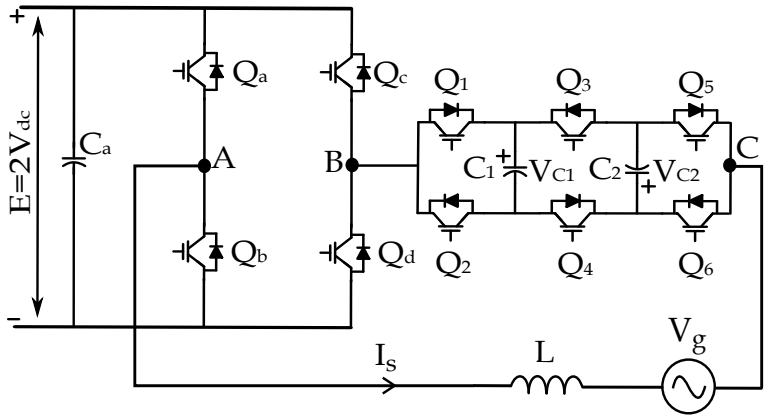

Figure 10. Proposed AHMMC converter topology.

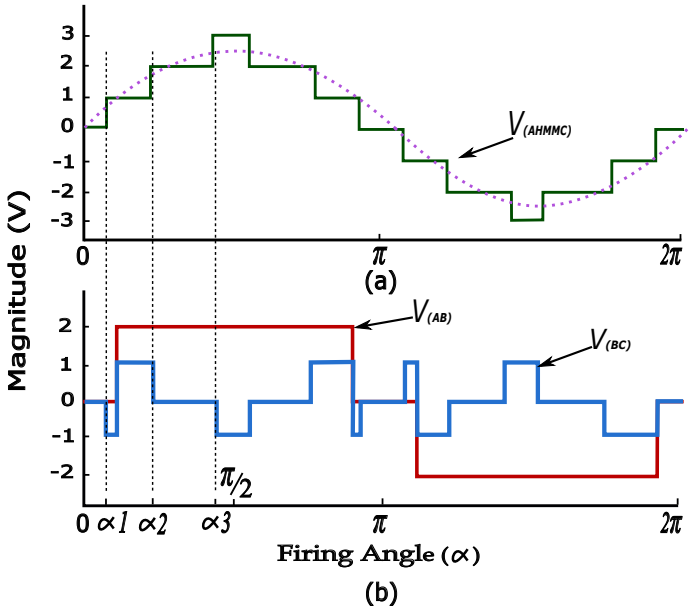

Figure 11. AHMMC operation mode (**a**) AHMM output voltage, and (**b**) H-bridge output voltage $(V_{(AB)})$ and FCCM output voltage $(V_{(BC)})$.

Table 3. Switching modes of FCCM module.

Modes	Switching States			Capacitor	Capacitor	FCCM Output Voltage
-	Q_1	Q_4	Q_5	C_1	C_2	$V_{(BC)}$
				Table (a) when $i_s > 0$		
1	1	1	1	discharge	discharge	$2V_{dc}$
2	1	1	0	discharge	by pass	V_{dc}
3	0	1	0	by pass	by pass	0
4	1	0	0	by pass	charge	$-V_{dc}$
5	0	0	0	charge	charge	$-2V_{dc}$
				Table (b) when $i_s > 0$		
1	1	1	1	discharge	discharge	$2V_{dc}$
2	0	1	1	by pass	discharge	V_{dc}
3	1	0	1	by pass	by pass	0
4	0	0	1	charge	by pass	$-V_{dc}$
5	0	0	0	charge	charge	$-2V_{dc}$

Table 4. AHMMC Converter Output Voltage.

Angle	$V_{(AB)}$	$V_{(BC)}$	$V_{(AHMMC)} = (V_{(AB)}) + (-V_{(BC)})$
$0 \leq \theta \leq \alpha_1$	0	0	0
$\alpha_1 \leq \theta \leq \alpha_2$	0	$-V_{dc}$	V_{dc}
$\alpha_1 \leq \theta \leq \alpha_2$	$2V_{dc}$	V_{dc}	V_{dc}
$\alpha_2 \leq \theta \leq \alpha_3$	$2V_{dc}$	0	$2V_{dc}$
$\alpha_3 \leq \theta \leq \pi$	$2V_{dc}$	$-V_{dc}$	$3V_{dc}$

3.2. Modulation Technique

A phase opposition disposition (POD) multi-carriers modulation strategy is implemented as a PWM technique for the proposed converter. In order to minimize the switching loss, the converter switches are categorised in two sets (i) high frequency switching of low voltage switches; (ii) low frequency switching of high voltage switches. Design of the heat dissipation of the system and switch type are the parameter for optimal selection of high frequency switches. In the proposed AHMMC converter, the switches Q_a and Q_c are under high voltage stress and therefore, they are operated with the fundamental switching frequency to minimise the switching loss. The voltage stress on the switches of the FCCM converter is not symmetric. Within the FCCM, the middle leg switches Q_3 and Q_4 are under high voltage stress and therefore, for the design consideration the PWM frequency of these switches is restricted below 1 kHz which will reduce the switching loss, whereas the PWM frequency for the outer leg switches Q_2 and Q_6 are set to 2 kHz (1 kHz effective switching frequency) due to the permissible operating range of high voltage devices up-to 2 kV. Moreover, the modulation scheme studied in this work has the benefit of a wide modulation index range. Figure 12 shows the graph of modulation index versus dc-link voltage value for series active filter (FCCM) at various operating angle.

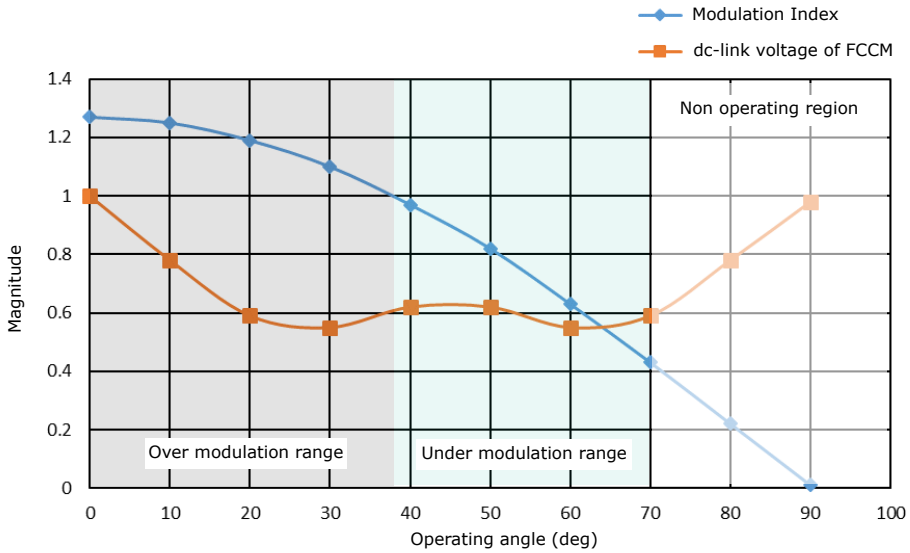

Figure 12. Modulation index versus dc-link voltage of FCCM.

3.2.1. Over Modulation Range (1∼1.27)

In the proposed AHMMC converter, the H-bridge cell will provide a fundamental support whereas the FCCM module will cancel harmonics produced by the H-bridge cell. The overall output voltage level of the proposed AHMMC converter depends on the modulation index (m) which is expressed by Equation (8). Where θ is the initial phase angle of the h-bridge cell which is calculated using Equation (9).

$$m = \frac{4}{\pi} cos(\theta) \tag{8}$$

$$\theta = arccos \frac{\pi}{4} \frac{V_g}{V_{dc}} \tag{9}$$

At θ = 0, a 27% maximum modulation index is achieved which results in the higher output voltage of the proposed converter. Figure 12 shows the over modulation range along with the dc-link voltage required for harmonic compensation. When the theta lies between $(0 \leq \theta < 38)$ degree, maximum seven-level output voltage is achieved which will lower the current value for the same power rating of the converter.

3.2.2. Switch Stress and Modulation Range (0.4∼1)

Operating the proposed converter in the modulation range of m = 0.4∼1, a five level converter output voltage is achieved with approximately half of the dc-bus voltage required for series active filter (FCCM). This will lower the voltage stress on the semiconductor switches. The voltage stress on the middle leg of the FCCM will be 0.6 E, whereas, voltage stresses on the upper legs will be 0.3E . Therefore, the switching frequency can be varied according to the system design.

3.3. Switch Losses

The switch losses were divided into the conduction and switching power losses. The total power switch losses P_T are grouped by power converters. The proposed AHMMC topology studied in this paper consists of 10 power switches with anti-parallel diodes. The conduction loss of the switch depends on the power conduction through the switch due to direction of the current. The calculation of total conduction losses P_{cd} at any instant across the power switch (p_{sw}) and diode (d) can be given as Equations (10)–(12):

$$P_{c\_m(p_{sw})} = \frac{1}{2\pi} \int_0^{2\pi} \left[(m_{p_{sw}} \times v_{p_{sw}}) i_s \cdot Q_l \right] d(\omega t) \tag{10}$$

$$P_{c\_m(d)} = \frac{1}{2\pi} \int_0^{2\pi} \left[(m_d \times v_d) i_s \cdot Q_l \right] d(\omega t) \tag{11}$$

$$P_{cd} = P_{c\_m(p_{sw})} + P_{c\_m(d)} \tag{12}$$

where $m_{p_{sw}}$ and m_d are switch and diode count during conducting period, $v_{p_{sw}}$ and v_d are voltage drops of the power switch and diode in conduction state, respectively, i_s is the conduction current of the power switch device, and Q_l is the switching command of the power switch.

The switching losses of active switch can be determined every ON and OFF state during a reference period. The overall switching losses can be calculated by Equations (13) and (14):

$$P_{sw} = P_{sw\_on} + P_{sw\_off} \tag{13}$$

$$= \sum_{j=1}^{2n+2} \left[\frac{1}{6} v_{b(j)} \cdot i \cdot (t_{on} + t_{off}) f_j \right] \tag{14}$$

where, v_b, i and f_j is the blocking voltage, a conduction current, and the switching frequency of the active switch, respectively.

The total power switch losses across the converter can be computed as:

$$P_T = P_{cd} + P_{sw} \tag{15}$$

3.4. Control Scheme

For a stable operation of the proposed converter, corrective current and voltage control techniques shown in Figure 13 are implemented to track the reference current and reference voltage to ensure the unity power factor and balanced dc-link voltage, respectively. An inner current control loop is implemented at the FCCM module; since the operating frequency of this converter is high it will respond quickly to any change.

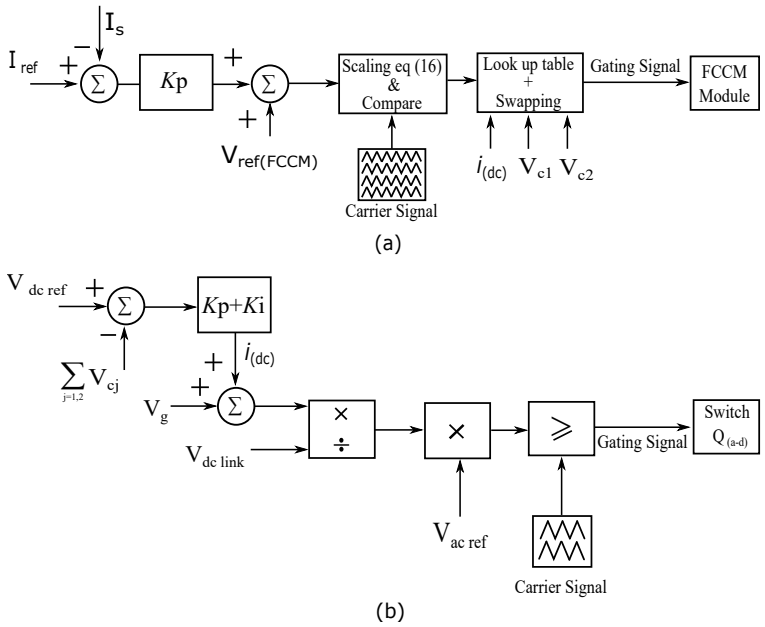

Figure 13. Corrective control scheme (**a**) current control loop, and (**b**) voltage control loop.

Figure 13a, shows a current control loop, in which an error signal is achieved by comparison of measured current I_s and I_{ref} which is further compensated by a proportional gain K_p and then added in the modulating signal for the FCCM converter. The dc link voltage variation impact in the current is minimized through dc voltage feed forward loop control by adjusting the PWM accordingly as described in Equation (16):

$$d = \left(p_1 \frac{|V_{out}|}{Vc_1} + p_2 \frac{|V_{out}|}{Vc_2} + p_3 \frac{|V_{out}| - V_{c1}}{Vc_2} + p_4 \frac{|V_{out}| - V_{c2}}{Vc_1}\right) \times Sign(V_{out}) \quad (16)$$

where d and $p_{(1-4)}$ is the duty cycle and PWM output conditions for FCCM, respectively. Table 5 presents PWM output conditions, whereas the direction of PWM output is determined by $Sign(V_{out})$ which is expressed by Equation (17):

$$Sign(V_{out}) = \begin{cases} 1, if\ V_{out} \geq 0 \\ -1, if\ V_{out} < 0 \end{cases} \quad (17)$$

Figure 13b shows the voltage control loop implemented for the proposed converter. In order to attain the desired output voltage level of the converter, The PWM allows to conduct through one node of the capacitor, which leads to the unbalancing of the capacitor V_{c1} and V_{c2}. Moreover, some of the power dissipates across the switches of the FCCM module which is fed by dc-link capacitors; therefore, a voltage control is needed to maintain balanced voltage on the dc-link. The voltage control loop is categorised into two parts (i) common mode voltage control (ii) voltage balancing among the capacitors. The common mode voltage is controlled by modifying the operating angle of the fundamental component of the H-bridge converter. For a stable operation of the converter, the difference among the dc-link capacitor voltages needs to be balanced, which is achieved by the

swapping technique, using the redundant switching states given in Table 3. It is presented in Table 3 that the voltage level $\pm V$ and 0 can be achieved in multiple ways with their respective states of charging and discharging of capacitor. The charge swapping using redundant switching states is based on the following set of rules.

- When $(i_{(s)} \times V_{ref}) < 0$, if $V_{C1} < V_{C2}$, then Table 3b will be selected.
- When $(i_{(s)} \times V_{ref}) > 0$, if $V_{C1} > V_{C2}$, then Table 3a will be selected.

where $i_{(dc)}$ is a direction of the dc reference current. Using the above relation of selecting tables, the balancing of capacitor voltage is achieved.

Table 5. PWM operating conditions.

Operating Condition	p_1	p_2	p_3	p_4
V_{c1} is a lower capacitor				
$\mid V_{out} \mid \leq V_{c1}$	1	0	0	0
$V_{c1} < \mid V_{out} \mid < (V_{c1} + V_{c2})$	0	0	1	0
V_{c2} is a lower capacitor				
$\mid V_{out} \mid \leq V_{c2}$	0	1	0	0
$V_{c2} < \mid V_{out} \mid < (V_{c1} + V_{c2})$	0	0	0	1

4. Simulation and Experimental Results

The AHMMC converter is simulated in MATLAB/Simulink environment to demonstrate the system's effectiveness, and performance of the modulation and control scheme. The AHMMC converter is designed for lower medium voltage application, hence efficiency greater then 97% is expected. However, an experimental validation is performed at low voltage laboratory prototype in which the proposed converter efficiency is determined by conduction losses of the semiconductor switches, which is not a very good indicator of real power losses appearing on the system, operating at a voltage range greater than 1 KV. To verify the system results, simulation results are scaled accordingly to a low voltage laboratory prototype using the system's parameters presented in Table 6, which are the same for both simulation and experimental models. The selection of all component values has been done by extensive simulations. The criteria for capacitors selection are based on the voltage ripple and stability consideration of a converter i.e., the capacitor capacity should be high enough to withstand imbalance to a couple of cycles. Through simulation analysis, approximately 2% capacitor ripple is designed, whereas the inductor L value is selected for a current ripple of 0.5% (peak to peak) under full rated current.

Table 6. System parameters of AHMMC.

Parameter	Value
Inductance	0.6 mH
DC-link Capacitor	20 µF
FCCM Switching Frequency	2 kHz
Capacitor Voltage	50 V_{dc}
Grid Voltage	110 (rms)
Current I_s	14 A (rms)
DC-bus Voltage	100 V

Figure 14 depicts the simulation and practical results of the AHMMC converter output voltage at m = 1.26. The three angles per quarter cycle operation gives an output of seven-level. Figure 14a shows simulation results, whereas Figure 14b shows experimental results of the stable converter operation because of balanced capacitor voltages. An active power is transferred by compensating the harmonics produced by H-bridge through series active filter (FCCM).

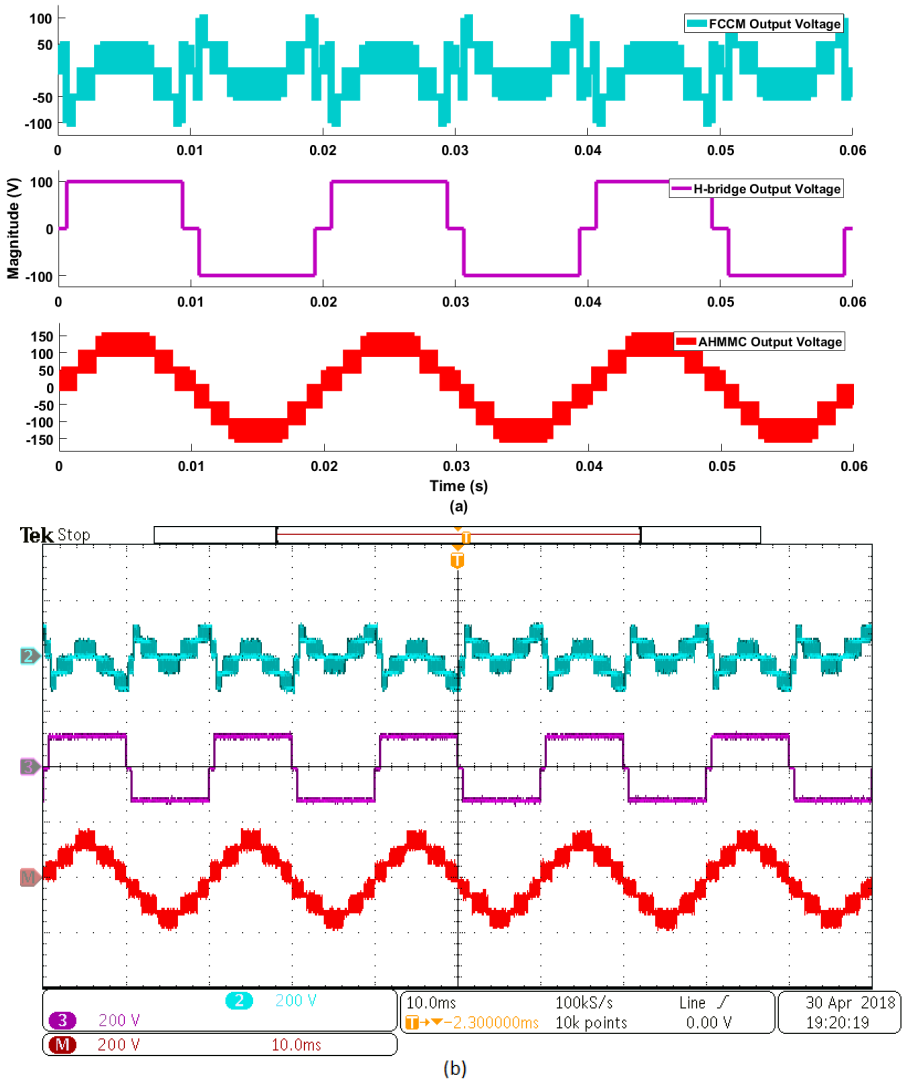

Figure 14. AHMMC converter output at m = 1.26, (**a**) simulation validation, and (**b**) experimental validation, traces channels 2 and 3 (200 V/div).

Figure 15 depicts the simulation and practical results of the AHMMC converter output voltage at m = 0.89. The two angles per quarter cycle operation gives an output of five-level. Figure 15a shows simulation results, whereas Figure 15b shows experimental results of the stable converter operation due to the balanced dc-link capacitor voltages. The situation is similar when an active power is transferred by compensating the harmonics produced by the H-bridge through series active filter (FCCM).

Figure 16 shows simulation and practical validation of the balance operation of the converter with balanced capacitors voltage due to voltage swapping technique by redundant switching state selection presented in Table 3 together with converter current. Figure 17 depicts the simulation and practical results of the grid voltage and converter current. The signals are in-phase which tells that the converter works as a rectifier. Figure 18 depicts the low voltage laboratory prototype of a proposed AHMMC converter. Table 7 presents the simulation and experimental current THD value of the converter operating at different power ratings.

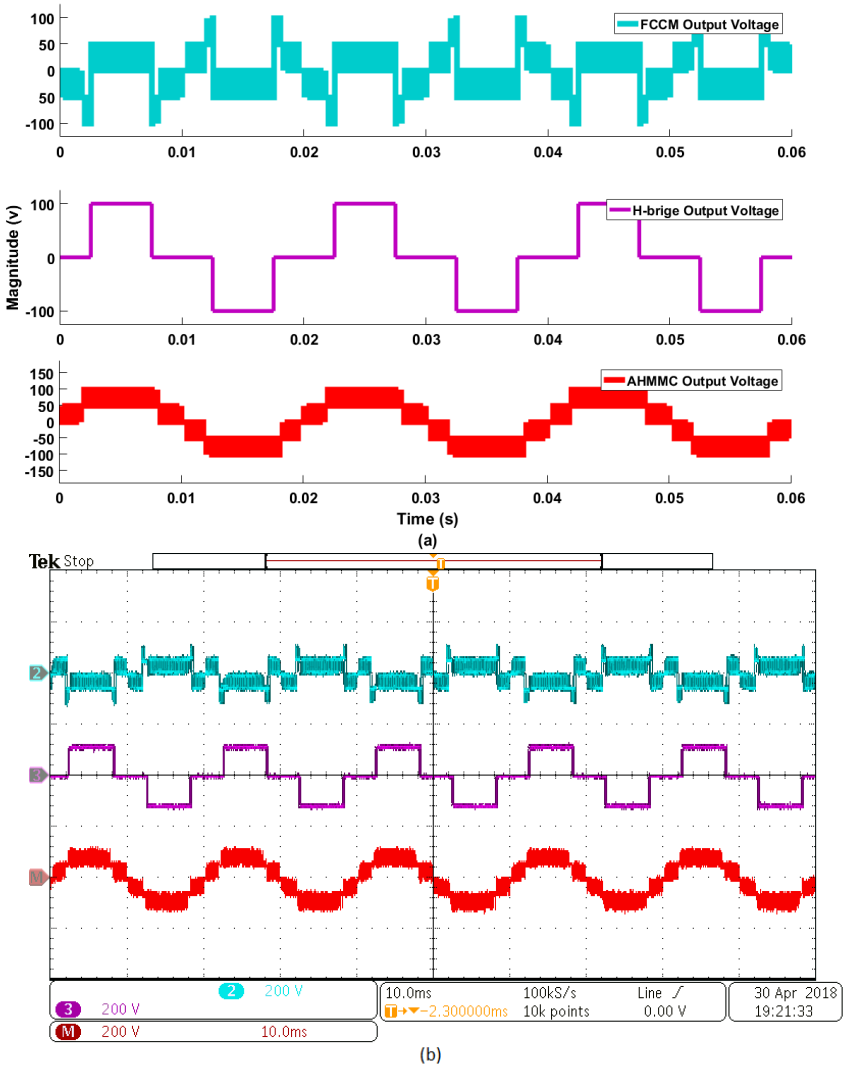

Figure 15. AHMMC converter output at m = 0.89, (**a**) simulation validation, and (**b**) experimental validation, traces chanels 2 and 3 (200 V/div).

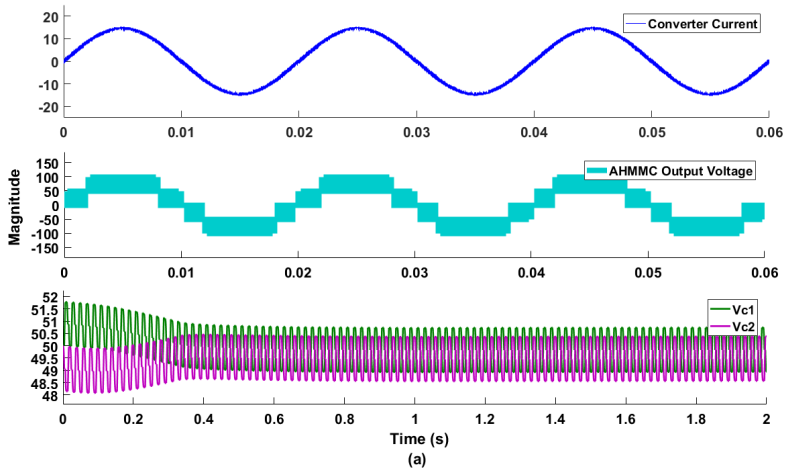

Figure 16. *Cont.*

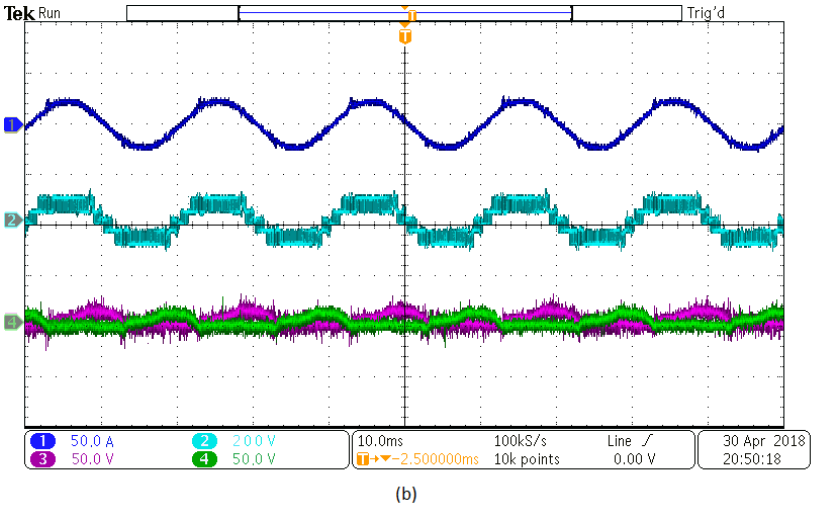

Figure 16. AHMMC converter output, (**a**) simulation validation of capacitor voltage balancing togather with a unity power factor, and (**b**) experimental validation, traces channels 1, 3, 4 (50 V/div), and 2 (200 V/div).

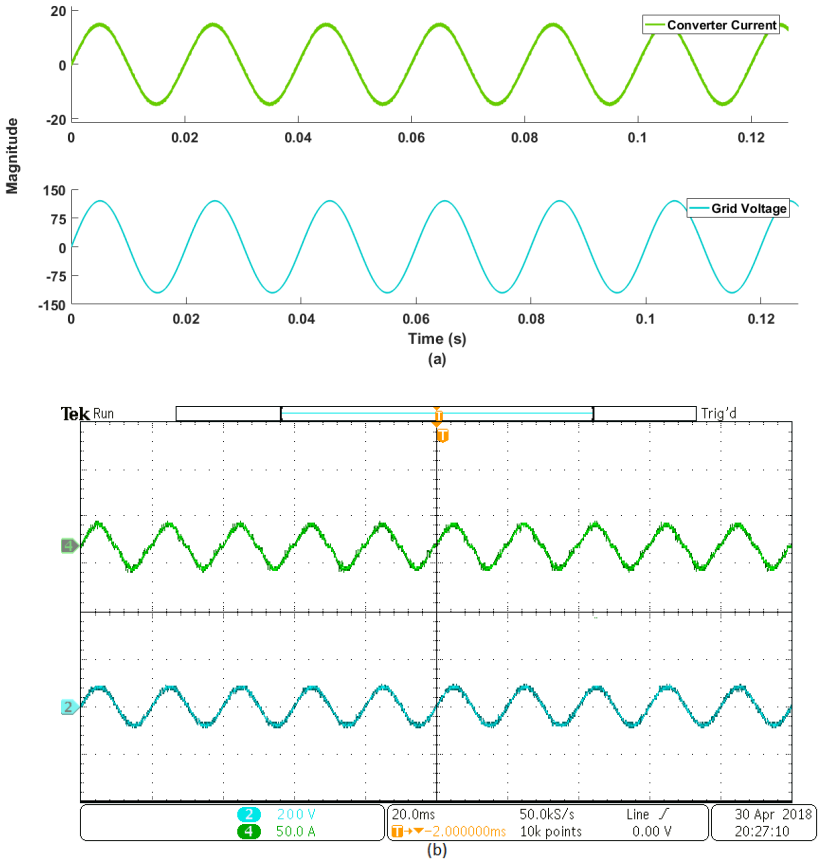

Figure 17. Low distortion in input current, (**a**) simulation validation of minimum distorion in current injected to ac main, and (**b**) experimental validation of minimum distortion in current injected to ac main. traces channels 2 (200 V/div), and 4 (50 A/div).

Table 7. Current THD of AHMMC operating at differnt power rating.

Current THD	Power Rating		
	25%	**50%**	**100%**
Simulation THD	6.55	3.31	1.66
Experiment THD	7.95	4.87	2.98

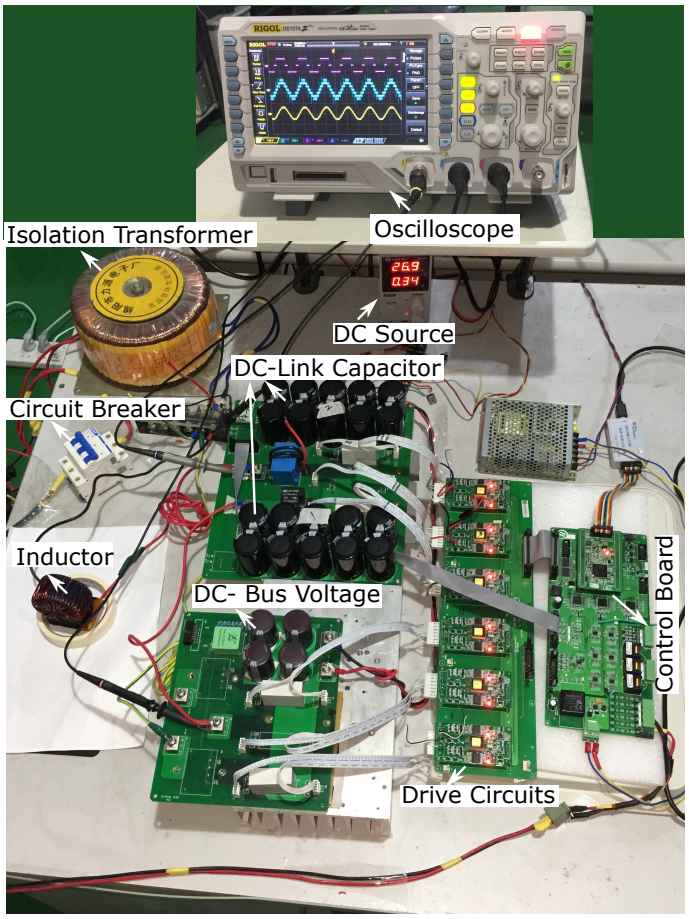

Figure 18. Experimental setup.

5. Comparision and Discussion

In this paper, the important characteristics of five different converter configurations were examined. A comparison is carried out among these topologies under power semiconductor devices (IGBT) available in different voltage levels (2.3, 3.3, and 4.16 kV) [30].

The NPC VSC has superior features compared to other hybrid converters presented here for upper voltage range up-to 3 kV for present devices operating at 1 kHz average switching frequency [40]. The key features include low conduction losses, better voltage and current THD, low components count and equal voltage stress on the active switches. However, due to the unequal loss distribution, the result is unsymmetrical temperature among the semiconductor devices.

Considering the dc bus voltage up-to 5 kV, the structural design of hybrid H-NPC with H-bridge has the benefit of seven-level output voltage by two more active switches which is inevitable. The topology can be used for higher voltage range as the dc link required for harmonic compensation is 0.35 E at maximum modulation index. Moreover, the switching losses is reduced by modulating the high voltage stressed switch at fundamental switching frequency. The structural drawback of

the H-NPC converter is the high voltage stresses on half bridge leg of H-NPC converter. The voltage stresses can be higher across the H-bridge for the topology used in higher range voltage application.

A CHB based converter is introduced to tackle the limit imposed by high voltage stresses which is reduced by splitting the dc link voltage of the H-bridge converter using five-level CHB for higher voltage application. However, the high component count will lead to a high system cost. A topology based on a H-NPC and cascaded module achieves better output voltage with reduced active switches and minimum conduction loss in comparison with CHB based topology.

The proposed converter topology is designed for a lower medium voltage range up-to 5 kV with the maximum output voltage of seven-level. Considering the same system parameters, the proposed topology has certain advantages over other hybrid converter topologies, for example, the wide operating rang, low current THD presented in Table 11, and the lower component count in comparison with the hybrid converter topologies listed in Table 8. The switching losses are addressed by operating the high stressed switch with low switching frequency; the switching loss of the proposed converter is lower which results in higher efficiency in comparison with NPC VSC as shown in Figure 19 based on the converter parameters given in Table 9. However, the current THD of the NPC converter is less than the AHMMC converter.

Table 8. Component count of converter.

Converter	Components Count		
	Active Switches	**Diode**	**Dc-Link Capacitor**
NPC	8	4	2
HNPC with H-bridge	10	2	3
HNPC with cascaded module	12	2	4
Proposed AHMMC converter	10	-	3

Table 9. Converter parameter for efficiency comparison.

Parameter	Value			
DC bus voltage	3 kV			
Grid voltage	1.75 kV (rms)			
Modulation index	Maximum modulation index			
Reactor inductance	0.6 mH			
	V_{CES}	V_{CESat}	Rise time	Fall time
IGBT	1.7 kV	2.45 V	0.29 µs	0.29 µs
IGBT	4.5 kV	2.84 V	0.35 µs	0.35 µs

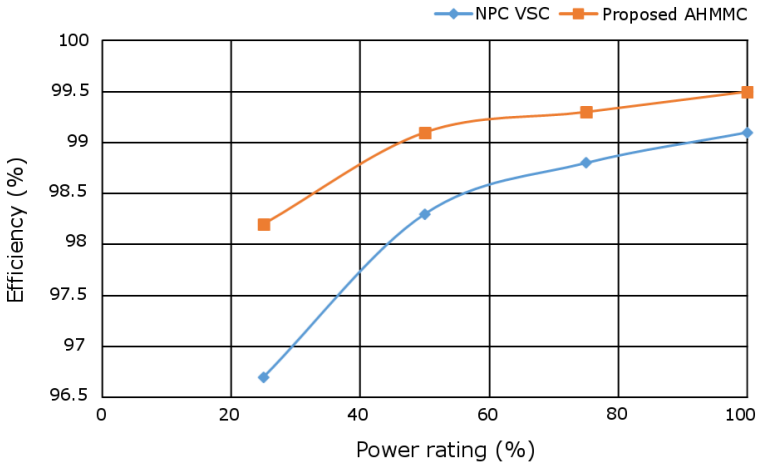

Figure 19. Converter's efficency.

Table 10 presents voltage stress on the semiconductor switches. The proposed topology has four active switches (in the outer leg of FCCM) which are under low voltage stress; thus, they are operated at high frequency to minimize the current ripple together with inductor size. The current total harmonic distortion (THD) of the converter operating at different power ratings is given in Table 11, which shows that the proposed converter current THD is lower than the other hybrid converter topologies discussed here.

Table 10. Voltage stress on semiconductor devices.

Semiconductor Devices	Voltage Stress	
	Active Switches	**Diode**
Half bridge NPC	E/2	E/2
Half bridge	E/2	–
Cascaded module centre cell	E	–
Cascaded module outer cell	E/2	–
Half Bridge (AHMMC)	E	–
Cascaded module centre cell	E	–
Cascaded module outer cell	E/2	–

Table 11. Converters current THD operating at different power ratings.

Converter	Power Rating		
	25%	**50%**	**100%**
NPC	5.31	2.83	1.38
HNPC with H-bridge	6.71	3.43	1.73
HNPC with cascaded module	6.59	3.39	1.71
Proposed AHMMC	6.55	3.31	1.66

6. Conclusions

In this paper, a comparative analysis of MLC topologies for medium voltage traction application has been demonstrated. The study will be helpful to select a suitable converter among the converters discussed for specific voltage ranges. Among all the converters, the proposed AHMMC configuration is studied in detail for medium voltage high power application due to its various features including a better output voltage, reduced switch losses by minimizing the switching frequency as well as the component count, and improved power factor with low THD. The proposed system performance is validated through simulation results using MATLAB/Simulink. Furthermore, a low voltage laboratory prototype is developed to test the performance of the proposed converter in practice.

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