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A Two-Stage X-Band 20.7-dBm Power Amplifier in 40-nm CMOS Technology

Zhichao Li [1], Shiheng Yang [2], Samuel B. S. Lee [1] and Kiat Seng Yeo [1,*]

[1] Electronics Design Lab, Singapore University of Technology and Design, Singapore 487372, Singapore; zhichao_li@mymail.sutd.edu.sg (Z.L.); samuel_lee@mymail.sutd.edu.sg (S.B.S.L.)

[2] School of Electronic Science and Engineering, University of Electronic Science and Technology of China, Chengdu 610054, China; ysh@uestc.edu.cn

* Correspondence: kiatseng_yeo@sutd.edu.sg; Tel.: +65-6499-4895

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Abstract: For higher integration density, X-band power amplifiers (PAs) with CMOS technology have been widely discussed in recent publications. However, with reduced power supply voltage and device size, it is a great challenge to design a compact PA with high output power and power-added efficiency (PAE). In the proposed design, a 40-nm standard CMOS process is used for higher integration with other RF building blocks, compared with other CMOS PA designs with larger process node. Transistor cells are designed with neutralization capacitors to increase stability and gain performance of the PA. As a trade-off among gain, output power, and PAE, the transistor cells in driving stage and power stage are biased for class A and class AB operation, respectively. Both transistor cells consist of two transistors working in differential mode. Furthermore, transformer-based matching networks (TMNs) are used to realize a two-stage X-band CMOS PA with compact size. The PA achieves an effective conductivity (EC) of 117.5, which is among the highest in recently reported X-band PAs in CMOS technology. The PA also attains a saturated output power (P_{sat}) of 20.7 dBm, a peak PAE of 22.4%, and a gain of 25.6 dB at the center frequency of 10 GHz under a 1 V supply in 40-nm CMOS.

Keywords: power amplifier (PA); X-band; CMOS; 40-nm; neutralization; differential; transformer-based matching network

1. Introduction

High data rate is one of the key factors for modern 5G communication system design. As conventional UHF band has been occupied, higher frequency bands, such as X-band, are explored by researchers to offer higher data rate communication for 5G applications [1]. Furthermore, X-band has important applications, such as satellite communications and phased-array systems. Thus, X-band communication systems have received a significant attention in recent years [1–26].

In the case of X-band PA ICs, many reported designs can achieve watt-level output power, but most of them are implemented with GaAs/GaN process in recent publications [21–26], which is not suitable for low cost portable wireless communication systems. For these applications, CMOS technology is the most suitable candidate for high-level integration and low-cost implementation. With the CMOS technology, the device size and the supply voltage are continuously being scaled down to realize better performance with reduced power consumption. However, it creates a challenge for CMOS PA to achieve high output power with compact size, especially for frequencies higher than 6 GHz, such as X-band and millimeter-wave bands.

Most of the reported X-band CMOS PA are implemented with 180 nm CMOS technology [2–8,10, 12,13,18,19], while some others are with 90 [9,11] and 65 nm [20] CMOS technology. On the other hand, the authors of [14–16] showed the possibility of using shrinking 45 nm node to implement an X-band

PA with reasonable performance. However, these PAs are designed with CMOS SOI process instead of standard CMOS process with complicated power supplies, which notably increase the cost and decrease their possibility to integrate with other blocks of an X-band wireless communication system. The PA reported by Author3 [17] is implemented with standard 40 nm CMOS technology, but the PA works on all digital switching mode (class E), which can hardly support modern modulation schemes compared with its counterpart works on linear mode. Furthermore, the PA only supports the lower frequency range (8–9.5 GHz) of the X-band and with a power supply higher than 1 V. The whole list of publications about CMOS PAs covering X-band frequencies is shown in Table 1.

Table 1. Lists of publications about CMOS power amplifiers covering X-band frequencies.

Reference	Process	Frequency (GHz)	V_{DD} (V)	Publication Year
[2]	180 nm CMOS	0–14	1.3	2004
[3]	180 nm CMOS	3.1–10.6	1.8	2005
[4]	180 nm CMOS	3–10	2	2006
[5]	180 nm CMOS	3.7–8.8	-	2007
[6]	180 nm CMOS	6–10	1.5	2008
[7]	180 nm CMOS	8.5–10	3.3	2008
[8]	180 nm CMOS	4–17	3.6	2009
[9]	90 nm CMOS	5.2–13	2.8	2010
[10]	180 nm CMOS	7–12	3.6	2010
[11]	90 nm CMOS	5.2–13	-	2010
[12]	180 nm CMOS	6.5–13	3.6	2011
[13]	180 nm CMOS	8.6–10.3	3	2011
[14]	45 nm CMOS SOI	4–50	1.1/6	2012
[15]	45 nm CMOS SOI	9–15	3.6/4.8	2013
[16]	45 nm CMOS SOI	10–32	0.75/1/2	2014
[17]	40 nm	3.5–9.5	1.2	2015
[18]	180 nm	7–10	3.3	2017
[19]	180 nm	3/9	3.6	2018
[20]	65 nm	8–11.4	1.2	2019

Some reported two-stage X-band PAs achieved more than 20 dBm output power with 3.6 and 3 V power supplies in [12,13,19], respectively. The power supply voltage in these designs is much higher than 1 V. In addition, a two-way power combining is utilized in these designs, which results in large die size occupation. The CMOS PA reported in [27] uses 1 V power supply and achieves a much higher peak PAE of 34.5%, but it works in switching mode. Thus, it can hardly supports modern modulation schemes, which require high linearity. Two other reported X-band PAs [7,20] achieve high output power utilizing two-stage cascode with TMN architecture. These two PAs achieve peak PAE of 24.5% and 19%, respectively.

In this paper, a two-stage X-band PA in 40-nm standard CMOS technology is presented. With shrinking process node, it can offer better integration capability compared with other X-band CMOS PA designs. Instead of switch mode, the proposed PA works in linear mode. This ensures the proposed PA can support any modulation scheme without limitations [28]. The proposed PA is implemented with a transformer-based matching network (TMN) to provide more degrees of design freedom, while occupying similar chip area as a single inductor [29]. While operating at $V_{DD} = 1$ V, the proposed PA has achieved a saturated output power of 20.7 dBm and 22.4% peak PAE at 10 GHz (23.5% peak PAE at 11 GHz). The PA also achieves an EC [20] of 117.5, which is among the best EC performances in recently reported X-band PAs in CMOS technology.

The structure of this article is as follows. Section 2.1 provides the architecture of proposed power amplifier. Section 2.2 discusses design procedure of transistor cells. Section 2.3 discusses matching network design among input GSG pads, transistor cells, and output GSG pads. Section 3 gives a photograph of the fabrication and measured results of the PA. The conclusion and references are in Section 4.

2. PA Design

2.1. PA Architecture

Figure 1 presents the schematic of the proposed PA. The PA consists of a driving stage and a power stage. Both the driving stage and the power stage are biased to linear mode instead of switching mode for better linearity. The driver stage is biased to class A operation for high gain, whereas the power stage is biased to class AB operation for high efficiency. Both the driving stage and the power stage consist of two NMOS transistors and work in differential modes.

For output and inter-stage matching network, a transformer T-model was used to fulfill matching procedure on Smith Chart. The transformer in the output matching network also works as a balun to transform differential input into single-ended output. On the other hand, for input matching network, the resonator-based design procedure was used for wider bandwidth consideration. The transformer in the input matching network works as a balun to transform single-ended input into differential output as well. Furthermore, both the input and output are connected to GSG pads with 100 µm pitch in the chip layout.

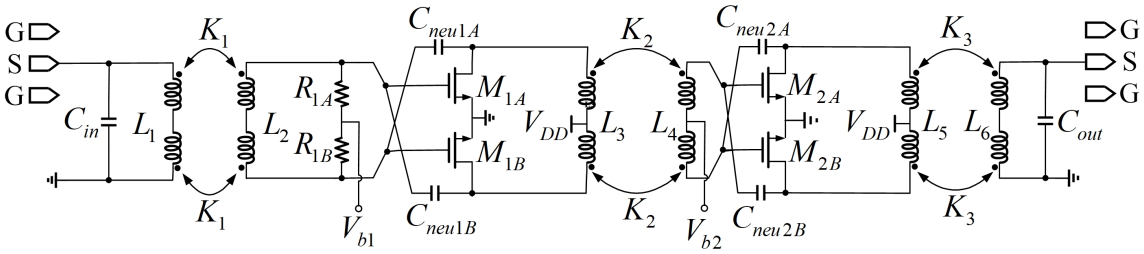

Figure 1. Schematic of the two-stage transformer-coupled PA.

2.2. Design of Transistor Cells

Transistor size of the power stage should be carefully chosen for PA design, as their size can determine output power and maximum PAE [12]. In this design, the unit transistor size is set to be 3 µm × 32 µm. Then, DC IV sweep is simulated based on the unit transistor size to determine the biasing voltage for each stage. Here, V_{b1} and V_{b2} in Figure 1 are set for class A and class AB operating condition, respectively. The multiplier of unit transistor cell is determined through several times of iterations of load pull simulations, in order to make the output power higher than 20 dBm. Here, the multiplier is set to be 20 for the transistor size of the power stage. After that, the transistor size of the driving stage is determined to be half the size of the power stage. In other words, the transistor size of the driving stage is 3 µm × 32 µm × 10 µm.

Once the transistor size is fixed, the neutralization capacitors are determined based on S_{12} performance of the differential pairs. The schematic used to tune neutralization capacitors is shown in Figure 2. The capacitor value is used when the best isolation performance is observed, i.e. when the smallest S_{12} value is observed. In this design, the neutralization capacitors of the power stage are set to be $382fF$, and the neutralization capacitors of the driving stage are set to be $193fF$.

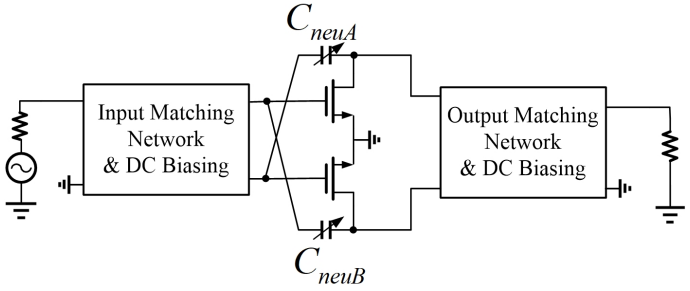

Figure 2. Schematic for neutralization capacitor tuning.

When the transistor size and the neutralization capacitors are fixed, both the input and output impedance of each stage can be extracted by load pull simulation, as shown in Figure 3 [30]. In Figure 3, both the input source impedance R_{in} and the output load impedance R_{out} are 50 Ω.

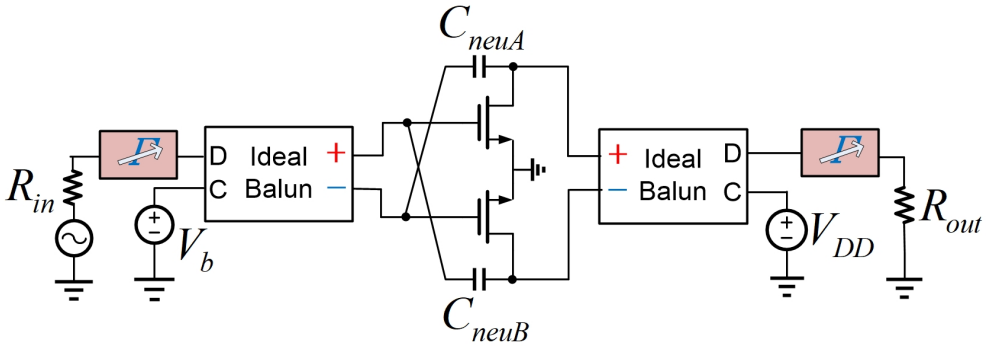

Figure 3. Schematic for optimal impedance extraction.

2.3. PA Matching Network Design

In the proposed design, transformers are used in matching networks. This is for compact size and convenient DC biasing, while occupying similar die area when compared to circuits with inductors [29].

The PA design is based on UMC's 40-nm CMOS technology, and its metal layer definition is shown in Figure 4. There are two thick metal layer in the top: Al_RDL (2.8 μm) and M7 (3.4 μm). All other layers (M1–M6) are thin metal layers. In this design, the top two thick metal layers are used for transformer layout, and thin metal layers are only considered as interconnections when the two thick metal layers are not available.

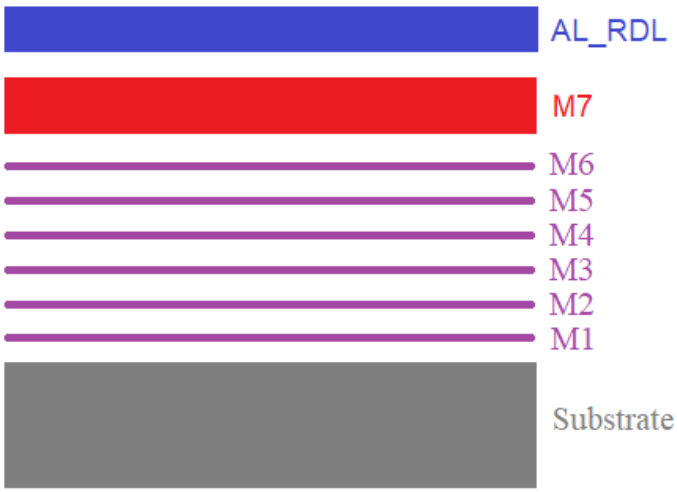

Figure 4. Metal layer stacks for UMC 40-nm CMOS technology.

2.3.1. Inter-Stage/Output Matching Network Design

For inter-stage matching network, instead of using optimal impedance obtained from load pull simulation, the conjugate of output impedance of the driving stage is used to simplify the design procedure. Normally, optimal impedance extracted from load pull and conjugate of output impedance are quite close to each other. Furthermore, as transistors of the driving stage are chosen to be half the size of those in the last stage, output power of the driving stage is far from P_{1dB} point. Thus, it is possible to get maximum current and maximum voltage swing simultaneously. In this condition, load pull is not necessary, and using the conjugate of output impedance as matching target for input impedance of the power stage is more desirable.

The schematic about how impedance are extracted for inter-stage matching is shown in Figure 5. Here, $Z_{out1} = 10.7 - j2.9\ \Omega$ and $Z_{in2} = 1.5 - j19.1\ \Omega$ (extracted under large signal S-parameter simulation). Thus, the inter-stage matching network should match the conjugate of output impedance of the driving stage ($Z^*_{out1} = 10.7 + j2.9\ \Omega$) to the input impedance Z_{in2} of the power stage. The transformer T-model is used for inter-stage matching network design, with the same technique stated in [31]. The proposed T-model and its equivalent transformer with Smith chart demonstration is shown in Figure 6, where the relation between mutual inductance M and coupling factor K is given by Equation (1).

$$K = \frac{M}{\sqrt{L_P * L_S}} \tag{1}$$

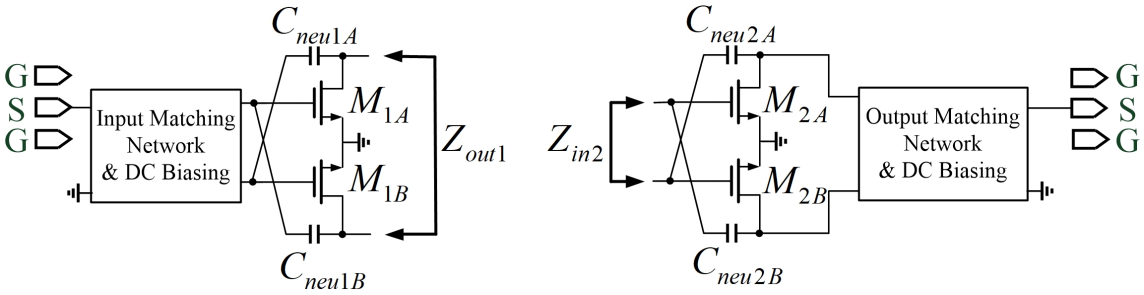

Figure 5. Schematic about impedance extraction for inter-stage matching.

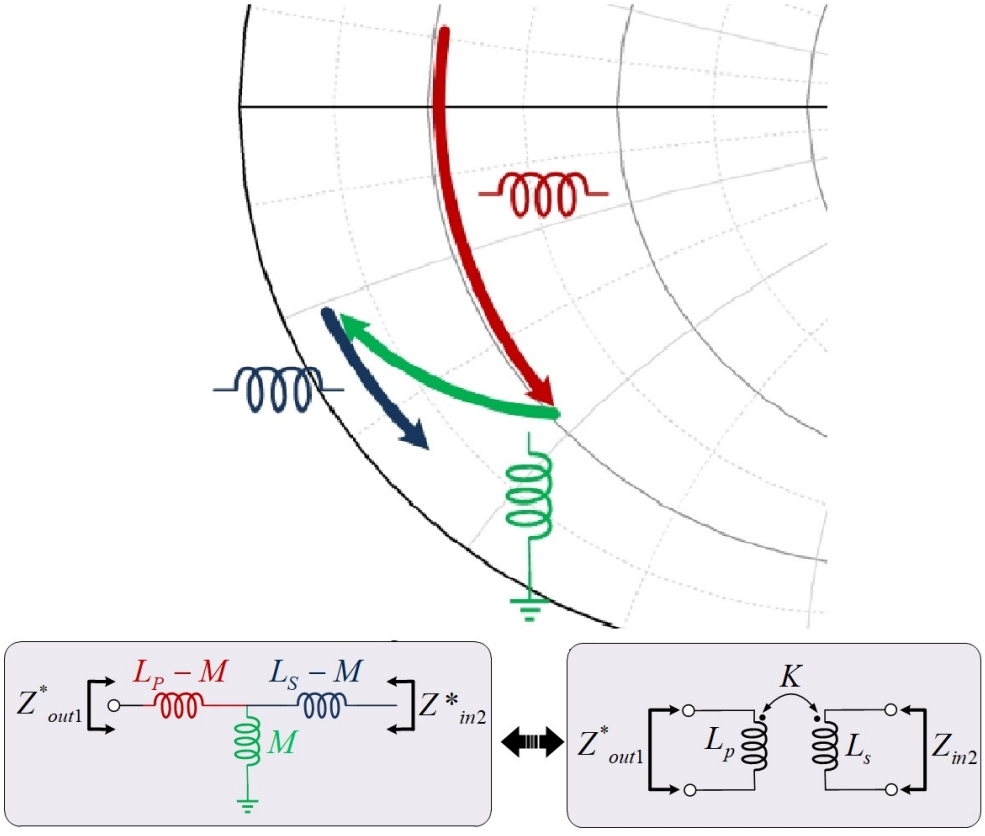

Figure 6. Smith chart of the inter-stage matching network with transformer T-model and its equivalent transformer.

As there is only a transformer T-model, the inter-stage matching network can be realized with merely a transformer. In Figure 6, $L_P = 674$ pH, $L_S = 392$ pH, and $M = 243$ pH. The EM setup with layout of the inter-stage transformer is shown in Figure 7. Then, parameters of the transformer are extracted based on s4p file get from EM simulation. Testbench for parameter extraction is shown in

Figure 8. Based on S-parameter simulation of the testbench with two extraction ports, the extracted parameter results are given by Equations (2)–(4), where f is the central frequency of 10 GHz.

$$L_P = \frac{Imag(Z_{11})}{2 * \pi * f} \tag{2}$$

$$L_S = \frac{Imag(Z_{22})}{2 * \pi * f} \tag{3}$$

$$M = \frac{Imag(Z_{21})}{2 * \pi * f} \tag{4}$$

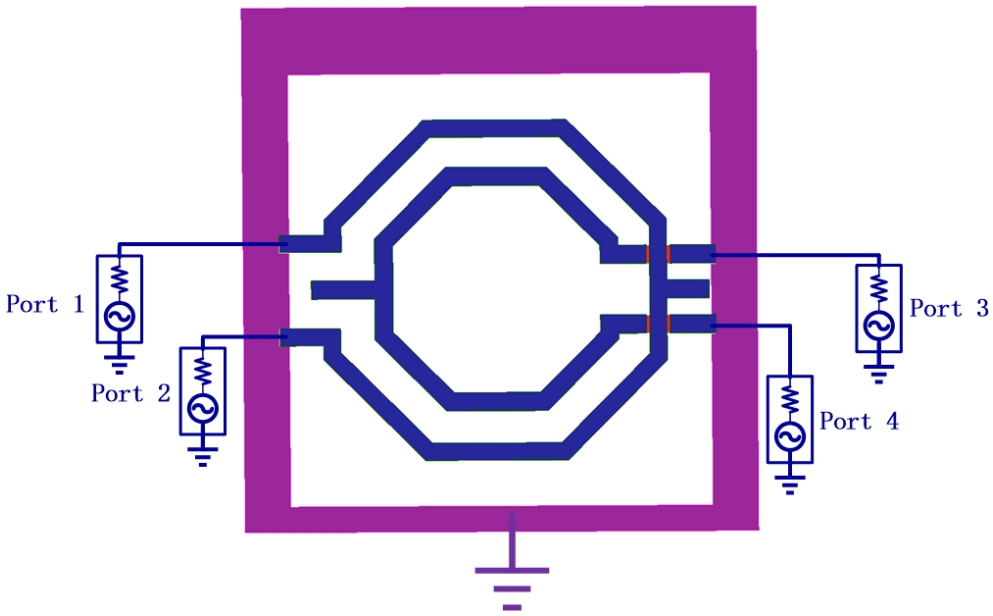

Figure 7. EM setup with layout of the inter-stage transformer.

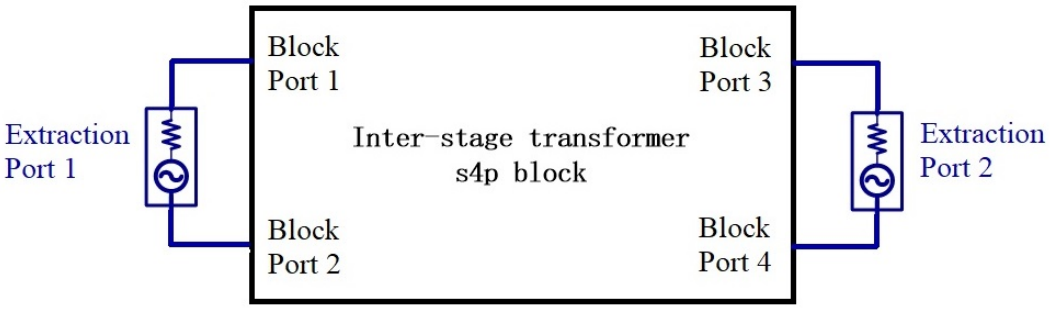

Figure 8. Testbench for parameter extraction of the inter-stage transformer.

The inter-stage transformer is implemented with stacked Al_RDL and M7. M7 is also used as interconnections of the secondary coil, and primary coil is implemented with Al_RDL instead of stacked layers when the interconnections go through. The transformer is enclosed with ground for isolation.

Similar as inter-stage matching network, the output matching network is also designed with transformer T-model, as shown in Figure 9 [31].

Considering the fact that the output matching network is connected with GSG pads (100 µm pitch). The parasitic capacitor of the the GSG C_{pad} should be simulated, and considered as part of the C_s in Figure 9. The EM simulation setup with ADS Momentum is shown in Figure 10. With EM simulation, $C_{pad} = 43fF$ is extracted. Thus, a parallel capacitor $C_s^{'}$ is placed next to the output GSG pads,

as calculated in Equation (5). In the setup, two ground pads are connected together with a narrow metal track. This ensures parasitic capacitors between both sides of ground pad to signal pad can be accounted for.

$$C_s^{'} = C_s - C_{pad} \tag{5}$$

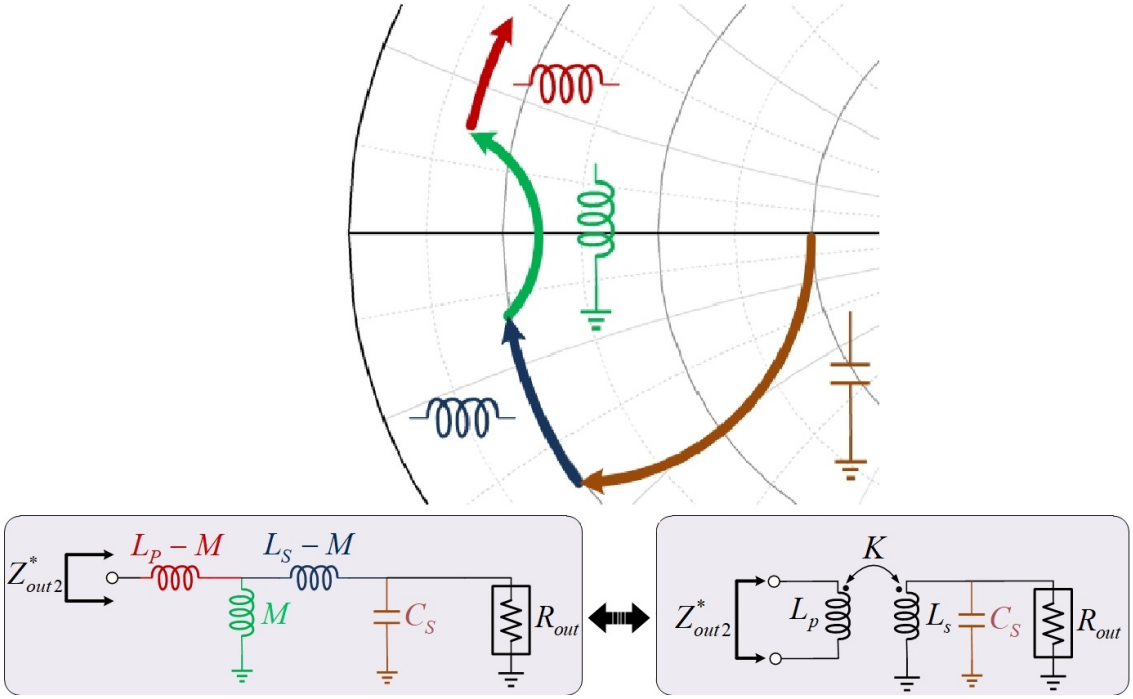

Figure 9. Smith chart of the output matching network with transformer T-model and its equivalent transformer.

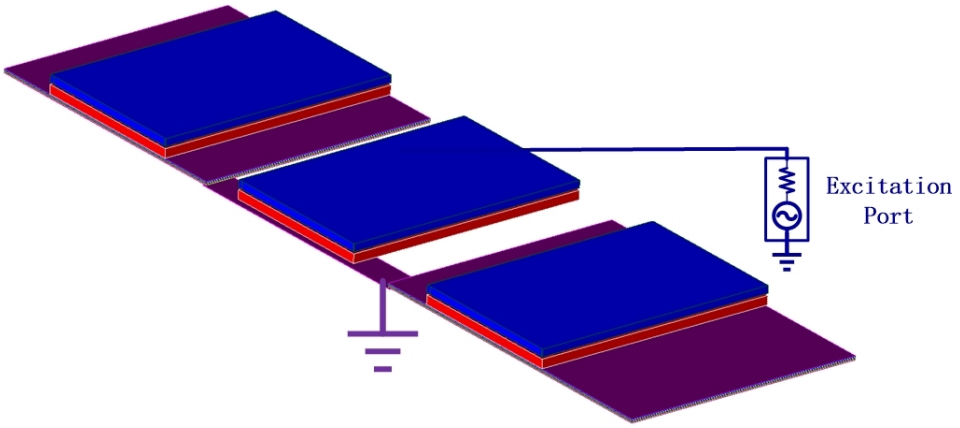

Figure 10. EM simulation setup for parasitic capacitor extraction of GSG pads.

2.3.2. Input Matching Network Design

The input matching network is designed when all the other parts of the PA have been determined. It is designed as a Magnetically Coupled Resonator (MCR), as we discussed in [31]. The MCR design technique gives us flexibility to tune the bandwidth and passband ripple of the matching network with coupling factor of the transformer. The schematic of the input matching network is shown in Figure 11. Similar to the output matching network, parasitic capacitor C_{pad1} of the GSG pads is added as part of the input capacitor.

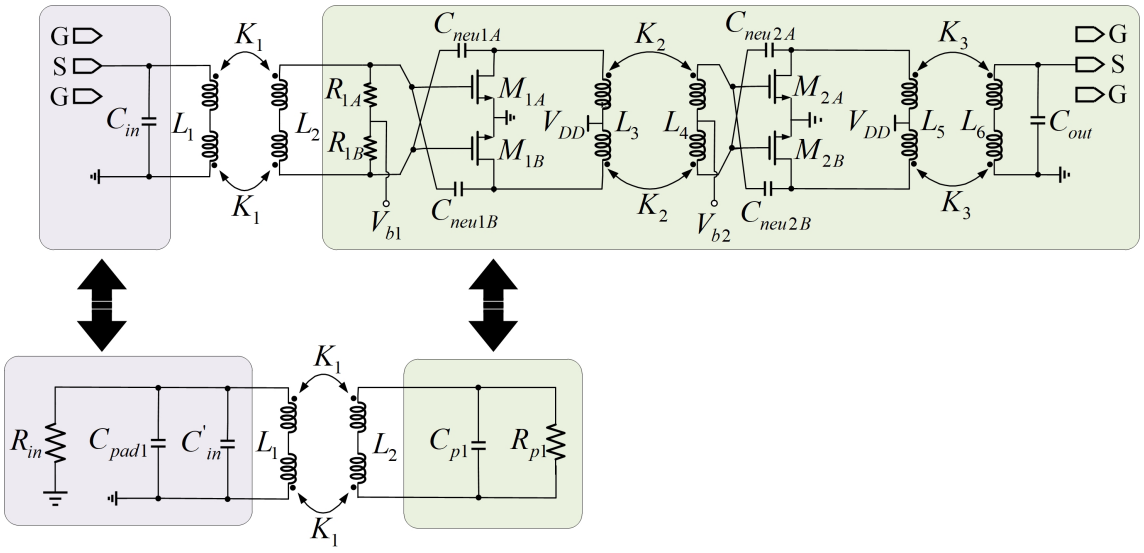

Figure 11. Schematic of input matching network.

In Figure 11, $L_1 = 208$ pH, $L_2 = 558$ pH, and $K_1 = 0.27$ pH. Considering the fact that the input balun is with single-ended input and differential output, its transformer parameter extraction method is different from that of the inter-stage transformer. The EM setup with layout of the input transformer is shown in Figure 12. Then, parameters of the transformer are extracted based on s3p file get from EM simulation. Testbench for parameter extraction is shown in Figure 13. Similar to inter-stage transformer, the extracted inductance of primary and secondary coil and mutual inductance are calculated with Equations (2)–(4).

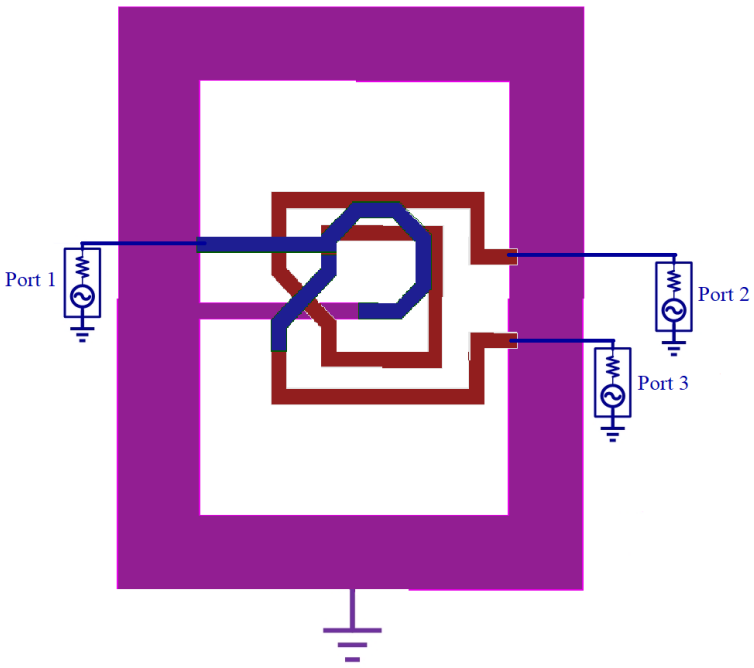

Figure 12. EM setup with layout of the input transformer.

3. Fabrication and Measurement

A chip photograph of the fabricated PA is shown in Figure 14, and the chip size without pads is 0.90 mm × 0.37 mm (1.00 mm × 0.46 mm with pads).

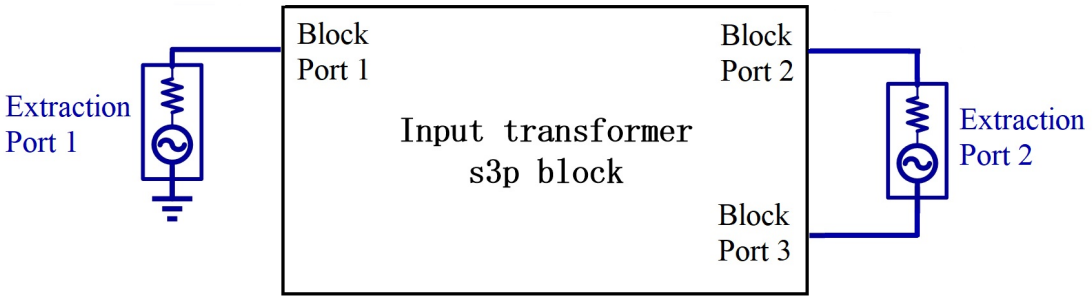

Figure 13. Testbench for parameter extraction of the input transformer.

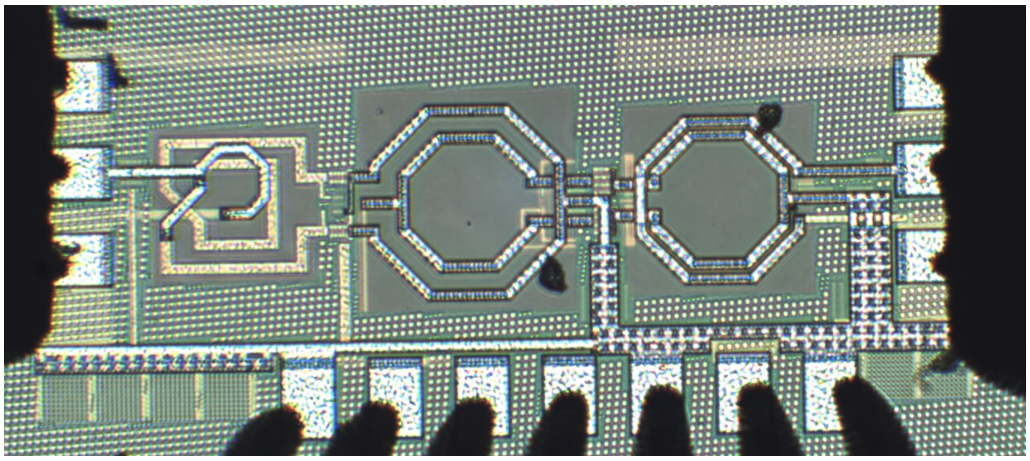

Figure 14. Photograph of the fabricated X-band PA.

Figure 15 compares the measured gain, output power and PAE performance of the PA versus input power for frequency range 8–12 GHz in steps of 2 GHz. Figure 16 shows measured results of the maximum output power (Pout), output 1 dB gain compression point (OP1dB), and peak PAE from 8 to 12 GHz in steps of 1 GHz of the PA. The PA achieves a peak gain of 25.6 dB, OP1dB of 13.7 dBm, and peak PAE of 22.4% at 10 GHz. The maximum peak PAE of 23.5% is obtained at 11 GHz.

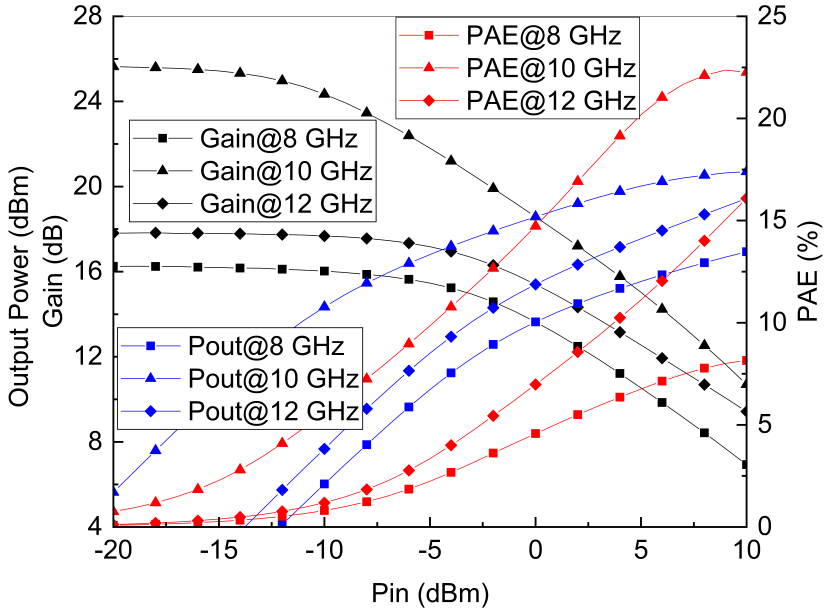

Figure 15. Measured power performance of the X-band PA for frequency range 8–12 GHz in steps of 2 GHz.

To assess the capability of the transistors in generating output power to the load with a variety of power supply, an EC defined in millisiemens (mS) [20] was used.

$$G_S = P_{out}/V_{DD}^2 \tag{6}$$

The proposed PA is compared with previously published state-of-the-art X-band CMOS PAs, as shown in Table 2. The comparison shows that our work has one of the best EC performances, while still being competitive in terms of output power, gain, and PAE when compared to the previously published works.

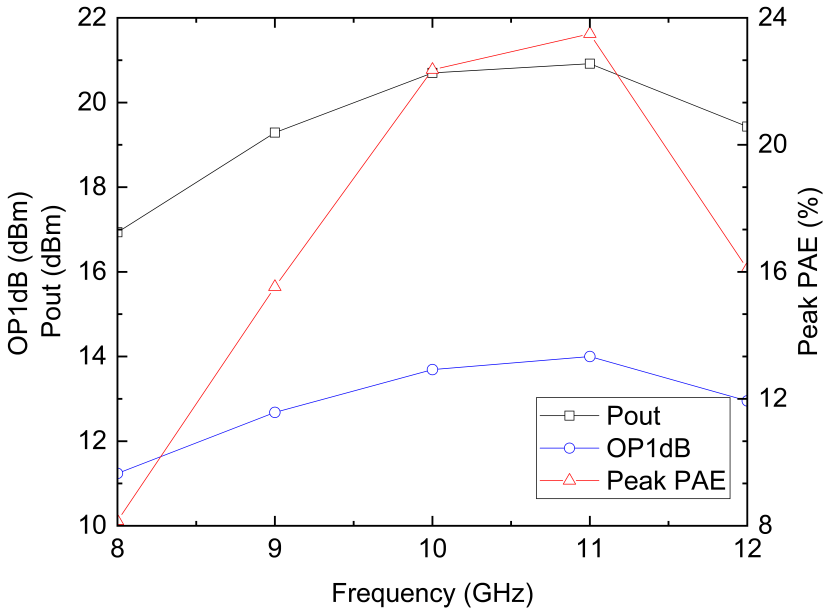

Figure 16. Measured maximum output power output (Pout), OP1dB, and peak PAE versus frequency.

Table 2. Summary and comparison of proposed PA and previously published X-band CMOS PA with similar architecture.

Reference	Technology	Frequency, GHz	Technique	P_{sat}, dBm	Gain, dB	V_{DD}, V	PAE, %	EC, mS
[20]	65 nm CMOS	8.0–11.4	Two-stage cascode	20.5	24.4	1.2	24.5	77.9
[12]	0.18 µm CMOS	6.5–13.0	Two-stage push-pull	21.5	25.3	3.3	20.3	13.0
[13]	0.18 µm CMOS	8.6–10.3	Two-stage with 2-way power combining	24.5	25.0	3.0	24.5	31.3
[7]	0.18 µm CMOS	8.5–10.0	Two-stage cascode	23.5	29.0	3.3	19.0	20.6
This work	**40 nm CMOS**	**8.0–12.0**	**Two-stage TF-coupled**	**20.7**	**25.6**	**1.0**	**23.5**	**117.5**

4. Conclusions

In this work, an X-band CMOS power amplifier using UMC's 40-nm standard CMOS technology is presented. The shrinking process node supports higher integration with other building blocks, compared with other X-band CMOS PA designs with larger process node. The PA works in a linear mode to support modern modulation schemes. It consists of a driving stage and a power stage with transformer-based matching networks. Both the driving stage and the power stage are made of differential transistor cells with neutralization capacitors to enhance their stability and gain. The PA is among the designs with the best EC performance when compared with several CMOS X-band PAs with similar architecture. It also attains a saturated output power (P_{sat}) of 20.7 dBm, a gain of 25.6 dB, and a peak PAE of 22.4% at 10 GHz under a 1 V supply in 40-nm CMOS.

Author Contributions: Conceptualization, formal analysis, investigation, data curation, writing—original draft preparation, validation, Z.L.; methodology, Z.L. and S.Y.; writing—review and editing, Z.L., S.Y., S.B.S.L., and K.S.Y.; and supervision, project administration, and funding acquisition, K.S.Y. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Peng, K.-C.; Lin, C.-C.; Lin, Z.-H.; Chen, C.-C.; Hsu, C.-C. A low noise X-band frequency synthesizer for 5G applications. In Proceedings of the IEEE International Conference on Consumer Electronics-Taiwan (ICCE-TW), Nantou, Taiwan, 27–29 May 2016; pp. 1–2.
2. Liu, R.-C.; Lin, C.-S.; Deng, K.-L.; Wang, H. Design and analysis of DC-to-14-GHz and 22-GHz CMOS cascode. *IEEE J. Solid-State Circuits* **2004**, *39*, 1370–1374.
3. Hsu, H.C.; Wang, Z.W.; Ma, G.K. A low power CMOS full-band UWB power amplifier using wideband RLC matching method. In Proceedings of the IEEE Conference on Electron Devices and Solid-State Circuits, Hong Kong, China, 19–21 December 2005; pp. 233–236.
4. Lu, C.; Pham, A.V.; Shaw, M. A CMOS power amplifier for full-band UWB transmitters. In Proceedings of the IEEE Radio Frequency Integrated Circuits (RFIC) Symposium, San Francisco, CA, USA, 10–13 June 2006.
5. Chao, L.; Pham, A.H.; Shaw, M.; Saint, C. Linearization of CMOS broadband power amplifiers through combined multigated transistors and capacitance compensation. *IEEE Trans. Microw. Theory Tech.* **2007**, *55*, 2320–2328. [CrossRef]
6. Chung, H.-W.; Hsu, C.-Y.; Yang, C.-Y.; Wei, K.-F.; Chuang, R.H. A 6-10-GHz CMOS power amplifier with an inter-stage wideband impedance transformer for UWB transmitters. In Proceedings of the IEEE 38th European Microwave Conference, Amsterdam, The Netherlands, 27–31 October 2008; pp. 305–308.
7. Ku, B.-H.; Baek, S.-H.; Hong, S. A X-band CMOS power amplifier with on-chip transmission line transformers. In Proceedings of the 2008 IEEE Radio Frequency Integrated Circuits Symposium, Atlanta, GA, USA, 15–17 June 2008; pp. 523–526.
8. Huang, P.-C.; Lin, K.-Y.; Wang, H. A 4–17 GHz Darlington Cascode Broadband Medium Power Amplifier in 0.18-µm CMOS Technology. *IEEE Microw. Wirel. Components Lett.* **2009**, *20*, 43–45. [CrossRef]
9. Wang, H.; Sideris, C.; Hajimiri, A. A CMOS broadband power amplifier with a transformer-based high-order output matching network. *IEEE J. Solid-State Circuits* **2010**, *45*, 2709–2722. [CrossRef]
10. Chi, P.-S.; Tsai, Z.-M.; Kuo, J.-L.; Lin, K.-Y.; Wang, H. An X-band, 23.8-dBm fully integrated power amplifier with 25.8% PAE in 0.18-µm CMOS technology. In Proceedings of the IEEE European Microwave Integrated Circuits Conference, Paris, France, 27–28 September 2010; pp. 436–439.
11. Wang, H.; Sideris, C.; Hajimiri, A. A 5.2-to-13GHz class-AB CMOS power amplifier with a 25.2 dBm peak output power at 21.6% PAE. In Proceedings of the IEEE International Solid-State Circuits Conference-(ISSCC), San Francisco, CA, USA, 7–11 February 2010; pp. 44–45.
12. Ku, B.-H.; Baek, S.-H.; Hong, S. A wideband transformer-coupled CMOS power amplifier for X-band multifunction chips. *IEEE Trans. Microw. Theory Techn.* **2011**, *6*, 1599–1609. [CrossRef]
13. Comeau, J.P.; Thoenes, E.W.; Imhoff, A.; Morton, M.A. X-band +24 dBm CMOS power amplifier with transformer power combining. In Proceedings of the IEEE 2011 IEEE 11th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems, Phoenix, AZ, USA, 17–19 January 2011; pp. 49–52.
14. Sarkas, I.; Balteanu, A.; Dacquay, E.; Tomkins, A.; Voinigescu, S. A 45 nm SOI CMOS Class-D mm-Wave PA with >10 V pp differential swing. In Proceedings of the IEEE International Solid-State Circuits Conference, San Francisco, CA, USA, 19–23 February 2012; pp. 88–90.
15. Chen, J.-H.; Helmi, S.R.; Jou, A.Y.-S.; Mohammadi, S. A wideband power amplifier in 45 nm CMOS SOI technology for X band applications. *IEEE Microw. Wirel. Components Lett.* **2012**, *23*, 587–589. [CrossRef]
16. Helmi, S.R.; Chen, J.-H.; Mohammadi, S. An X to K a-Band Fully-integrated stacked power amplifier in 45 nm CMOS SOI technology. In Proceedings of the IEEE 14th Topical Meeting on Silicon Monolithic Integrated Circuits in Rf Systems, Newport Beach, CA, USA, 19–23 January 2014; pp. 74–76.

17. Qian, H.J.; Liang, J.O.; Luo, X. A 3.5–9.5 GHz compact digital power amplifier with 39.3% peak PAE in 40nm CMOS technology. In Proceedings of the IEEE International Wireless Symposium (IWS 2015), Shenzhen, China, 30 March–1 April 2015; pp. 1–4.
18. Tsai, J.-H.; Wang, J.-W. An X-Band Half-Watt CMOS Power Amplifier Using Interweaved Parallel Combining Transformer. *IEEE Microw. Wirel. Components Lett.* **2017**, *27*, 491–493. [CrossRef]
19. Jaeyong, K.; Nam, S. A Two-Stage S-/X-Band CMOS Power Amplifier for High-Resolution Radar Transceivers. *IEEE Microw. Wirel. Components Lett.* **2018**, *28*, 606–608.
20. Trinh, V.-S.; Nam, H.; Park, J.-D. A 20.5-dBm X-band power amplifier with a 1.2-V supply in 65-nm CMOS technology. *IEEE Microw. Wirel. Compon. Lett.* **2019**, *3*, 234–236. [CrossRef]
21. Bae, K.-T.; Lee, I.-J.; Kang, B.; Sim, S.; Jeon, L.; Kim, D.-W. X-Band GaN Power Amplifier MMIC with a Third Harmonic-Tuned Circuit. *Electronics* **2017**, *6*, 103. [CrossRef]
22. Chen, R.; Li, R.; Zhou, S.; Chen, S.; Huang, J.; Wang, Z. An X-Band 40 W Power Amplifier GaN MMIC Design by Using Equivalent Output Impedance Model. *Electronics* **2019**, *8*, 99. [CrossRef]
23. Shin, D.-H.; Yom, I.-B.; Kim, D.-W. X-band GaN MMIC power amplifier for the SSPA of a SAR system. In Proceedings of the IEEE International Symposium on Radio-Frequency Integration Technology (RFIT), Seoul, Korea, 30 August–1 September 2017; pp. 93–95.
24. Couturier, A.M.; Poitrenaud, N.; Serru, V.; Dionisio, R.; Fontecavc, J.J.; Camiade, M. 50% High Efficiency X-Band GaN MMIC Amplifier for Space Applications. In Proceedings of the IEEE 48th European Microwave Conference (EuMC), Madrid, Spain, 23–27 September 2018; pp. 352–355.
25. Lee, B.-H.; Park, B.-J.; Choi, S.-Y.; Lim, B.-O.; Go, J.-S.; Kim, S.-C. A 20 W GaN-based Power Amplifier MMIC for X-band Radar Applications. *J. IKEEE* **2019**, *23*, 181–187.
26. Kamioka, J.; Kuwata, E.; Hangai, M.; Nakahara, K.; Kamo, Y.; Shinjo, S.; Shimozawa, M. A 26-W X-Band High Efficiency GaN MMIC Power Amplifier with Compact Spurious Suppression Filters. In Proceedings of the IEEE Asia-Pacific Microwave Conference (APMC), Kyoto, Japan, 6–9 November 2018; pp. 1211–1213.
27. Kurniawan, T.A.; Yoshimasu, T. A 2.5-GHz 1-V High Efficiency CMOS Power Amplifier IC with a Dual-Switching Transistor and Third Harmonic Tuning Technique. *Electronics* **2019**, *8*, 69. [CrossRef]
28. Choe, Y.-J.; Nam, H.; Park, J.-D. A compact 5 GHz power amplifier using a spiral transformer for enhanced power supply rejection in 180-nm CMOS technology. *Electronics* **2019**, *8*, 1043. [CrossRef]
29. Jia, H.; Prawoto, C.C.; Chi, B.; Wang, Z.; Yue, C.P. A full Ka-Band power amplifier with 32.9% PAE and 15.3-dBm power in 65-nm CMOS. *IEEE Trans. Circuits Syst. Regul. Pap.* **2018**, *65*, 2657–2668. [CrossRef]
30. Shakib, S.; Park, H.-C.; Dunworth, J.; Aparin, V.; Entesari, K. A highly efficient and linear power amplifier for 28-GHz 5G phased array radios in 28-nm CMOS. *IEEE J. Solid-State Circuits* **2016**, *51*, 3020–3036. [CrossRef]
31. Li, Z.; Yang, S.; Liu, H.; Yeo, K.S. CMOS Transformer Design for X-band Power Amplifier Applications. In Proceedings of the International Conference on Solid-State and Integrated Circuit Technology (ICSICT), Kunming, China, 3–6 November 2020.