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A 2.4 GHz 2.9 mW Zigbee RF Receiver with Current-Reusing and Function-Reused Mixing Techniques

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Abstract: This study presents a low-power Zigbee receiver with a current-reusing structure and function-reused mixing techniques. To reduce the overall power consumption, a low noise amplifier (LNA) and a power amplifier (PA) share the biasing current with a voltage-controlled oscillator (VCO) in the receiving (RX) mode and transmitting (TX) mode, respectively. The function-reused mixer reuses the radio frequency trans-conductance (RF gm) stage to amplify the down-converted intermediate frequency (IF) signal, obtaining a free IF gain without extra power consumption. A peak detector circuit detects the receiving signal strength and auto-adjusts the biasing current to save power when a strong signal strength is detected. Meanwhile, the peak detector helps to provide a coarse gain control as part of the auto-gain-control function. As part of the IF gain range is shared by the multiple-feedback (MFB) low-pass filter, the number of programmable-gain IF amplifier stages can be reduced, which also means a decrease in power consumption. A prototype of this wireless sensor network (WSN) receiver was designed and fabricated using the TSMC 130 nm CMOS process under a supply voltage of 1 V. The entire receiver realizes a noise figure (NF) of 3.5 dB and a receiving sensitivity of −90 dBm for the 0.25 Mbps offset quadrature phase shift keying (O-QPSK) signal with a power consumption of 2.9 mW.

Keywords: RF receiver; low power; current reusing; function-reused mixing

1. Introduction

In today's handset wireless communication devices such as cell phones, handset GPS terminals, and wireless body sensors, achieving a low power consumption is the primary target to prolong the recharging cycle. In such devices, the RF receiver is among one of the most power-hungry modules. Therefore, low power design on RF circuits is crucial to decrease the power consumption of the entire device [1]. In a RF receiver, the low noise amplifier (LNA), power amplifier (PA), mixer, and voltage controlled oscillator (VCO) work in the RF frequency range and dominate the total power consumption. There are various techniques to improve the power efficiency of the above-mentioned building blocks proposed in previous studies, including current-reusing and function-reused structures. A typical example of a current-reusing structure is stacking the LNA and the mixer up and down between the supply voltage and the ground, sharing the DC biasing current [2–4]. The total power of the front end can be decreased by 50% compared with conventional techniques. However, as a result of limitation of the voltage headroom, the current generated by the LNA is directly injected into the mixer in most of the current-reusing front end. This leads to a deficient voltage gain in the absence of preamplification.

Besides the current-reusing technique, an alternative structure named the recursive mixer structure was introduced by [5,6]. The recursive mixer reuses the RF gm stage to amplify both the RF signal and the down-converted IF signal. Thus, the overall conversion gain can be boosted and takes the place of a traditional front end, which comprises an LNA and a mixer. However, without a preceding LNA, a high biasing current is needed for generating a relatively high transconductance to suppress the noise contributed by the mixer. In [7–10], the authors present receivers with state-of-the-art low-power techniques. The power consumption and performance are balanced in consideration of the application scenario. According to the latest publications, if a 13 dB NF is acceptable, a power consumption as low as 1.1 mW can be achieved [9]. However, when an NF less than 4 dB is required, more power consumption is necessary to guarantee high sensitivity. On this occasion, the typical power dissipation can be as high as 10 mW [7].

In this study, a RF receiver combining the current-reusing technique and function-reused mixing technique is proposed, as illustrated in Figure 1. The receiver front end is formed by the cascading of a current-reusing LNA and the mixer. Since the LNA provides a preceding voltage gain, both a high conversion gain and a low noise figure are achieved. With the LNA gain and the conversion gain, the mixer can be biased under a much lower DC current than the stacked current-reusing front end. Meanwhile, the LNA shares the bias current with the VCO, saving 50% in terms of power consumption compared with a traditional receiver with independent LNA and VCO, which are the most power-hungry modules. In transmitting mode, LNA is shut down and the PA turns on to share the current with the VCO. To avoid signal blocking under a strong input signal strength, a peak detecting circuit detects the receiving signal strength at the output of the mixer, and auto-adjusts the mixer's biasing current to adapt the upper limit of the mixer's output amplitude. When the input signal power is below −60 dBm, the biasing current of the mixer is automatically turned up by the analogue gain-control loop, and provides a high conversion gain to guarantee a sufficient signal-noise-ratio (SNR). The gain control scheme also helps to reduce power consumption by reducing the biasing current under a relatively strong input signal strength. After all, a low noise figure is not necessary to obtain the required SNR condition. The mixer itself performs a second-order filtering as a coarse channel selection. Besides that, a second-order Butterworth filter is used to provide a steeper, low-pass frequency selection for suppressing out-band interferences. In the programmable-gain amplifier, three AC-coupled fixed-gain amplifiers are used as coarse gain controls, and a negative feedback amplifier is used to perform fine gain control to achieve a precise output signal strength.

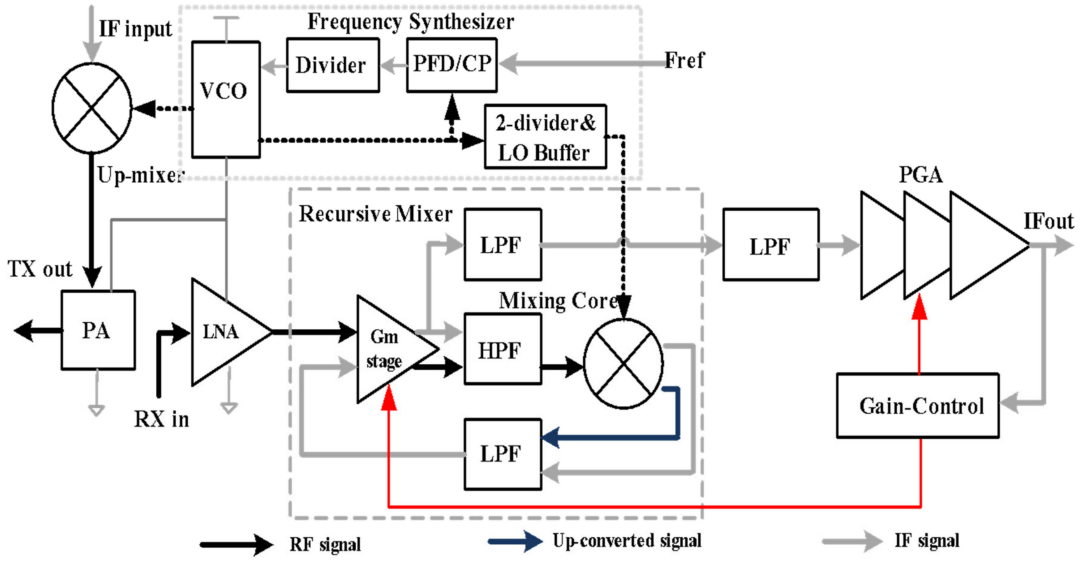


Figure 1. The system topology of the proposed recursive receiver.

Table 1 shows the systematic design and simulation results of the receiver modules. Performance indexes, such as NF, power consumption, gain and Input 3rd order intercept point (IIP3), are designed, balanced, and optimized. To achieve low NF, most of the power budget is assigned to the LNA and mixer. The NF of the LNA is 2.5 dB. The biasing current of the mixer is carefully chosen to be low enough not to impact the cascading NF of the entire receiver data link. To avoid signal blocking under strong signal strength and interferences, the receiver modules all have a low gain mode. The total out-of-band IIP3 can be higher than −15 dBm, which is acceptable according to the ambient environment estimation. For the systematic cascading of NF and the linearity estimation, the conventional formulas are given by Equation (1) and Equation (2). However, the modeling is far from accurate.

$$NF_{tol} = 1 + (NF_1 - 1) + \frac{NF_2 - 1}{A_{p,1}} + \cdots \frac{NF_N - 1}{A_{p,1} \cdots A_{p,N-1}} \quad (1)$$

$$\frac{1}{IIP3_{tol}} = \frac{1}{IIP3_1} + \frac{A_{v1}^2}{IIP3_2} + \frac{A_{v1}^2 A_{v2}^2}{IIP3_3} + \cdots \quad (2)$$

Table 1. Systematic design and simulation of the receiver modules.

Module	NF (dB)	Power Consumption (mW)	Low Gain (dB)	High Gain (dB)	HP-Freq (MHz)	LP-Freq (MHz)	OB-IIP3 (Low Gain) (dBm)
LNA	2.5	1.2	10	20	2300	2550	−5
Mixer	12	0.8	10	30	2400	2600	−5
LPF	30	0.3	0	0	0	3.5	10
PGA	28	0.3	12	48	0.2	10	10
Total	2.8	2.6 *	32	98	2400	2550	−15

* The power consumption of dividers and charge pump (CP) is excluded from the receiver data link budget.

Equation (1) gives the estimated NF in receiving systems. NF_{tol} is the equivalent cascaded noise figure of the entire receiver chain. NF_N represents the noise figure of the N_{th} stage. $A_{p,N}$ is the normalized power gain of the N_{th} stage. It is indicated that the NF of the front-end stages dominates the whole NF. Equation (2) shows the cascade formula of IIP3. $IIP3_{tol}$ is an equivalent cascaded IIP3 of the entire receiver. $IIP3_N$ is the IIP_3 of the N_{th} stage. A_{vN} is the voltage gain of each stage, which is also equal to the normalized power gain. Equation (2) reveals that the linearity of the back-end stages plays a more important role in realizing a high total IIP3.

2. Circuit Design

2.1. The Current-Reusing Structure

A schematic of the current-reusing structure is illustrated in Figure 2. The VCO is stacked on top of the LNA and PA to share the DC bias current. The joint node makes an AC ground by the decoupling capacitors, which are realized by gate-channel capacitance of the NMOS transistors, NM0 and NM1, to prevent interaction between the two modules. The VCO structure is a L-C-resonating (LC) oscillator with PMOS cross-coupling transistors. With the LC tank providing the peak load impedance and a 0° phase shift at the resonating frequency, the cross-coupling transistors, PM0 and PM1, start the oscillation and keep it going. The switched capacitors array is used to trim the frequency band. An AMOS varactor is connected between the differential terminals to provide continuous tuning of the oscillation frequency. The LNA is a single-ended-input and differential-output structure which is composed of a common-gate (CG) cascode amplifier and a common-source (CS) cascode amplifier with the same biasing current and transistor sizes. The input signal is fed to the source of a CG transistor N1 and to the gate of a common-source transistor N2, simultaneously. The CG stage also provides impedance matching between the input terminal of the LNA and the signal source. An LC resonating tank is used at the input terminal to provide a DC path to the ground for the biasing current and also

performs band-pass filtering. The parasitic capacitance induced by the chip bounding and package pin is also neutralized.

The CS and CG gain stages provide both voltage amplification and single-to-differential conversion. When a high input signal strength is applied, the gain-control switch between the differential pair of the LNA is turned on to prevent distortion.

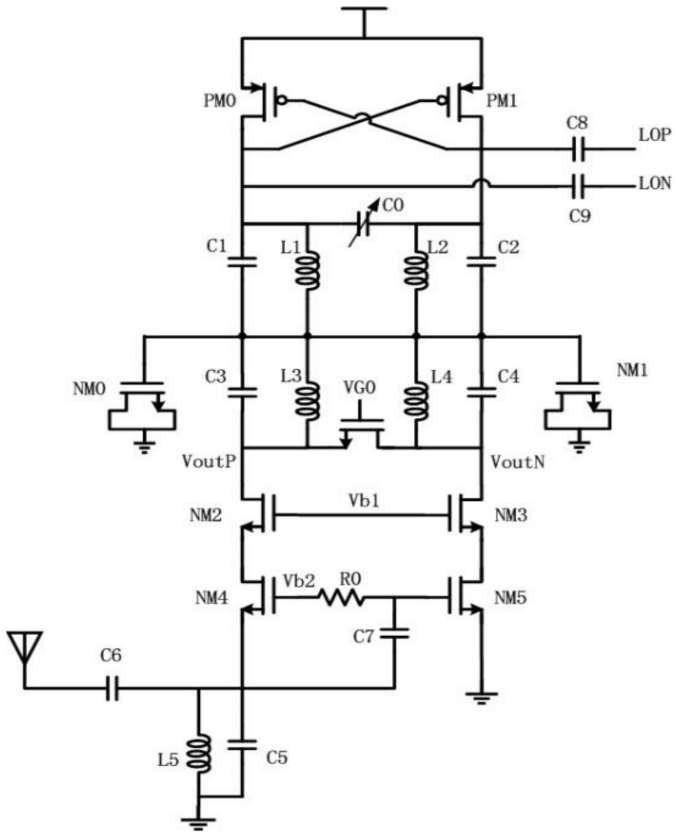


Figure 2. Circuit schematic of the current-reusing structure of the low noise amplifier (LNA) and voltage controlled oscillator (VCO).

2.2. The Function-Reused Mixer

This study proposes a function-reused mixer with a reconfigurable gm stage which aims to improve the linearity of the reused IF amplifier. For a traditional recursive mixer, the RF gm stage is also used to amplify the down-converted IF signal [5,6]. In consideration of the voltage gain and bandwidth, the gm stage for the RF signal is mostly an open-loop structure with insufficient linearity. Reused as the recursive gain stage for the IF signal, the gm stage limits the linearity of the mixer. For the purpose of improving the linearity of the IF gain while maintaining sufficient RF gm, a function-reused mixer structure combined with the self-reconfigurable gm stage is designed. With the low-pass and high-pass coupling networks and feedback networks, the gm stage is an open-loop common-source topology for the input RF signal, and the closed-loop negative feedback amplifier for the IF signal. The self-reconfigurable structure also provides sufficient signal isolation between RF and IF signals, keeping the loop gain for the entire frequency range well below 0 dB. An auto-gain-control circuit is designed to set the upper-limit of the mixer's output amplitude to the preset value. The peak detector extracts the peak value of the mixer's output amplitude and stores it on a capacitor. The gain-control voltage generated by the error amplifier is applied to the gate of NMOS transistors which are used as the source-degenerated resistors. The resistance variance causes the gm stage to adjust to the biasing current, achieving continuous gain control to the mixer. If the input signal strength is well below the reference level, the error amplifier outputs a control voltage close to the supply voltage and sets

the biasing current to the maximum. When the input power increases to exceed the gain-adjusting threshold, the source-degenerated resistance is automatically adjusted by the gain-control loop to set the output amplitude equal to the reference voltage. The gain-control scheme automatically optimizes the biasing current of the mixer according to the receiving signal strength, or in another words, the SNR. When a large received signal power is detected, the biasing current is reduced to save power by degenerating the conversion gain and noise performance.

A schematic of the mixer is illustrated in Figure 3. The gm stage is a CMOS cascode structure which provides sufficient open-loop voltage gain for the IF signal. The RF signal is applied to the gate of MP1, MP5, and MN1 by coupling capacitors C3, C1, and C9. The degenerated resistance is decoupled by the capacitor MN7, which improves the effective gm for RF signal. The generated RF current is coupled into the switching pair by C5 and C7. For the RF signal, C7 and C5 short the source terminal and drain the terminal of the cascode transistor MP3. The phase deviation caused by the common gate transistor MP3 is eliminated. In order to improve the noise performance, the DC biasing current of the switching pair is set by MP5 and is lower than the biasing current of the gm stage. The switching pair commutates the input RF current and converts it into an IF current. The up-conversion outcomes are eliminated by the filtering capacitors C13, C11, and C12. The self-biasing load converts the IF current into IF voltage. For IF signals, the impedances of the coupling capacitors C1, C3, C5, C7, and C9 are much higher than the resistors R5 and R9 in the feedback branch. Seen from the output of the mixer-stage (MOP) to the output node (IFP), the gm stage becomes a recursive IF amplifier with negative feedback. Because of the high open-loop gain of the cascode gm stage, the closed-loop gain of the recursive IF amplifier is set by the resistance ratio of R5 and R9. A first-order RC network is added to the nodes of IFP and IFN, isolating the RF signal at the output of the gm stage from the final output IF signal.

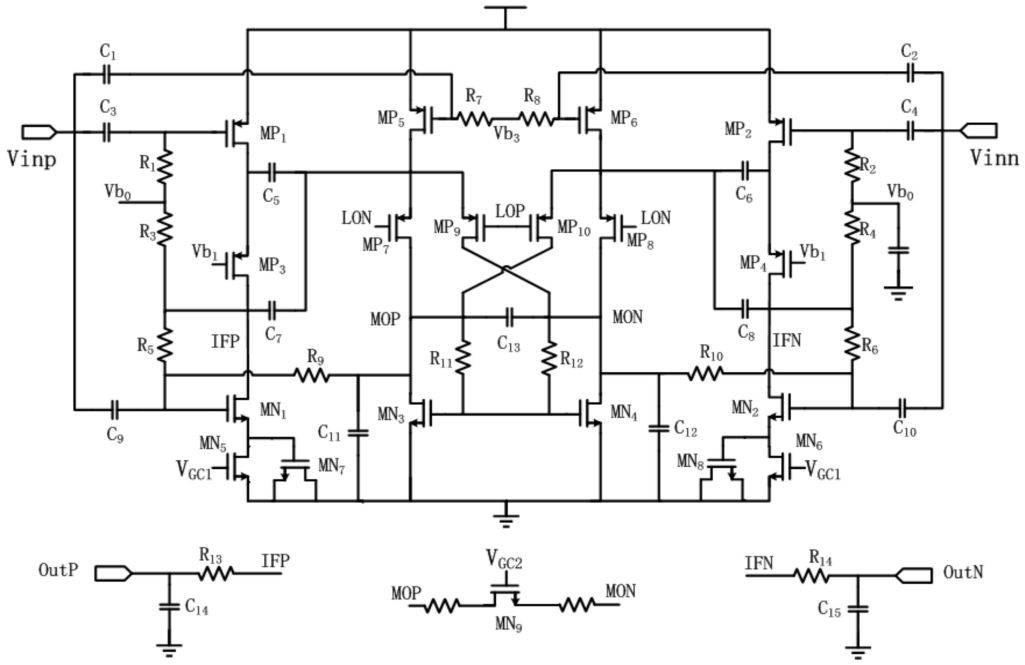


Figure 3. The circuit schematic of the proposed function-reused mixer.

The conversion gain of the function-reused mixer is indicated in Equation (3). It shows that compared with a traditional folded mixer, an additional IF gain of R_5/R_9 is obtained without extra

power consumption. Meanwhile, compared with previous recursive mixers, the IF gain is obtained by a close-loop amplifier, which gives higher linearity.

$$A_{CG} = \frac{2}{\pi} \cdot \left(g_{mp1} + g_{mp5} + g_{mn1} \right) \cdot R_{11} \cdot \frac{R_5}{R_9} \tag{3}$$

The stability of the mixer with a recursive loop is also an important concern. Theoretically, the double-balanced switching pair converts the RF signal to IF and RF + local oscillator (LO) frequency, eliminating any possibility of self-oscillation. However, the feed through between the source and drain terminals of the switching transistors can induce remixing and generates spurious outputs. Thanks to the large distance between the corner frequencies of the low-pass and the high-pass networks, the voltage gain at spurious frequencies are suppressed. The simulated loop-gain versus input frequency at the LO frequency of 2.4 GHz is shown in Figure 4. It is indicated that the loop gain is well below −20 dB for the entire frequency band. Frequency stability is guaranteed.

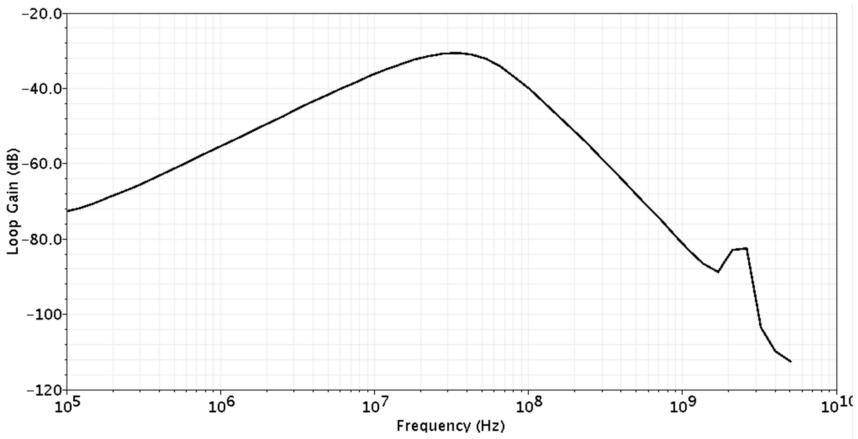


Figure 4. Simulated loop gain versus frequency at the LO frequency of 2.4 GHz.

The self-reconfigurable gm stage provides high linearity for the IF gain, which has a minor impact on the overall linearity. Figure 5 shows the simulated IIP3 curves with and without the recursive IF gain. The simulated IIP3 values are −15.6 dBm and −14.8 dBm, which are much closer to each other. It is also indicates that the recursive IF amplification offers an additional 15 dB to the conversion gain without damaging the overall linearity.

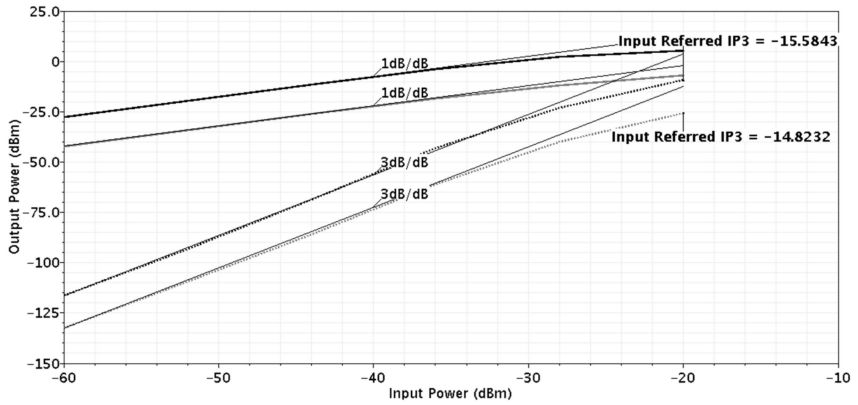


Figure 5. Simulated IIP3 curves with and without the recursive IF amplification stage.

2.3. The IF Modules

In the receiving chain, a filter is necessary to select the target signal and to remove the unwanted channels and interference signals. In this design, the mixer provides near-second-order low-pass filtering characteristics. To obtain sufficient out-band rejection, a separated second-order multiple-feedback (MFB) Butterworth filter is added in cascade with the mixer. To avoid the interaction between the RC networks in the mixer and the filter, a voltage buffer is connected between the two modules. The programmable gain amplifier (PGA) is constructed using the coarse-adjustment gain stage and the fine-adjustment gain stage, as shown in Figure 6. The coarse-adjustment gain stage is made of three fixed-gain stages as shown in Figure 7. In the fixed-gain stages, the signal AC is coupled between two adjacent stages. Three pairs of by-pass switches are employed in each stage to set the voltage gain to 0 dB, 12 dB, 24 dB, and 36 dB. The by-passed gain stages are shut down when a voltage gain lower than 36 dB is chosen. The fine-adjustment gain stage is made of a class-AB output operational trans-conductance amplifier (OTA). The gain-control range is from 0 dB to 12 dB with the step of 1 dB. The gain is controlled by adjusting the feedback factors. A feedback resistor array is employed with 13 branches to cover the 13 gain modes. Since the fixed-gain stage is open loop in its structure, the high output impedance makes it improper to drive R0 which is the input resistor of the fine-adjustment gain stage. To cope with the driving issue, a voltage buffer is added. The voltage buffer is based on the differential-input single-ended-output OTA structure with its negative input terminal connected to the output node.

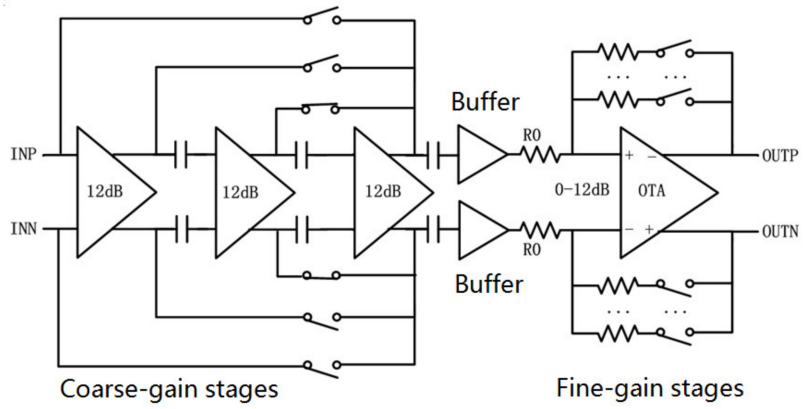


Figure 6. The topology of the programmable gain amplifier.

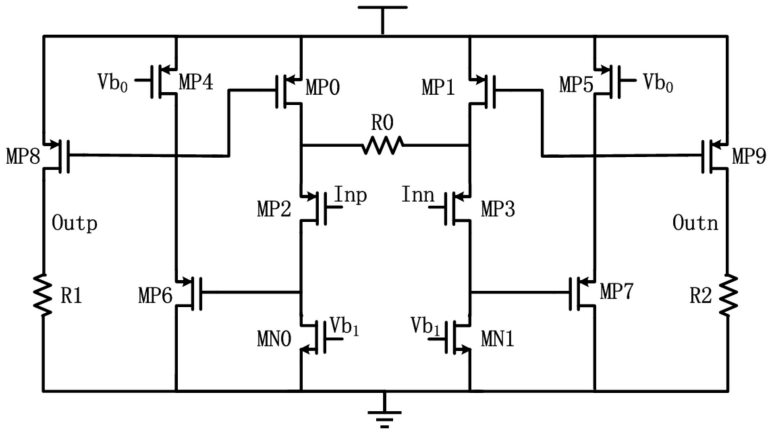
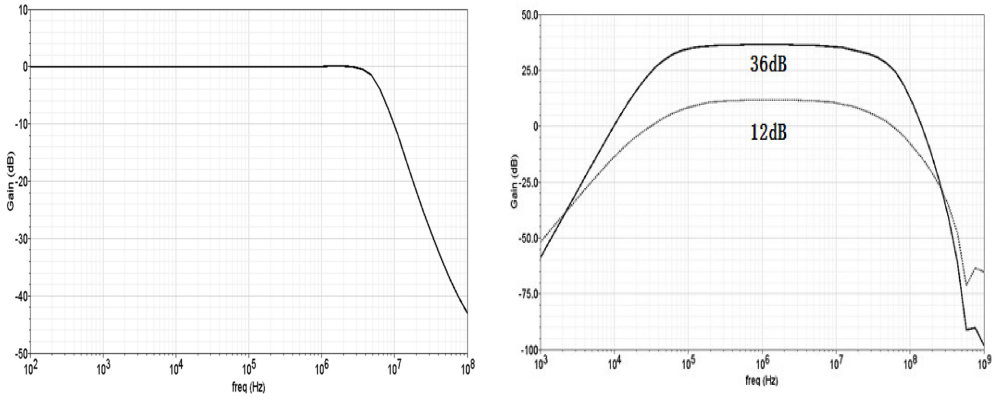


Figure 7. The circuit schematic of the fixed-gain stage.

Figure 8 shows the simulated AC response of the low pass filter (LPF) and the PGA. The in-band response is very flat thanks to the Butterworth characteristic. The 1 dB bandwidth is 3.5 MHz which is slightly higher than the right border of the Zigbee channel. The phase margin of the feedback loop

in the MFB LPF is around 65 degrees, diminishing the up-warping of the AC response around the passing-bandwidth. The AC response of PGA shows typical band-pass characteristics; the high-pass and low-pass frequencies are 80 KHz and 20 MHz, respectively, which can safely cover the Zigbee channel from 1 MHz to 3 MHz.



(**a**) (**b**)

Figure 8. (**a**) The simulated AC response of the LPF. (**b**) The simulated AC response of the programmable gain amplifier (PGA) in different gain modes.

3. Experimental Results

The prototype of the receiver is designed and fabricated in a TSMC 130 nm CMOS process under a supply voltage of 1 V. The microphotograph of the prototype chip is illustrated in Figure 9. The entire die area of the transceiver is 1 mm × 2 mm, among which the active area of the proposed low power receiver including the LNA, the mixer, the filter, and the PGA is 0.7 mm^2. The entire receiver achieves a receiving sensitivity of −90 dBm and an NF of 3.5 dB with a power consumption of 2.9 mW.

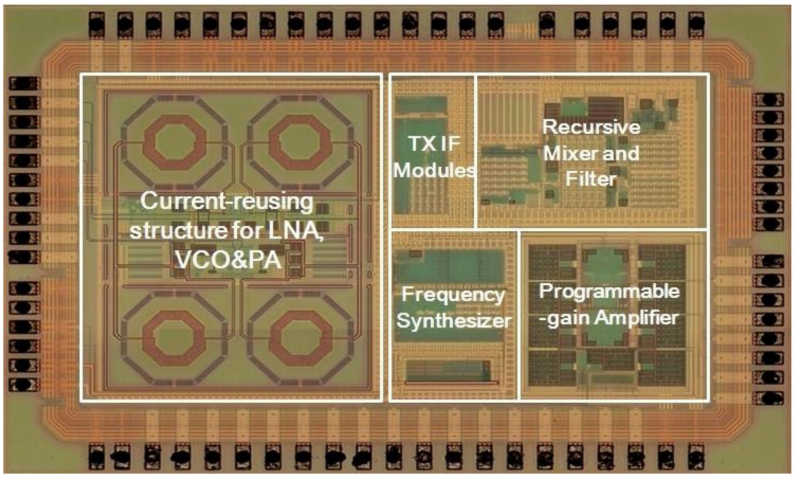


Figure 9. The microphotograph of the proposed receiver.

The testing signal is generated by an Agilent E4438C, which is programmed to output a modulated 2.4 GHz Zigbee applicable O-QPSK signal. The received signal tested at the PGA's output terminal is captured by an oscilloscope Agilent MS08104A. The input signal strength is manually scanned to investigate the dynamic range of the receiver. The digital vector signal analyzer software 89600 vector-signal analyzer (VSA) implements the demodulation process and outputs the received data and constellation graph.

Figure 10 shows the measurements of the out-of-band IIP3 and output 3rd order intercept point (OIP3) under two-tone test procedures at the LO frequency of 2.4 GHz. The input frequencies are located 20 MHz away from the LO frequency, with a center frequency of 2 MHz and a frequency interval of 500 KHz. In this figure, a −16 dBm IIP3 and a 13.8 dBm OIP3 are observed. The IIP3 value is limited by the relatively high conversion gain. Thanks to the self-reconfigurable gm stage which provides sufficient linearity IF gain, a relatively high OIP3 is achieved.

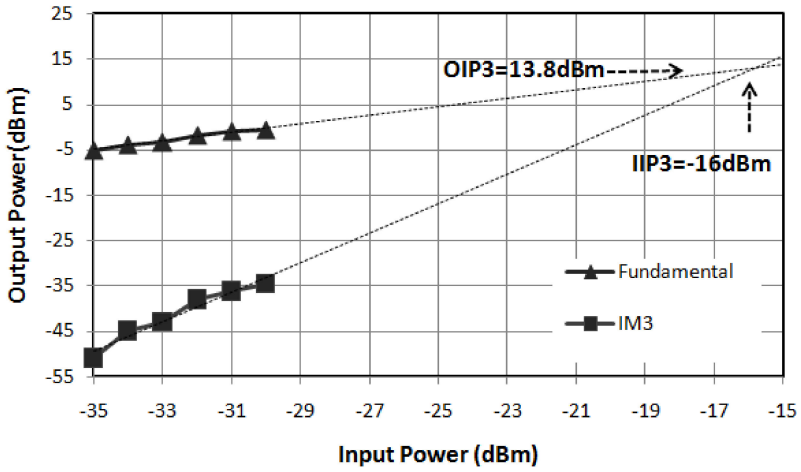


Figure 10. Measured out-of-band IIP3 and OIP3 at the LO frequency of 2.4 GHz.

The NF versus input frequency curve is shown in Figure 11. Thanks to the LC impedance transforming network which provides a 7 dB passive gain, a low noise figure is obtained with a relatively low biasing current. The output IF frequency is fixed at 2 MHz by scanning the LO frequency and the input frequency. The measured NF curve is very close to the simulated curves with a deviation of less than 0.5 dB. The lowest NF is 3.5 dB at 2.41 GHz. A NF of 3.8 dB is obtained at 2.49 GHz.

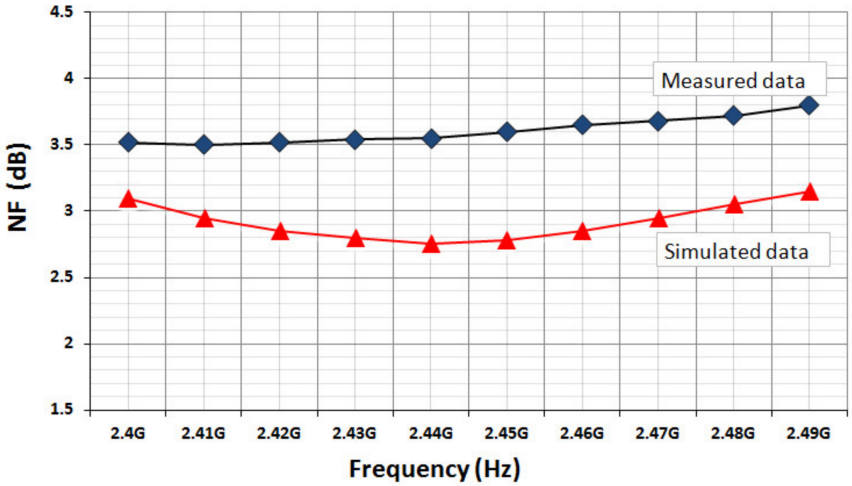
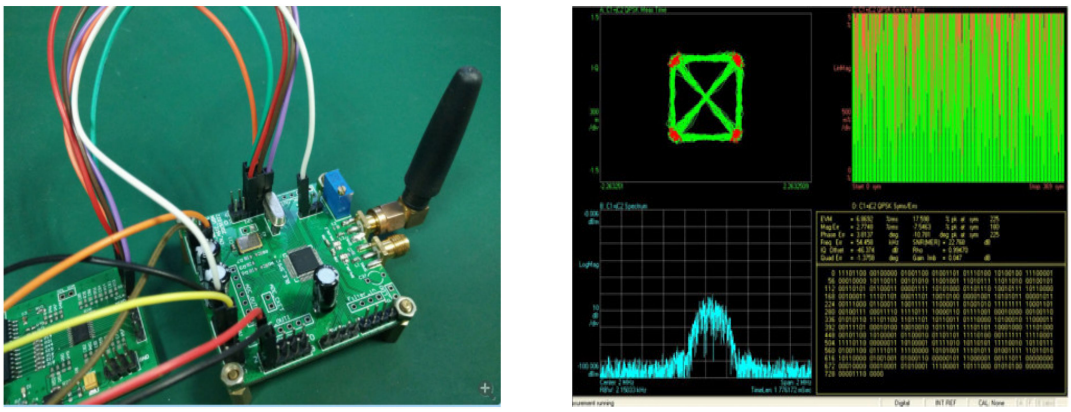


Figure 11. Measured and simulated NF versus input frequency with a fixed IF frequency of 2 MHz.

Figure 12a shows the testing board with the proposed receiver chip mounted on. Figure 12b indicates the output signal waveform of the PGA at an IF frequency of 2 MHz, under the input signal strength of −80 dBm. The analogue signal bandwidth and the data rate is 2 MHz and 0.25 Mbps, respectively. The signal is demodulated by the Agilent software 89600 VSA.



(**a**) (**b**)

Figure 12. (**a**) The testing board of the proposed receiver. (**b**) The received signal at an IF frequency of 2 MHz with 250 kbps O-QPSK measured by Agilent 89600 VSA.

The performance comparisons with other reported work are shown in Table 2. The previous examples listed are state-of-the-art RF receivers in a similar frequency band. This work and the work in [7] and [8] have an intact LNA as the first stage, which is helpful to achieve a low NF of the whole receiver. In [9] and [10], the designs have a merged LNA and mixer, which reuses the biasing current at the cost of noise performance. This design has an independent LNA before the mixer while realizing current reusing at the same time, achieving both low NF and low power consumption. Compared with the other works, the receiver proposed in this work shows the lowest supply voltage and the power consumption is lower than in [7,8,10]. Although the work in [9] achieves a lower power consumption, the noise performance and conversion gain are inferior to those in previous work. Because of the high linearity recursive IF gain, the proposed receiver shows high conversion gain, high linearity, and low power consumption at the same time. It has benefited from the extra conversion gain with no additional power consumption or penalty to the linearity; a high figure of merit (FoM) of 26 is achieved.

Table 2. Performance comparison of the proposed recursive mixer with other reported work.

	[7]	[8]	[9]	[10]	This Work
Frequency (GHz)	3–10.6	2.4	2.4	1–10	2.4
Supply voltage (V)	1.2	1.8	1.2	1.2	1
Conversion Gain (dB)	20.6	35.6	20.5	8	45
OB-IIP3 (dBm)	−8.5	−31	−7.8	−4	−16
NF (dB)	3.4	5.8	13.2	11.3	3.5
Power (mW)	10.8	9	1.08	8.4	2.9 *
Chip area (mm^2)	0.91	-	1.69	0.28	0.7 **
FoM *	17	12	18	6.5	26 ***

* The power consumption of the frequency synthesizer is included. ** The transmitting (TX) mode and Frequency Synthesizer are excluded in the chip area evaluation. *** The FoM is defined by the prevalent format: $FoM = 10log\left(\frac{10^{\frac{G}{20}} \cdot 10^{\frac{(IIP3-10)}{20}}}{10^{\frac{NF}{20}} \cdot P}\right)$.

4. Conclusions

This paper proposes a low-power Zigbee receiver with a current-reusing LNA/PA and VCO stacked structure and function-reused mixer to reduce the overall power consumption. In the receiver, the LNA and PA share the biasing current with the VCO in the RX mode and TX mode, respectively. The mixer reuses the RF gm stage to amplify the down-converted IF signal, obtaining a free IF gain without extra power consumption. A prototype of this WSN receiver was designed and fabricated in a TSMC 130 nm CMOS process under a supply voltage of 1 V. The entire receiver realizes a NF of 3.5 dB

and achieves a sensitivity of −90 dBm for the 0.25 Mbps O-QPSK signal with a power consumption of 2.9 mW.

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Conflicts of Interest: The authors declare no conflict of interest.

References

1. Larson, L. RF and microwave hardware challenges for future radio spectrum access. *Proc. IEEE* **2014**, *102*, 321–333. [CrossRef]
2. Liscidini, A.; Mazzanti, A.; Tonietto, R.; Vandi, L.; Andreani, P.; Castello, R. Single-Stage low-power quadrature RF receiver front-end: The LMV cell. *IEEE J. Solid State Circuits* **2006**, *41*, 2832–2841. [CrossRef]
3. Ghosh, D.; Gharpurey, R. A low-power receiver down-converter with high dynamic range performance. In Proceedings of the 2010 IEEE Radio Frequency Integrated Circuits Symposium, Anaheim, CA, USA, 23–28 May 2010; pp. 35–38.
4. Lin, Z.; Mak, P.I. A 2.4 GHz ZigBee receiver exploiting an RF-to-BB-current-reuse blixer + hybrid filter topology in 65 nm CMOS. *IEEE J. Solid State Circuits* **2014**, *49*, 1333–1344. [CrossRef]
5. Han, J.; Gharpurey, R. Recursive receiver down-converters with multi-326 band feedback and gain-reuse. *IEEE J. Solid State Circuits* **2008**, *43*, 1119–1131. [CrossRef]
6. Lin, Z.; Mak, P.I.; Martins, R.P. A Sub-GHz multi-ISM-band ZigBee receiver using function-reuse and gain-boosted N-path techniques for IoT applications. *IEEE J. Solid State Circuits* **2014**, *49*, 2990–3004. [CrossRef]
7. Simitsakis, P.; Papananos, Y. Design of a low voltage-low power 3.1–10.6 GHz UWB RF front-end in a CMOS 65 nm technology. *IEEE Trans. Circuits Syst. II* **2010**, *57*, 833–838. [CrossRef]
8. Aaron, V.D.; Chirn, C.B. An energy-aware CMOS receiver front end for low-power 2.4-GHz applications. *IEEE Trans. Circuits Syst. I* **2010**, *57*, 2675–2685.
9. Lee, S.Y.; Wang, L.-H.; Chen, T.-Y.; Yu, C.-T. A low-power RF front-end with merged LNA, differential power splitter, and quadrature mixer for IEEE 802.15. 4 (ZigBee) applications. In Proceedings of the 2012 IEEE International Symposium on Circuits and Systems—(ISCAS), Seoul, Korea, 20–23 May 2012; pp. 937–940.
10. Hu, Z.; Koen, M.A. 1–10 GHz RF and wideband IF cross-coupled Gilbert mixer in 0.13-µm CMOS. *IEEE Trans. Circuits Syst. II* **2013**, *60*, 726–730.