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Article

Low Power 24 GHz *ad hoc* Networking System Based on TDOA for Indoor Localization

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Abstract: This paper introduces the key elements of a novel low-power, high precision localization system based on Time-Difference-of-Arrival (TDOA) distance measurements. The combination of multiple localizable sensor nodes, leads to an *ad hoc* network. Besides the localization functionality this *ad hoc* network has the additional advantage of a communication interface. Due to this a flexible positioning of the master station for information collection and the detection of static and mobile nodes is possible. These sensor nodes work in the 24 GHz ISM (Industrial Scientific and Medical) frequency range and address several use cases and are able to improve various processes for production scheduling, logistics, quality management, medical applications and collection of geo information. The whole system design is explained briefly. Its core component is the frequency modulated continuous wave (FMCW) synthesizer suitable for high performance indoor localization. This research work focuses on power and size reduction of this crucial system component. The comparison of the first and second generation of the system shows a significant size and power reduction as well as an increased precision.

Keywords: fmcw; tdoa; *ad hoc* networking; pll; synthesizer; tspc; frequency divider

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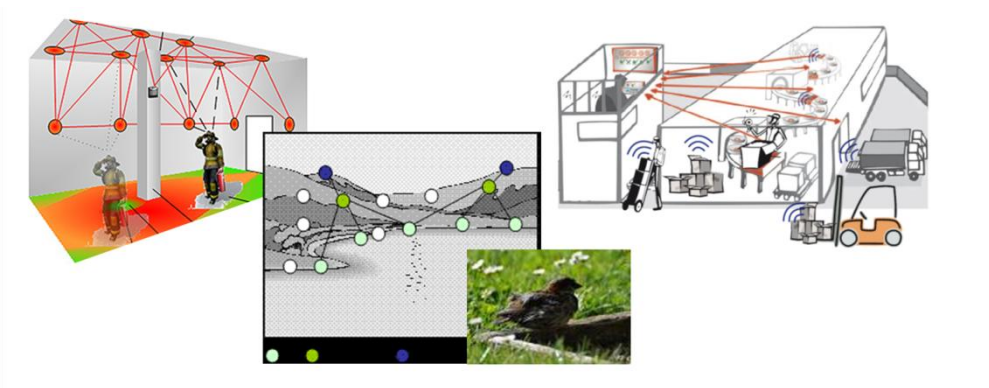
1. Introduction

Indoor local positioning systems have become very popular in recent years. Similar to the evolution of wireless communication systems, the variety, functionality and performance of indoor localization systems are increasing. A wide field of usability in medical, industrial, logistics, transportation systems and collection of geo information is possible (Figure 1). Due to small system sizes tracking of people, animals, industrial goods, machinery and other production equipment, as well as mapping of buildings are possible applications of the presented system. The system is available for collecting positioning information in difficult areas like caves, crevices and densely forested areas, where the GPS signal is not able to deliver information. Due to its structure with communication ability, sensors for humidity, temperature, air quality, *etc.* can also be added to the system. The information can be collected in the system and transferred from the sensor nodes to a master station. Localization data not only allows diverse applications but also requires highly accurate and energy efficient localization sensors with minimized costs and a highly integrated structure. In this context, Frequency Modulated Continuous Wave (FMCW) radar, based on the Time-Difference-of-Arrival (TDOA) technique, enables spectral efficient and accurate positioning. There are plenty of available ISM (Industrial, Scientific and Medical) frequency bands [1]. In order to mitigate possible interference issues with other wireless systems, it is beneficial to choose the less crowded 24 GHz ISM band.

Figure 1. Illustration of the possible application of the sensor system.



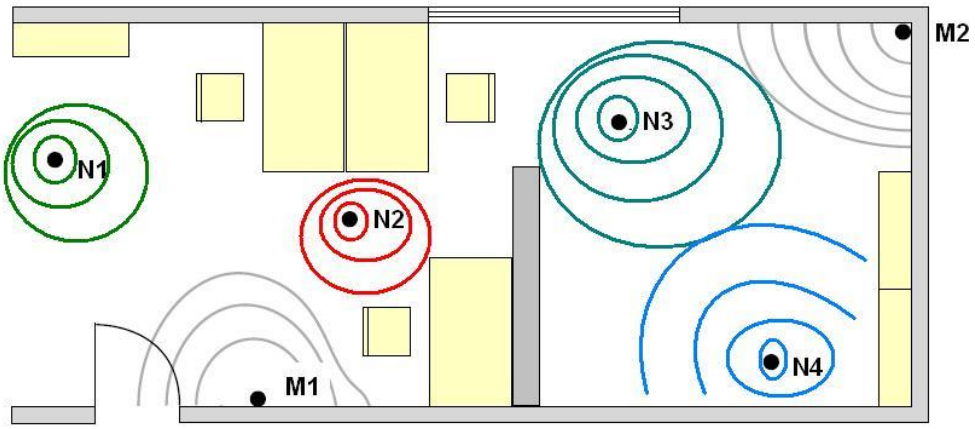
Although high performance is a key element, low power consumption of the systems is even more appreciated. In order to reach the power efficiency goals, new system architectures and components for the sensor nodes are necessary. The presented work focuses on the demand of small and low power sensor systems for *ad hoc* networking. The system and its key features are presented. The power saving potentials with application specific integrated circuits (ASIC) are shown on the example of the synthesizer, which is the core component of the localization system.

2. Localization Using Time-Difference-of-Arrival (TDOA)

Localization systems based on Global Navigation Satellite Systems (GNSS) such as GPS are well known and have penetrated our daily life. These systems reach their limits when operating indoors or when higher localization accuracy is required. In these scenarios applications can benefit from the use of wireless sensor nodes with localization capability. Figure 2 shows a typical application example.

The room is separated by a wall, and furniture is reflecting and absorbing the signal. The master stations M1 and M2 are mounted on known positions inside the room. The nodes N1 up to N4 are moving targets. As the sensor nodes can measure the distance to the other nodes and to the master station their position inside the room can be calculated.

Figure 2. Illustration of wireless sensor network with possible applications.



Linear frequency modulation of a continuous wave signal is an ideal approach to localization in wireless sensor networks. This system concept allows a precise localization with moderate circuit complexity. For integration of radar systems in a modern semiconductor technology, a FMCW radar approach is much more suitable compared to a pulse radar based approach. With modern deep sub-micron silicon technology, the maximum achievable output power of the transmit signal is limited. Thus the ratio of the maximum to the average transmission power is a critical system parameter. This ratio is considerably greater in FMCW systems than in pulse radar systems. As a result, a much greater range for the same maximum transmit power is reached. A low-power implementation of the RF circuitry and the analog signal processing is feasible for FMCW systems. Furthermore, a significantly higher spatial resolution compared to pulse radars with the same circuit complexity is possible. The digital signal processing and the detection of individual objects is performed with a Fast Fourier Transform (FFT) and is therefore also realizable with low cost and low power consumption in an integrated circuit.

The core component of the FMCW system is the frequency synthesizer, which generates the necessary frequency ramps. The instantaneous output frequency of the transmitted signal f is given by the start frequency f_0 and the slope μ of the frequency ramp, which depends on the bandwidth B and the time τ for the chirp:

$$\begin{aligned} f &= f_0 + \mu t \\ &= f_0 + \frac{B}{\tau} t \end{aligned} \quad (1)$$

For distance calculation between the nodes the transmitted and the received signals are mixed. The frequency difference is directly proportional to the distance between the sensor nodes.

For position determination by means of the Roundtrip-Time-of-Flight (RTOF) or the Time-of-Arrival (ToA) method, the fixed baste stations (BS) and the mobile stations (MS) must be

synchronized with each other. The higher the required accuracy, the greater the demands on the synchronization of the time bases for all participants. The used TDOA method has the advantage that only the BS must be synchronized with one another. No synchronization takes place between the MS and the BS or among the MS. The MS sends out a signal which is received by several BS. One BS serves as a reference node for all other. For position determination the absolute time-of-flight is not necessary. Instead, the difference of the time-of-flight between the i-th BS and the reference BS is used to calculate the position. The measurements of the signal propagation time between the MS t'_i and the i-th BS are received at a central node in the infrastructure, where the calculation of the position of each MS takes place. Each measurement provides a time t'_i which is composed of the actual time of flight of the signal t_i, and a time offset t_{Offset}:

$$t'_i = t_i + t_{\text{Offset}} \tag{2}$$

The calculation of the time difference t_{12} between BS 1 and BS 2 is based in the measured times t'_1 between BS 1 and MS and from t'_2 between BS and MS 2. Since all BS are synchronized, the offset t_{Offset}, i is the same for all BS:

$$\begin{aligned} \Delta t_{12} &= t'_2 - t'_1 \\ &= t_2 + t_{\text{Offset2}} - (t_1 + t_{\text{Offset1}}) \\ &= t_2 - t_1 \end{aligned} \tag{3}$$

The synchronization between the fixed nodes relies on the work presented in [2]. The concept for high precision clock synchronization relies on a concept similar to the standard FMCW (frequency-modulated continuous wave) radar principle and is used to estimate the offset in time and in frequency between two sensor nodes.

3. System Design

The following system focuses on an active sensor node with localization ability at 24 GHz with a chirp bandwidth of 250 MHz. The high bandwidth has the benefit of an increased precision and less susceptibility to multipath effects compared to the 2.45 GHz [3] or the 5.8 GHz [4] ISM band. The following chapter compares the system before and after the improved hardware design, which is necessary to reach the goals for size and power reduction without loss in accuracy.

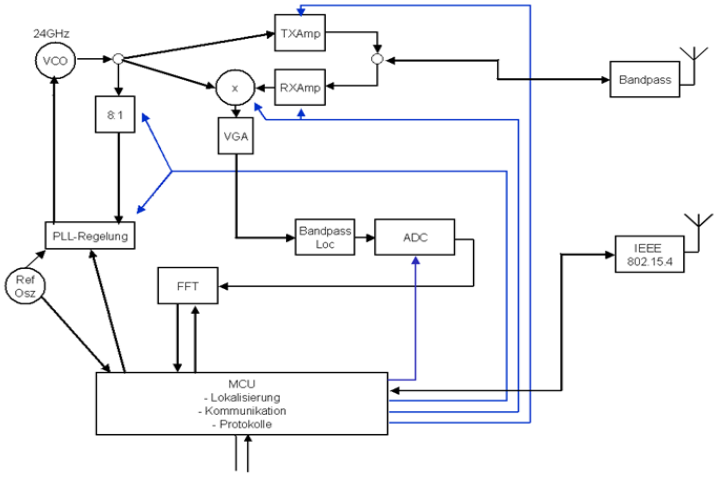
3.1. System Overview

The focus of the presented system (Figure 3) lies on a miniaturized wireless sensor system with localization in the 24 GHz ISM-band. An additional wireless connection between the nodes for *ad hoc* data transfer is also part of the system and simplifies the information exchange between sensor nodes. The use of the 24 GHz ISM band avoids interference issues at the lower frequency bands. Furthermore the high bandwidth is beneficial for radar localization in terms of spatial resolution.

Besides the efficient algorithms for the calculation of distance, this research focuses on high precision front-end components with high system integration in combination with low power consumption. The applied FMCW based Fractional-N synthesizer concept is less power hungry compared to conventional Direct Digital Synthesizer (DDS) based systems. The classical synthesizer

concept for precise FMCW frequency ramps relies on a DDS circuitry for ramp generation. This block delivers the time varying reference frequency for an integer-N PLL. The PLL acts as a frequency multiplier. In our concept a fixed reference frequency is used. The frequency chirp is solely generated by a continuous variation of the frequency divider values, which is controlled by a digital ΔΣ-modulator and an additional finite state machine. The DDS in the classical concept has a power consumption of about 400 mW. It is replaced with the mentioned digital circuitries which only need 2 mW from a 1.5 V supply rail. Due to this, the power consumption of the FMCW synthesizer is reduced by about 90%.

Figure 3. Schematic of the proposed 24 GHz localization system.

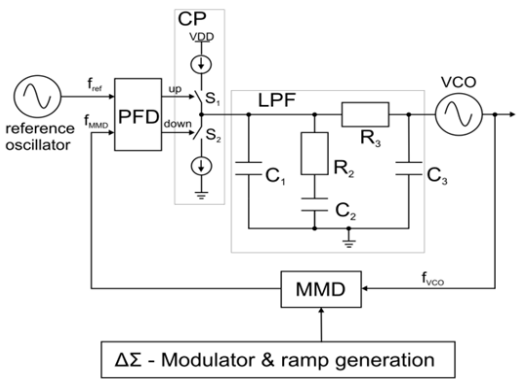


The synchronization between the nodes and the distance measurement is performed by a multi-step approach. Details of the used methodology are shown in [5–7].

3.2. Synthesizer Concept

A synthesizer with a 24 GHz voltage controlled oscillator (VCO) and a phase-locked loop (PLL) is the key element of the sensor node. The 24 GHz VCO is the contribution of a partner in the project consortium. The fractional-N PLL (Figure 4) consists of the phase-frequency detector (PFD) connected to a charge-pump (CP), a third order loopfilter (LPF), the multi modulus divider (MMD) and a digital building block including the ΔΣ-Modulator and a state machine for the ramp generation.

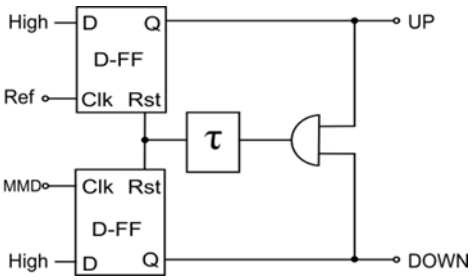
Figure 4. Schematic of the proposed 24 GHz FMCW Synthesizer.



3.2.1. Phase-Frequency Detector

The PFD compares the phase and frequency of the divided VCO signal with the reference frequency. Depending on the transitions of the input signals, the PFD generates UP and DOWN pulses, which trigger the charge-pump (CP) current sources. Figure 5 shows the PFD circuit, realized with two edge-triggered D flip-flops, an AND gate and a delay τ to prevent the dead zone. The D inputs of the D-FFs are tied to logic high input levels. The flip-flops are clocked by the output signal of the MMD and the reference clock respectively. The output signals UP and DOWN are connected to a logic AND-gate. The result is delayed by the delay element and then used to reset both flip-flops.

Figure 5. Schematic of the Phase-Frequency Detector.



3.2.2. Charge Pump

The basic charge pump structure consists of two MOS-Transistors as current sources. This concept has matching discrepancies and tolerances during the fabrication of the integrated circuit lead to non-idealities and degrades the overall system performance. Another problem is the clock-feed through of the reference frequency. This problem is especially severe at high reference frequencies above 100 MHz. Both effects lead to increased spurs in the output spectrum of the synthesizer. Only with an improved charge pump design can the expected system accuracy be realized.

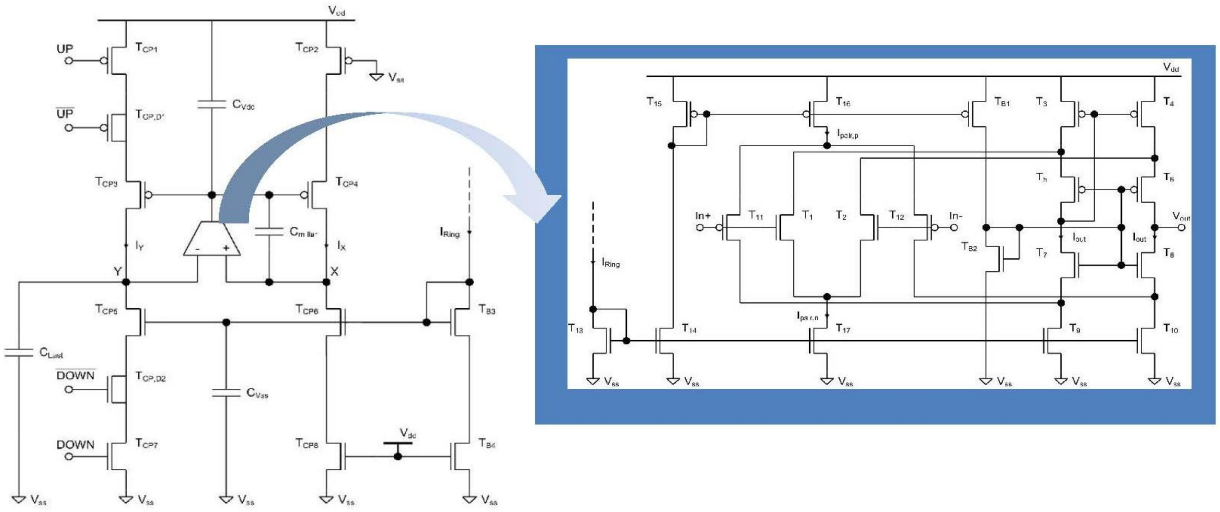
3.2.3. Improved Charge Pump Design

The structure of the improved charge pump design is given in Figure 6. This charge pump consists of the basic structure with changed position of the switching transistors, an transconductance amplifier and additional transistors $T_{CP,D}$ for the cancellation of charge injection [8]. The switching transistors T_{CP1} and T_{CP7} are placed at the rails and the transistors T_{CP3} and T_{CP5} act as current sources. The charge compensation transistors between the switches and the current sources compensate the charge injection from the switches into the current sources. An inverse DOWN and UP signal is necessary to drive the compensation transistors. This inverse clock is generated with respect to the PFD delay between the inverted and non-inverted UP and DOWN signals to achieve two non-overlapping clock signals. By use of these transistors, it is possible to significantly reduce the clock-feed through at high reference clock speeds.

Another enhancement of this structure is the use of an operational transconductance amplifier (OTA) to regulate the current mismatch between the UP and DOWN current sources. The OTA is placed in a feedback loop between the output node Y and the reference node X at the input and the gate of the current source transistors T_{CP3} and T_{CP4}. The node X is the reference for the output voltage.

The feedback loop ensures that I_{CP4} always equals I_{CP3} and thus also the output current of the charge pump. Thereby it is possible to ensure the same drain-source voltage across the current sources and to minimize the current mismatch between the UP and DOWN sources.

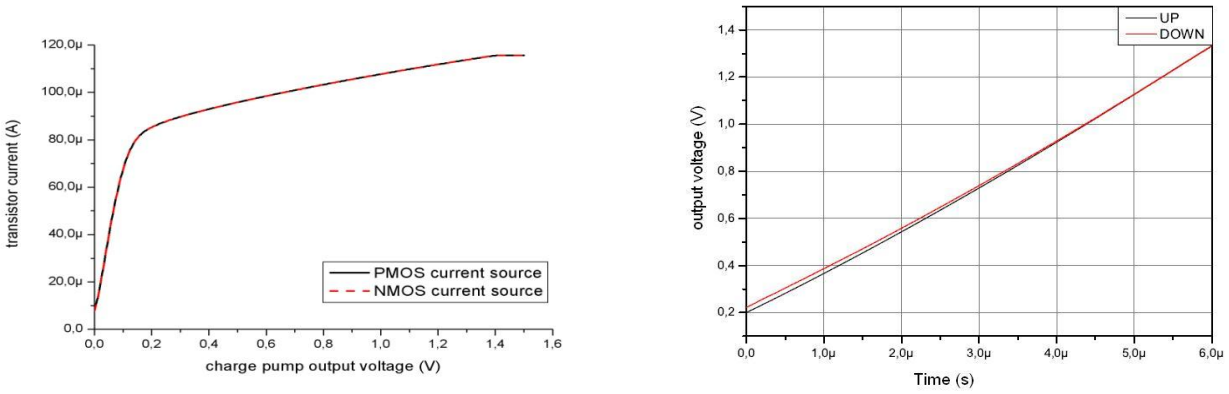
Figure 6. (**a**) Structure of improved chargepump. (**b**) and the used operational transconductance amplifier (OTA).



The structure of the operational transconductance amplifier is shown in Figure 6b. A rail-to-rail differential input stage is used. A high input voltage range is required to ensure that the output voltage range of the charge pump is not restricted by the OTA. To reach the necessary gain for a fast regulation of the difference voltage between the nodes X and Y, the output stage of the OTA is realized with a folded cascode stage. For the biasing of the cascode transistors, a MOSFET T_{B2} in diode connection is used. Other biasing structures are also possible, but for this use a gain variation due to process variations is tolerable [9]. The capacitors C_{Vss} and C_{Vdd} are used to stabilize the gates of the current sources against fast voltage drops due to switching effects. The capacitance C_{miller} is part of the OTA and is necessary to stabilize the feedback loop. By use of a miller capacitance the pole-zero diagram changes and stability over the desired frequency range is assured.

Figure 7a shows the two regulated PMOS and NMOS currents over an output voltage variation from 0 to 1.5 V. Compared to the basic design, the two currents match and the PMOS current follows the NMOS current equally. The maximum current mismatch of the new design is less than 1% for an output voltage range from 0.1 V to 1.3 V. The output voltage range of the enhanced charge pump design covers 94% of the 1.5 V supply while the conventional design offers only 38% of the supply range. Figure 7b shows the voltage up ramp from 0.2 V to 1.3 V, which is created while the up current permanently injects a charge on the loop filter for 6 µs. The ramp starts at 0 s and ends at 6 µs. The down ramp is also shown. It starts at 6 µs and ends at 0 s. This makes it easier to compare the summed voltage difference produced by the very small current mismatch.

Figure 7. (**a**) Improved current mismatch. (**b**) Output voltage at Up and Down ramp.



(a) **(b)**

3.2.4. Loop Filter

If the spurs to be filtered are more than ten times the loop bandwidth, a third order filter can provide additional benefit. Designing a passive loop filter, involves solving for the time constants and then determining the loop filter components from the time constants. The impedance of the loop filter is:

$$Z(s) = \frac{1 + s \times T_2}{s \times A_0 \times (1 + s \times T_1) \times (1 + s \times T_3)} = \frac{1 + s \times C_2 \times R_2}{s \times (A_2 \times s^2 + A_1 \times s + A_0)} \quad (4)$$

With the time constants T_1–T_3 and the factors A_0–A_2 given in [10], the component parameters can be calculated as:

$$C_1 = \frac{A_2}{T_2^2} \times (1 + \sqrt{1 + \frac{T_2}{A_2} \times (T_2 \times A_0 - A_1)}) \quad (5)$$

$$C_3 = \frac{-T_2^2 \times C_1^2 + T_2 \times A_1 \times C_1 - A_2 \times A_0}{T_2^2 \times C_1 - A_2} \quad (6)$$

$$C_2 = A_0 - C_1 - C_3 \quad (7)$$

$$R_2 = \frac{T_2}{C_2} \quad (8)$$

$$R_3 = \frac{A_2}{C_1 \times C_3 \times T_2} \quad (9)$$

3.2.5. Frequency Divider

The frequency divider has to divide the incoming 24 GHz VCO signal in order to compare it with the reference frequency. The divider structure for the realized PLL consists of a prescaler with a permanent division factor of S = 8 and a multi-modulus divider (MMD) [11] with five control bits. These can be switched to change the division factor of the MMD. The generic MMD architecture includes a number of cascaded divide-by-2/3 cells. The shown architecture achieves a division ratio *N* of,

$$N = S \times (R_0 + 2^1 R_1 + \ \ldots \ + 2^{n-2} R_{n-2} + 2^{n-1} R_{n-1}) \quad (10)$$

in which R_0, R_1, …, R_{n-2}, R_{n-1} are the programmable control bits. Due to the prescaler with static division and the reference frequency of 128 MHz, a MMD with five divide-by-2/3 cells is necessary. A division factor of 16 to 31 in the MMD can be reached with the five controlling bits. The MMD structure is designed in CMOS logic and consumes a total power of 3.4 mW. The prescaler for division from 24 GHz down to 3 GHz was designed in true single phase clock (TSPC) logic [12] to reach the speed and power requirements and consumes only 14 mW from 1.5 V supply voltage.

3.2.6. New TSPC based Static Frequency Divider

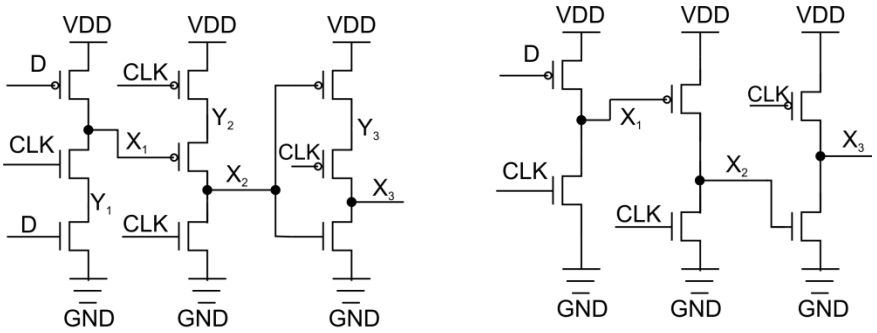
The most critical part in the divider chain is the first stage, which must operate at the highest input frequency. Speed improvements in digital CMOS circuits are not only achieved by scaling to shorter channel length but also by improved circuit techniques. If there are no constraints in power consumption the use of current mode logic (CML) based dividers is common. The topology of a static divide-by-two circuit in CML is described in [13] it is based on edge triggered flip-flops in a negative feedback form, similar to the CMOS structure. To overcome the problems of the CML design, a single-phase clocking technique called TSPC (true single phase clock) grows in importance.

The TSPC logic is based on the principle of precharging and evaluating stages [14]. When the clock is low, the N-section is in precharge mode. This ensures a faster change of the output for P-transistor logic blocks. The precharging takes place with a rising clock edge and evaluation with a falling clock edge. This precharging increases the speed of the TSPC structure and makes it a well working concept at tens of gigahertz. Based on the design concept of a D flip-flop as static divider it can be designed in TSPC structure. The first step is to transfer the functional principle of a flip-flop into the TSPC design structure. In this circuit a n-latch followed by a p-latch is used, and a third stage is needed for evaluation of the output. Here an inverter stage represents the third stage. By use of these three stages as well as the feedback from the output back to the input, the behavior of the static divide-by-two structure can be realized. Assuming the input signal D is at GND, the node X1 is charged to VDD. Due to this charging the following PMOS transistor of the second latch is turned off. Now the value of node X2 is dependent on the clock signal. If the clock signal is falling, the information of X2 will be stored. If the clock signal is rising, the node X2 will be at GND and X3 keeps the previous signal. The node Y3 is precharged to VDD due to the change of X2. This allows a faster change of the output at the next clock cycle. The feedback from the output X3 to the inputs D ensures a stable position of the D-FF until the clock signal changes. The falling clock signal causes node X1 to switch from VDD to GND. This change of potential influences the second latch and node X2 changes from GND to VDD. The output signal turns from VDD to GND and affects the first latch due to the feedback. Now the first latch charges node X1 to VDD again and the described procedure will start again. Due to this behavior, the frequency of the input clock signal will be halved. The cascading of NMOS- and PMOS-logic and an odd number of stages is necessary to ensure correct functionality.

For the proposed designs, an extended true single phase clock (E-TSPC) divider is used instead of the explained TSPC divider to decrease the RC delay and increase the speed of the structure [15]. The functionality of the E-TSPC structure is similar to the TSPC structure, but the circuit is reduced to the necessary minimum of transistors (Figure 8b). Due to leakage currents in the E-TSPC flip-flops, it is important to scale the width of the transistors in each stage correctly. The ratio between NMOS- and

PMOS-transistors is obtained by employing the classical domino logic scaling [16]. Only for this transistor scaling can the right signal decision of each stage and the overall behavior of the system be ensured.

Figure 8. (**a**) True single phase clock (TSPC) based D-FF. (**b**) Extended true single phase clock (E-TSPC) based D-FF.



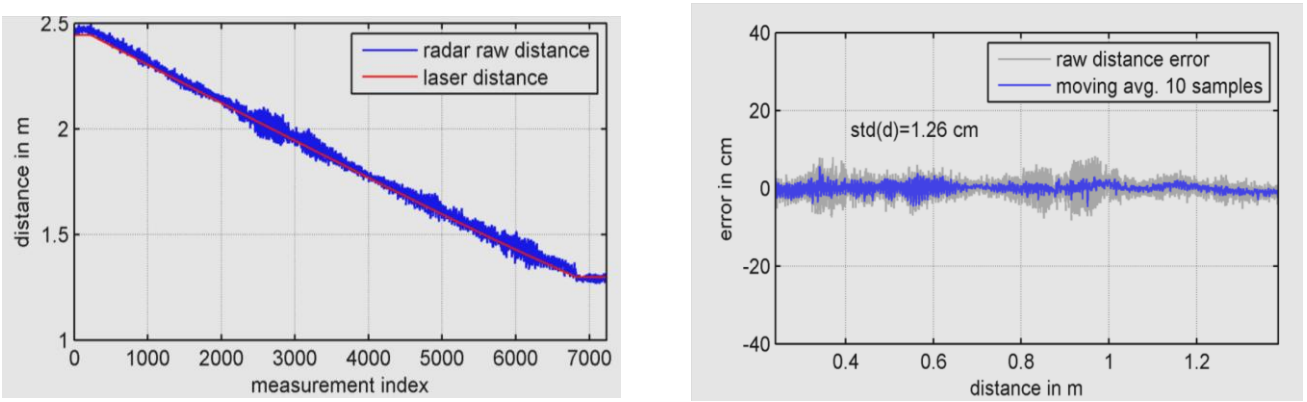
(**a**) (**b**)

4. Prototype and Experiment

The presented system is tested for localization ability and accuracy, system integration and low power consumption. The first step of verification is the proof of concept. This is performed with a system demonstration based on state of the art system components [17]. The first system concept with high precision components shows the ability to cover a measurement distance of 70–80 m with a measurement uncertainty of less than 2 cm. Figure 9a shows the distance in far field compared to a laser based measurement and Figure 9b shows the distance error in a distance of less than 1 m. The disadvantage of the first generation was its size, as shown in Figure 10a and its power consumption. With the first work on system integration, the power consumption and size decreased significantly.

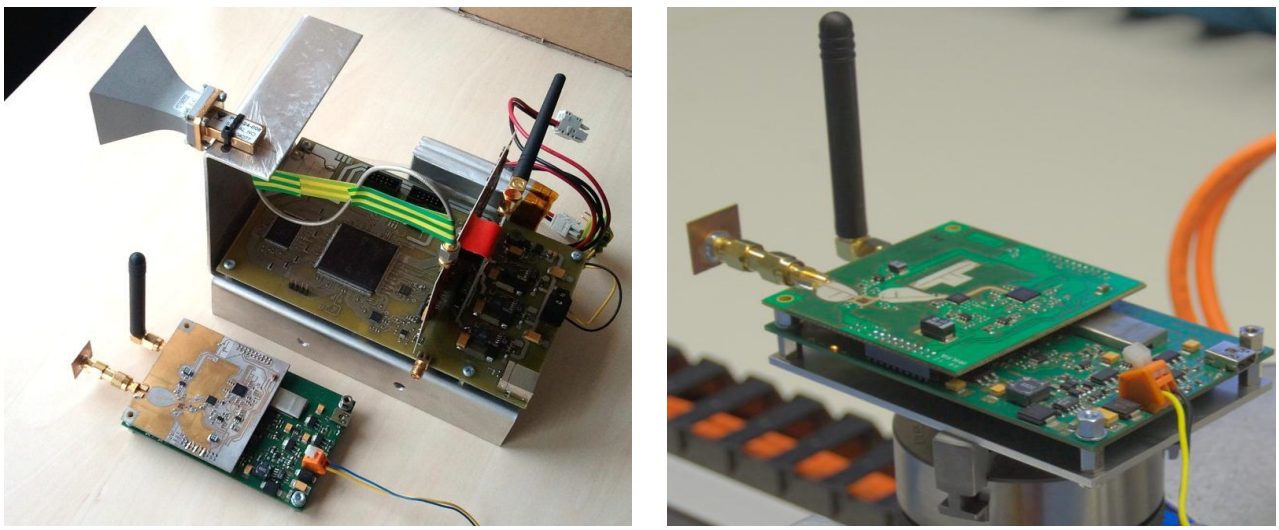
The system of the second generation focuses on miniaturization and power reduction. The synthesizer as the core component of the transceiver can reach a size below 1 cm^2 with a power consumption of less than 40 mW in total and an expected measurement distance of up to 20 m. The PLL itself only consumes 10 mW due to the new divider concept based on true-single phase clock technique. The divider within the PLL consists of a static CML divider stage followed by TSPC stages and a CMOS multi-modulus divider. The measurement results of the TSPC divider in Figure 11 show the division of a 22 GHz signal. A maximum input frequency of 24 GHz is expected with the third generation and new PLL generation. Thus the system of the second generation uses a commercial 24 GHz VCO and prescaler to verify it. The measurement results for the system of the second generation are shown in Figure 12. The error of the second generation is worse than the one of the first generation. This was expected due to size reduction and power reduction. All measurements were done inside a laboratory with concrete walls and a lot of measuring equipment. This scenario can be declared as worst case due to a lot of non line of sight signal. A better accuracy in the industry with wider wall space and outside buildings is expected.

Figure 9. (**a**) Distance compared to laser distance. (**b**) Measurement error within 1 m.



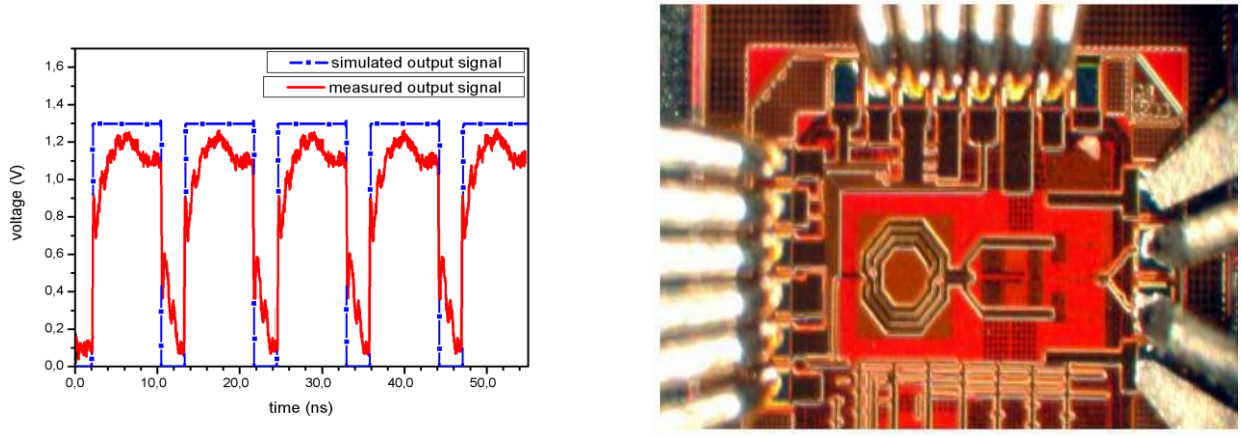
(**a**) (**b**)

Figure 10. (**a**) Sensor of the first and second generation. (**b**) Measurement system.



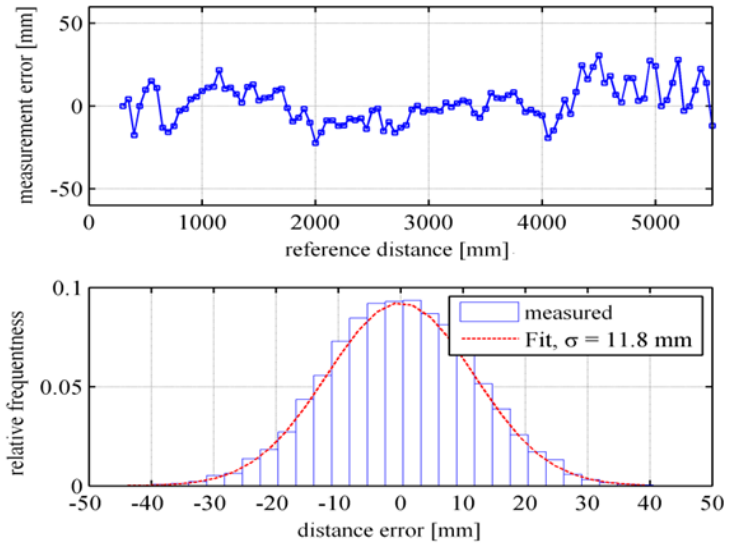
(**a**) (**b**)

Figure 11. (**a**) Measured and simulated output of the divider frequency. (**b**) microphotograph of the integrated synthesizer chip.

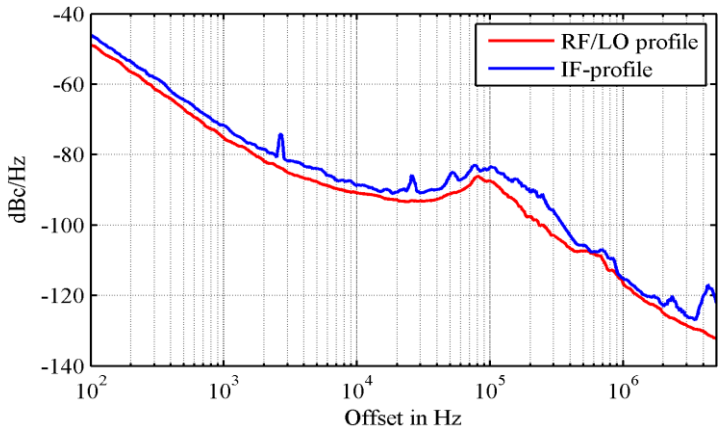


(**a**) (**b**)

Figure 12. (**a**) Distance accuracy and (**b**) phase noise of the second generation 24 GHz synthesizer.



(**a**)



(**b**)

5. Conclusions

Within this article a low-power localization system is presented. The system concept is based on the TDOA principle for localization and additionally has the feature of communication between the sensor nodes. The detection of static and mobile sensor nodes in the *ad hoc* network is possible with this system concept. The goal of the system is a low power consumption and small system size in combination with highly accurate node localization. The novel miniaturized low power hardware components are presented in this paper. It is shown that a synthesizer design with a low power fractional-N PLL is feasible for accurate FMCW distance measurement. The 24 GHz synthesizer consumes less than 40 mW. Thus the system goal of less than 100 mW power consumption has been met and a localization accuracy of less than 2 cm has been reached.

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Conflicts of Interest

The authors declare no conflict of interest.

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