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# A Compact and High-Performance Acoustic Echo Canceller Neural Processor Using Grey Wolf Optimizer along with Least Mean Square Algorithms

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**Abstract:** Recently, the use of acoustic echo canceller (AEC) systems in portable devices has significantly increased. Therefore, the need for superior audio quality in resource-constrained devices opens new horizons in the creation of high-convergence speed adaptive algorithms and optimal digital designs. Nowadays, AEC systems mainly use the least mean square (LMS) algorithm, since its implementation in digital hardware architectures demands low area consumption. However, its performance in acoustic echo cancellation is limited. In addition, this algorithm presents local convergence optimization problems. Recently, new approaches, based on stochastic optimization algorithms, have emerged to increase the probability of encountering the global minimum. However, the simulation of these algorithms requires high-performance computational systems. As a consequence, these algorithms have only been conceived as theoretical approaches. Therefore, the creation of a low-complexity algorithm potentially allows the development of compact AEC hardware architectures. In this paper, we propose a new convex combination, based on grey wolf optimization and LMS algorithms, to save area and achieve high convergence speed by exploiting to the maximum the best features of each algorithm. In addition, the proposed convex combination algorithm shows superior tracking capabilities when compared with existing approaches. Furthermore, we present a new neuromorphic hardware architecture to simulate the proposed convex combination. Specifically, we present a customized time-multiplexing control scheme to dynamically vary the number of search agents. To demonstrate the high computational capabilities of this architecture, we performed exhaustive testing. In this way, we proved that it can be used in real-world acoustic echo cancellation scenarios.

**Keywords:** grey wolf optimization; swarm intelligence; real world application; spiking neural P system; AEC system; LMS; neuromorphic architecture; FPGA

**MSC:** 68W10; 68Q06; 68Q45; 68W99; 94A12



**Citation:** Pichardo, E.; Anides, E.; Vazquez, A.; Garcia, L.; Avalos, J.G.; Sánchez, G.; Pérez, H.M.; Sánchez, J.C. A Compact and High-Performance Acoustic Echo Canceller Neural Processor Using Grey Wolf Optimizer along with Least Mean Square Algorithms. *Mathematics* **2023**, *11*, 1421. <https://doi.org/10.3390/math11061421>

Academic Editor: Gaige Wang

Received: 1 February 2023

Revised: 28 February 2023

Accepted: 13 March 2023

Published: 15 March 2023



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## 1. Introduction

Nowadays, acoustic echo canceller (AEC) systems mainly use the least mean square (LMS) adaptive filter algorithm, since it exhibits low computational complexity [1]. Therefore, this algorithm is easy to implement in low-area devices. However, its use can cause instability in the system, since it has an uni-model error surface. Hence, this algorithm is limited when a multimodal error surface is considered, since this algorithm must be initialized in the valley of the global optimum to converge to the global optimum [2]. Another aspect is linked to its convergence speed, because this depends on the eigen-value spread of the correlation Matrix (R) [3]. To overcome these problems, bio-inspired evolutionary [4,5] and swarm intelligence (SI) techniques [6–8], have emerged as potential solutions for the parameter optimization. Recently, the grey wolf optimization (GWO)

algorithm [6], which is considered to be one of the most recent metaheuristic SI methods, has proven to be very successful in multiple fields, such as image processing [9,10], health care/bioinformatics [11,12], control systems [13], electromagnetics [14,15], environmental applications [16,17], and adaptive filtering [18,19], among others [20,21], since this algorithm offers impressive characteristics in contrast with other swarm intelligence methods.

In general terms, the GWO algorithm shows a good balance between the exploration and exploitation processes during the search. As a consequence, this allows high accuracy. From the engineering point of view, this algorithm can be seen as a potential solution in practical applications, since it involves fewer parameters and less memory compared with the most advanced metaheuristic SI methods. Therefore, this algorithm requires few controlling parameters. As a consequence, its practicality is increased significantly [21]. Based on these features, new variants of the GWO algorithm can be developed to be applied in practical and real-time acoustic echo canceller (AEC) systems.

In general, bio-inspired algorithms are capable of globally optimizing any class of adaptive filter structures. Therefore, the use of these algorithms opens new opportunities in the development of advanced adaptive filters and enables their implementation in embedded devices [22]. Specifically, recent studies have proven that the particle swarm optimization (PSO) algorithm can be used in the development of AEC systems. For example [23] proposed a PSO-based AEC system to guarantee a high degree of accuracy in terms of echo return loss enhancement (ERLE). Specifically, the authors used the PSO to perform the error minimization in the frequency domain. Ref. [24] presented a PSO-based AEC system, in which the PSO algorithm provides a very fast convergence rate by performing the error minimization in the time domain. Another PSO-based AEC system was developed by [25]. This approach was applied to multichannel systems to improve stability.

After analysing all the works mentioned above, we found that the PSO algorithm may suffer some limitations, especially when a heavy constraint optimization is required. Under this situation, one may get trapped in local minima. To avoid this, the GWO algorithm can be seen as a potential solution, since it offers a high convergence rate at the cost of exhibiting high computational complexity and low tracking capabilities [26–28]. In particular, good performance can be obtained, especially when a large population is used, i.e., population-based meta-heuristics generally have greater exploration when compared to a single solution-based algorithm [6]. However, its implementation in current embedded devices becomes infeasible. Hence, the development of new variants of GWO algorithms, to decrease their computational cost whilst maintaining performance, is still a great challenge. Recently, some authors have proposed convex combinations of adaptive filters, in which two adaptive algorithms with complementary capabilities are used to improve the steady-state MSE and the tracking performance [29,30]. With respect to the latter, the tracking performance determines the capabilities of the system to track variations in the statistics of the signals of interest [31]. Therefore, in practical AEC systems, the improvement of this factor is highly required [32].

Here, we propose a new variant of the convex adaptive filter, based on the GWO and LMS algorithms. In addition, we include the block-processing scheme in both algorithms to easily implement them in parallel hardware architectures. As a consequence, these algorithms were applied to real-time and practical AEC applications. Specifically, we used the GWO algorithm to guarantee a high convergence rate and high tracking capabilities. With respect to the latter, we added new exploration capabilities by dynamically adjusting the search space, especially in the context of abrupt changes occurring in the acoustic environment, which cannot be achieved when using the conventional GWO algorithm. A significant improvement in terms of computational cost was achieved by dynamically decreasing the population of the GWO algorithm over the filtering process. In addition, the use of the LMS allowed us to improve the steady-state MSE.

From an engineering perspective, the development of low computational complexity metaheuristic SI methods makes their implementation in current resource-constrained devices feasible. In addition, the development of advanced and novel implementation

techniques also opens new opportunities in the creation of compact and high-performance devices. Specifically, the simulation of the proposed convex GWO/LMS adaptive filter requires an enormous number of large precision multipliers. Therefore, the development of low area, low latency and large precision adders and multipliers is still a challenging task. Inspired by the neural phenomena, Ionescu presented, for the first time, a class of distributing and parallel computing models, denominated as spiking neural P systems [33]. This new area of membrane computing intends to exploit, to the maximum, the intrinsic parallel capabilities of the soma of the neurons to create novel processing systems. In recent years, several authors focused their efforts to create advanced arithmetic circuits, such as adders and multipliers.

- *Parallel neural adder.*

Recently, Ref. [34] developed a neural adder circuit to compute two large integer numbers in parallel. In spite of this achievement, this adder demands an enormous number of synapses and neurons to process large integer numbers. As a result, its use for simulation purposes becomes impractical, since metaheuristic SI methods demand high precision numerical accuracy.

- *Parallel neural multiplier.*

In [35], the authors intended to significantly reduce the number of synapses to create an ultra-compact parallel multiplier. Despite decreasing the area consumption, the processing speed was still high.

Analyzing previous works, we noted that these circuits were proposed to process large integer numbers in parallel at the cost of increasing their processing speed. Therefore, any of these circuits can be used in the simulation of real-time AEC systems. In addition, arithmetic circuits with more precision exhibit a clear trade-off between area consumption and processing speed. From an engineering perspective, several authors still continue to make tremendous efforts to design advanced neural arithmetic circuits with high-precision to be used in real-time AEC systems. Specifically, these developments face two large challenges:

- Design of high-speed and high-precision neural adders and neural multipliers.
- Design of high-processing speed hardware architectures to efficiently simulate the proposed convex GWO/LMS adaptive filter in embedded devices.

Regarding the latter, we developed three potential proposals:

1. *Design of a high-precision floating-point parallel adder circuit.* Here, we present, for the first time, a neural adder, which computes the numbers in a customized floating-point model. We employ new variants of the SN P systems, called coloured-spikes [36], rules on the synapses [37], target indications, extended channel rules [38] and extended rules [39] to process numbers under this format in the proposed arithmetic circuit.
2. *Design of a high-precision floating-point parallel multiplier.* Here, we present, for the first time, the development of a neural multiplier to compute floating-point numbers at high processing speeds.
3. *Design of a new FPGA-based GWO/LMS neuromorphic architecture.* We design the proposed neuromorphic architecture employing basic digital components, such as shift registers, adders and multiplexors, to guarantee a low area consumption. Since the proposed convex GWO/LMS adaptive filter dynamically varies the number of search agents, we propose, for the first time, a time-multiplexing control scheme to adequately support this behavior.

Our results showed that the proposal of new variants of the GWO algorithm, along with new implementation techniques, generates a compact neuromorphic architecture to be used in practical and real-time AEC applications.

The paper is structured as follows. Section 2 introduces the fundamentals of GWO and LMS algorithms. Additionally, we introduce the proposed Convex GWO/LMS algorithm, which involves the use of a new set of equations to improve its tracking capabilities and computational complexity. Section 3 presents software simulation tests, including the justification of the selection of some tuning parameters and display comparisons

between existing approaches and the proposed algorithm. In Section 4, we present a new parallel neural adder circuit and a new parallel neural multiplier circuit, which are highly demanded in the computation of the proposed algorithm. In addition, this section introduces experimental results of the implementation of the proposed Convex GWO/LMS algorithm in the Stratix IV GX EP4SGX530 FPGA. Finally, in Section 5 we provide the conclusions.

## 2. The Proposed Block Convex GWO/LMS Algorithm

### 2.1. GWO Algorithm

In general terms, the GWO is considered a population-based optimization technique inspired by the behavior of the *Canis lupus* [6]. This algorithm intends to mimic the hunting and hierarchical behavior of grey wolves. Regarding the latter, this algorithm involves four hierarchical levels; alpha ( $\alpha$ ) represents the fittest solution in the population, while beta ( $\beta$ ) and delta ( $\delta$ ) denote the second and third best solutions, respectively. Finally, omega ( $\omega$ ) are the search agents. To simulate the GWO algorithm, the following equations are used:

$$\vec{W}(n+1) = \vec{W}_p(n) - \vec{A} \cdot |\vec{C} \times \vec{W}_p(n) - \vec{W}(n)| \tag{1}$$

where  $n$  denotes the current iteration,  $\vec{W}_p$  is the position vector of the prey,  $\vec{W}$  represents the position of a grey wolf,  $\vec{A} = 2\vec{a} \cdot \vec{r}_1 - \vec{a}$  and  $\vec{C} = 2\vec{r}_2$  denote coefficient vectors, where  $\vec{r}_1$  and  $\vec{r}_2$  represent random vectors in  $[0, 1]$ , respectively, and  $\vec{a}$  is linearly decreased from 2 to 0 using the following equation

$$\vec{a}(t) = 2 - \frac{2t}{MaxIter} \tag{2}$$

where *MaxIter* is the total number of iterations.

To update the position of the search agents, the following equations must be used

$$\vec{W}_1(n) = \vec{W}_\alpha(n) - \vec{A}_1 \cdot |\vec{C}_1 \cdot \vec{W}_\alpha(n) - \vec{W}(n)| \tag{3}$$

$$\vec{W}_2(n) = \vec{W}_\beta(n) - \vec{A}_2 \cdot |\vec{C}_2 \cdot \vec{W}_\beta(n) - \vec{W}(n)| \tag{4}$$

$$\vec{W}_3(n) = \vec{W}_\delta(n) - \vec{A}_3 \cdot |\vec{C}_3 \cdot \vec{W}_\delta(n) - \vec{W}(n)| \tag{5}$$

$$\vec{W}_p(n+1) = \frac{\vec{W}_1(n) + \vec{W}_2(n) + \vec{W}_3(n)}{3} \tag{6}$$

where  $\vec{W}_\alpha(n)$ ,  $\vec{W}_\beta(n)$ ,  $\vec{W}_\delta(n)$  are the best three wolves at each iteration and  $\vec{W}_p(n+1)$  is the new position of the prey.

### 2.2. LMS Algorithm

The LMS algorithm is a practical method to obtain estimates of a filter's weights,  $\mathbf{w}(n)$ , in real time [1]. The equation for updating the weights of the LMS algorithm in a sample by sample fashion is given by:

$$\mathbf{w}(n+1) = \mathbf{w}(n) + \mu e(n)\mathbf{x}(n) \tag{7}$$

where  $\mathbf{x}(n)$  is the current input vector,  $\mu$  is a fixed step-size  $[0, 1]$ ,  $e(n)$  is the error signal and is calculated using:

$$e(n) = d(n) - \mathbf{w}^T(n)\mathbf{x}(n) \tag{8}$$

and  $d(n)$  is the desired signal.

### 2.3. Convex GWO/LMS

As discussed above, the GWO algorithm is widely used to solve a variety of problems since it exhibits significant properties. However, it has a number of limitations and suffers

from inevitable drawbacks. The main limitation comes from the no-free-lunch (NFL) theorem, which states that no optimization algorithm is able to solve all optimization problems [40]. This means that GWO might require modification when solving some real-world problems. In particular, we proposed some modifications to the conventional GWO to be used in the development of AEC systems. Specifically, we present a new combination between the GWO and the LMS algorithms to improve tracking-capabilities and the steady-state error of the filter, respectively, since it has been proven that the use of convex combination approaches significantly improve the performance of adaptive schemes by using two adaptive algorithms [41].

As can be observed in Figure 1, the proposed system computes the coefficients of the filters,  $\mathbf{w}_1$  and  $\mathbf{w}_2$ , as follows:

- *The calculation of the filter coefficients by employing the LMS algorithm.* Here, we use the block LMS algorithm to calculate the  $\mathbf{w}_1$  weights. This has allowed us to create efficient implementations by using commercially available embedded devices [42,43]. The adaptive filter coefficients  $\mathbf{w}_1$  are defined as:

$$\mathbf{w}_1(n + 1) = \mathbf{w}_1(n) + \mu \mathbf{X}(n) \mathbf{e}_{LMS}(n) \tag{9}$$

where  $\mathbf{w}_1(n)$  is the weight-vector  $\mathbf{w}_1(n) = [w(0), w(1), \dots, w(N - 1)]^T$ ,  $\mu$  is the step-size, and  $\mathbf{e}_{LMS}(n)$  is the error vector. The error vector is composed as:

$$\mathbf{e}_{LMS}(n) = [e(nL), e(nL - 1), \dots, e(L(n + 1) + 1)]^T \tag{10}$$

and  $\mathbf{X}(n)$  is derived from the current input block

$$\mathbf{x}(n) = [x(nL), x(nL - 1), \dots, x(nL - N + 1)] \tag{11}$$

where  $L$  depicts the length of the block and  $N$  is the size of the filter. Additionally,  $\mathbf{X}(n)$  is calculated as follows:

$$\mathbf{X}(n) = \begin{bmatrix} x(nL), & x(nL - 1), & \dots & x(nL - N + 1) \\ x(nL - 1) & x(nL - 2) & \dots & x(nL - N) \\ \vdots & \vdots & \ddots & \vdots \\ x(nL - L + 1) & x(nL - L) & \dots & x(nL - L - N + 2) \end{bmatrix}^T \tag{12}$$

The error vector is obtained as follows:

$$\mathbf{e}_{LMS}(n) = \mathbf{d}(n) - \mathbf{y}_{LMS}(n) \tag{13}$$

where the desired response vector  $\mathbf{d}(n)$  is given by L

$$\mathbf{d}(n) = [d(nL), d(nL - 1), \dots, d(nL - N + 1)]^T \tag{14}$$

The filter output  $\mathbf{y}_{LMS}(n)$  of each block is given by the following matrix vector product:

$$\mathbf{y}_{LMS}(n) = \mathbf{X}(n) \cdot \mathbf{w}_1(n) \tag{15}$$

- *The calculation of the filter coefficients by employing the GWO algorithm.* Here, the use of the block-processing scheme in SI algorithms allowed us to process the signal in real-time applications. As a consequence, this potentially allows full exploitation of the performance capabilities of the parallel hardware architectures by simulating the intrinsic parallel computational capabilities of the SI algorithms. In this work, we introduce, for the first time, the block-based GWO algorithm to be applied in practical and real-time AEC applications, as shown in Figure 2.

The encircling behavior of the grey wolves is mathematically described as follows:

$$\vec{W}(n+1) = \vec{W}_p(n) - \vec{A} \cdot |\vec{C} \cdot \vec{W}_p(n) - \vec{W}(n)| \tag{16}$$

where  $\vec{A} = 2\phi(n) \cdot \vec{r}_1 - \phi(n)$  denotes a coefficient vector, and  $\phi(n)$  is in function of the value of instantaneous error. In addition, this value is in a range of 0 and 2. This can be described by:

$$\phi(n) = \frac{4}{1 + e^{-[e_{GWO}(n)]}} - 2 \tag{17}$$

To obtain the best solution, a fitness function, which is defined in terms of the mean square error (MSE), is used to evaluate each search agent. Hence, the fitness value  $f_k$  of the position  $\vec{W}$  is expressed as:

$$f_k(n) = \frac{1}{L} \sum_{i=1}^L e_k^2(i) \tag{18}$$

where  $k = 1, 2, \dots, P(n)$ . Here, we propose a mechanism to dynamically adjust the number of search agents over the filtering process, i.e.,  $P(n)$  denotes the current number of search agents. Specifically, this adjustment is a function of the power of the instantaneous error, and is obtained as follows:

$$P(n) = \lfloor \frac{2 \cdot (P_{max} - P_{min})}{(1 + e^{-[e_{GWO}(n)]})} - (P_{max} - P_{min}) \rfloor + P_{min} \tag{19}$$

where  $P_{max}$  and  $P_{min}$  defines the maximum and the minimum number of search agents, respectively. In addition, we use Equations (3)–(6) to update the position of the search agents and the prey. On the other hand, the error signal,  $e_{GWO}(n)$ , and filter output,  $y_{GWO}(n)$ , are described as follows:

$$\mathbf{e}_{GWO}(n) = \mathbf{d}(n) - \mathbf{y}_{GWO}(n) \tag{20}$$

$$\mathbf{y}_{GWO}(n) = \mathbf{X}(n) \cdot \mathbf{w}_2(n) \tag{21}$$

where  $\mathbf{w}_2(n) = \vec{W}_\alpha$ .

Considering the output of both filters,  $\mathbf{y}_{GWO}(n)$  and  $\mathbf{y}_{LMS}(n)$  at time  $n$ , we obtain the output of the parallel filter as:

$$\mathbf{y}(n) = \lambda(n) \cdot \mathbf{y}_{GWO}(n) - [1 - \lambda(n)] \cdot \mathbf{y}_{LMS}(n) \tag{22}$$

where  $\lambda(n)$  is a mixing parameter, which is in the range [0, 1]. This parameter is used to control the combination of the two filters at each iteration, and is defined by:

$$\lambda(n) = \frac{1}{e^{-a(n)}} \tag{23}$$

where  $a(n)$  is an auxiliary parameter used to minimize the instantaneous square error of the filters, and is obtained as follows:

$$a(n+1) = a(n) + \mu_a \cdot e(1) \cdot \{e_{GWO}(1) - e_{LMS}(1)\} \cdot \lambda(n) \cdot [1 - \lambda(n)] \tag{24}$$

Finally, the performance of the combined filter can be further improved by transferring a portion of  $\mathbf{w}_1$  to  $\vec{W}_\alpha$ ,  $\vec{W}_\beta$  and  $\vec{W}_\delta$ . This can be formulated as follows:

$$\vec{W}_\alpha(n) = \lambda(n) \cdot \vec{W}_\alpha(n) - [1 - \lambda(n)] \cdot \mathbf{w}_1(n) \tag{25}$$

$$\vec{W}_\beta(n) = \lambda(n) \cdot \vec{W}_\beta(n) - [1 - \lambda(n)] \cdot \mathbf{w}_1(n) \tag{26}$$

$$\vec{W}_\delta(n) = \lambda(n) \cdot \vec{W}_\delta(n) - [1 - \lambda(n)] \cdot \mathbf{w}_1(n) \tag{27}$$

In this way, the GWO filter can reach a lower steady-state MSE and continues to keep a high convergence rate.

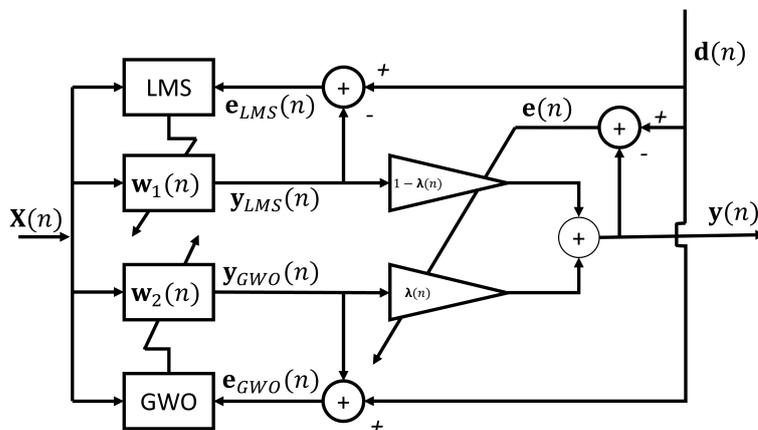


Figure 1. Proposed convex structure.

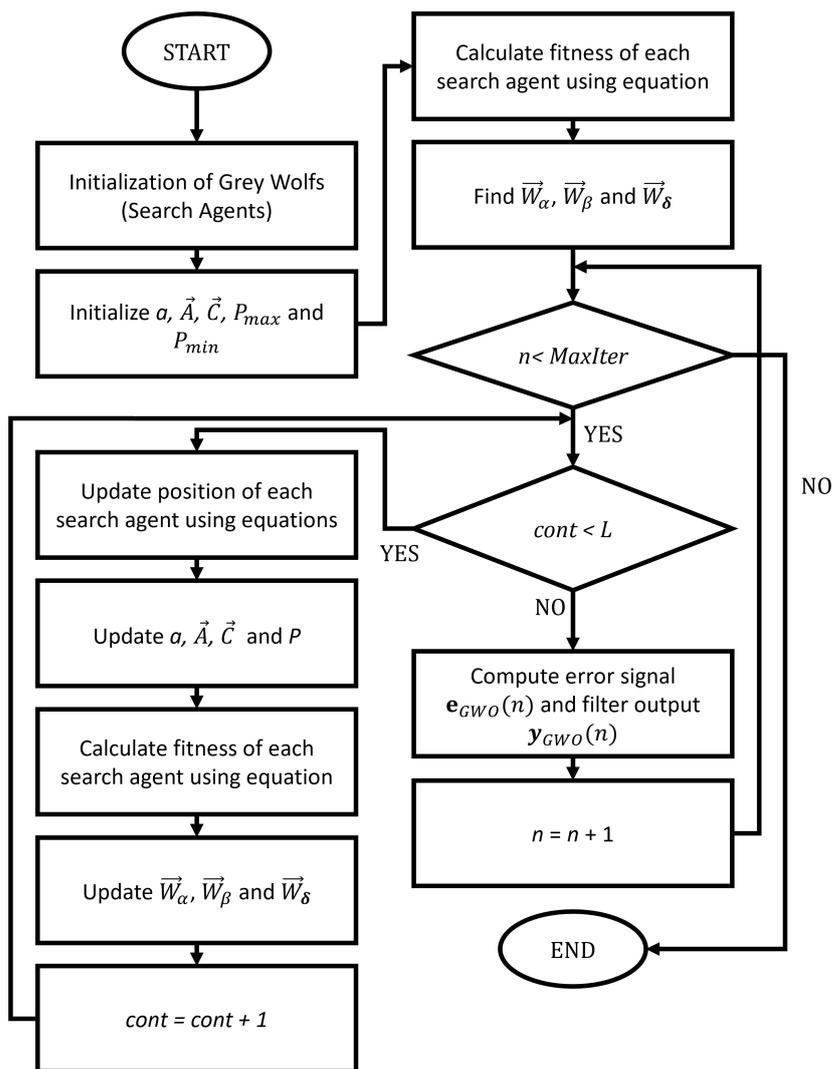


Figure 2. The flowchart of the block GWO algorithm.

### 3. Pure Software Simulation

Before implementing the proposed convex GWO/LMS adaptive filter in parallel hardware architectures, we simulated it in Matlab software for testing and comparison purposes. Specifically, we simulated the conventional LMS, GWO and our proposal to compare their performances. In addition, we used AEC structure, in which the existing approaches and the proposed convex GWO/LMS adaptive filter were used, as shown in Figure 3. As can be observed,  $x(n)$  is the far-end input signal,  $e(n)$  denotes the residual echo signal,  $d(n)$  represents the sum of the echo signal,  $y(n)$  and the background noise,  $e_0(n)$ .

To simulate the proposed convex GWO/LMS adaptive filter and existing approaches, we considered the following conditions:

1. We used an impulse response as the echo path, obtained from the ITU-T G168 recommendation [44]. This echo path was modeled using 500 coefficients, as shown in Figure 4.
2. The echo signal was mixed with white Gaussian noise (SNR = 20 dB).
3. We used an AR(1) process as input signal.
4. The filter and the block had the same length as the echo path. As is well known, the efficiency of the block processing scheme is guaranteed when the length of the blocks is greater than, or equal to, the order of the filter [45,46].
5. In the proposed algorithm, the swarm size was defined in the range of 15–30 search agents.
6. To test the tracking capabilities of the proposed algorithm, we induced an abrupt change in the impulse response of the acoustic echo path in the middle of the adaptive filtering process by multiplying the acoustic paths by  $-1$ .
7. The maximum number of iterations was set to 2,000,000.

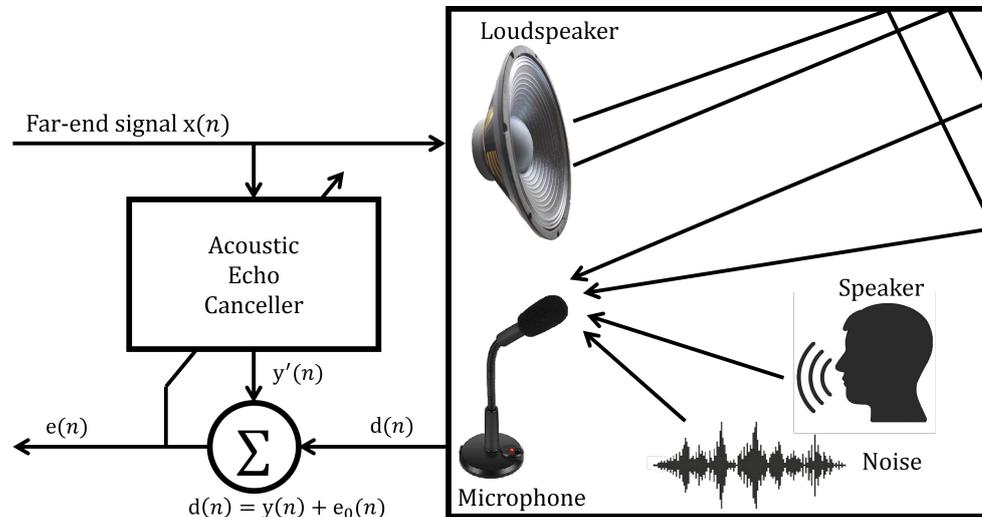


Figure 3. Structure of the acoustic echo canceller.

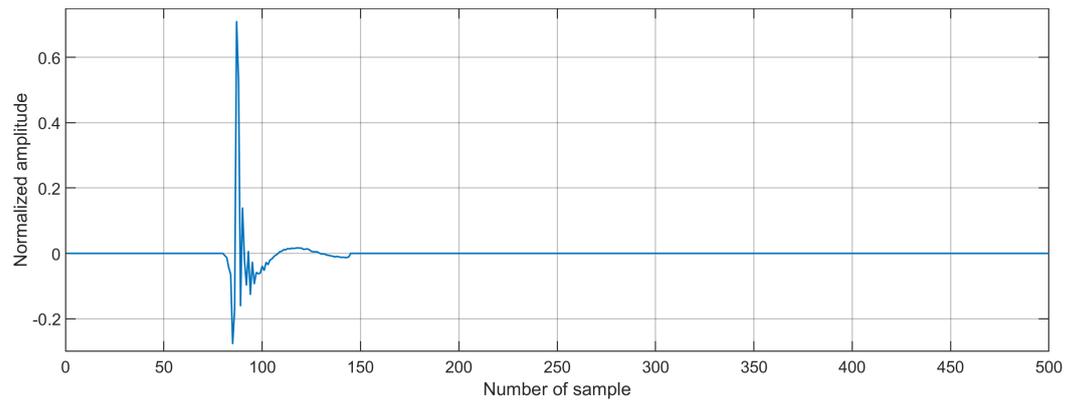


Figure 4. Acoustic echo path used for the simulation of the existing and the proposed algorithms.

Considering a single-talk scenario, we performed three experiments to verify the performance of the proposed convex GWO/LMS adaptive filter in terms of echo return loss enhancement, ( $ERLE = 10\log_{10}(\frac{d(n)^2}{e(n)^2})$ ).

- *Effect of changing the order of the adaptive filter.*  
 Figure 5 shows the evaluation of the ERLE level of the proposed algorithm. In this evaluation, we used a population size of 30 search agents and varied the number of coefficients of the adaptive filter from 150 to 500. The aim of this experiment was to observe how the ERLE level was affected by using different numbers of coefficients. Here, the proposed convex GWO/LMS adaptive filter guaranteed the same ERLE level regardless of the number of coefficients, as shown in Figure 5. Therefore, we used the minimum number of coefficients, since this factor is relevant, especially when it is implemented in resource-constrained devices.

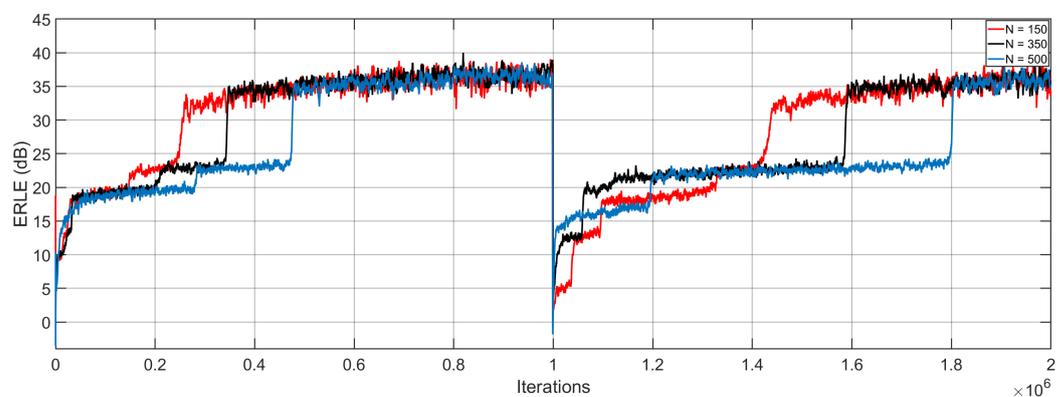
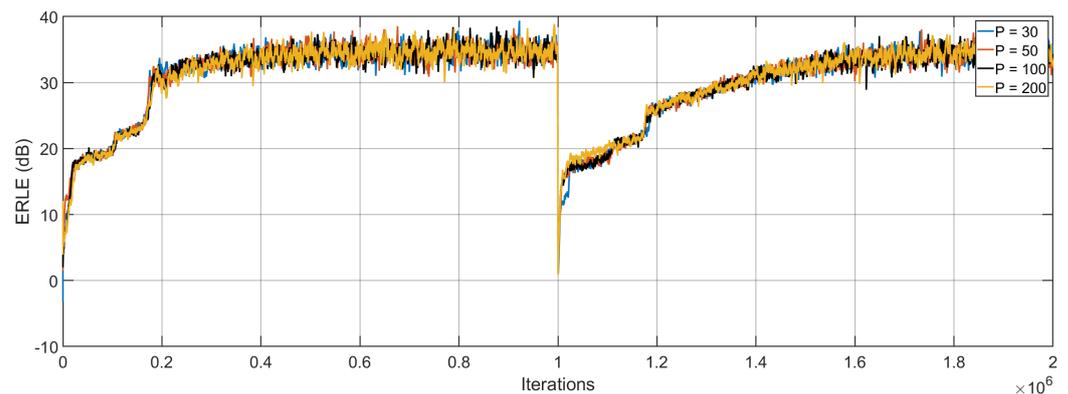


Figure 5. ERLE level for different number of coefficients  $N$ .

- *Effect of varying the number of search agents of the proposed convex GWO/LMS adaptive filter.* In this experiment, we varied the number of search agents from 30 to 200 to evaluate the performance of the proposed algorithm in terms of ERLE level. Since the minimum number of adaptive filter coefficients (150) guaranteed a good ERLE level, we used this number for the experiment. As can be observed from Figure 6, we obtained the same performance by using different numbers of search agents. In this way, we confirmed that, when employing the minimum number of search agents, the proposed method reached a good ERLE level. From an engineering perspective, this has a great impact on the performance of resource-constrained devices, since the proposed algorithm intends to reduce its computational cost by decreasing the number of search agents over the adaptive process.



**Figure 6.** ERLE for different numbers of search agents  $P$ .

- *Performance comparison between the proposed convex GWO/LMS and existing approaches.*  
We performed two experiments to make a coherent comparison between the proposed convex GWO/LMS and the following existing approaches: LMS algorithm [1], conventional GWO [6], PSO [23], differential evolution (DE) algorithm [47], artificial bee colony optimization (ABC) [48], hybrid PSO–LMS [49] and modified ABC (MABC) [50]. In the first experiment, we shifted the acoustic path, and in the second experiment, we multiplied the acoustic path by  $-1$  at the middle of the adaptive process. In addition, the tuning parameters of all the algorithms were selected to guarantee the best performance. Such tuning parameters are displayed in the following list:
  1. **LMS**
    - Convergence factor =  $9 \times 10^{-7}$
  2. **GWO**
    - $a$  decreases linearly from 2 to 0
    - lower bound =  $-1$
    - Upper bound = 1
    - Population size = 50
  3. **PSO**
    - Acceleration coefficient,  $c_1 = 1.6$
    - Acceleration coefficient,  $c_2 = 1$
    - Inertia weight = 0.8
    - Lower bound =  $-1$
    - Upper bound = 1
    - Population size = 100
  4. **DE**
    - Crossover rate = 0.35
    - Scaling factor = 0.8
    - Combination factor = 0.25
    - Lower bound =  $-1$
    - Upper bound = 1
    - Population size = 50
  5. **ABC**
    - Evaporation parameter = 0.1
    - Pheromone = 0.6
    - Lower bound =  $-1$
    - Upper bound = 1
    - Population size = 50

## 6. PSO-LMS

- Acceleration coefficient,  $c_1 = 0.00005$
- Acceleration coefficient,  $c_2 = 1.2$
- Inertia weight = 1
- Lower bound =  $-1$
- Upper bound = 1
- Convergence factor =  $1 \times 10^{-9}$
- Population size = 60

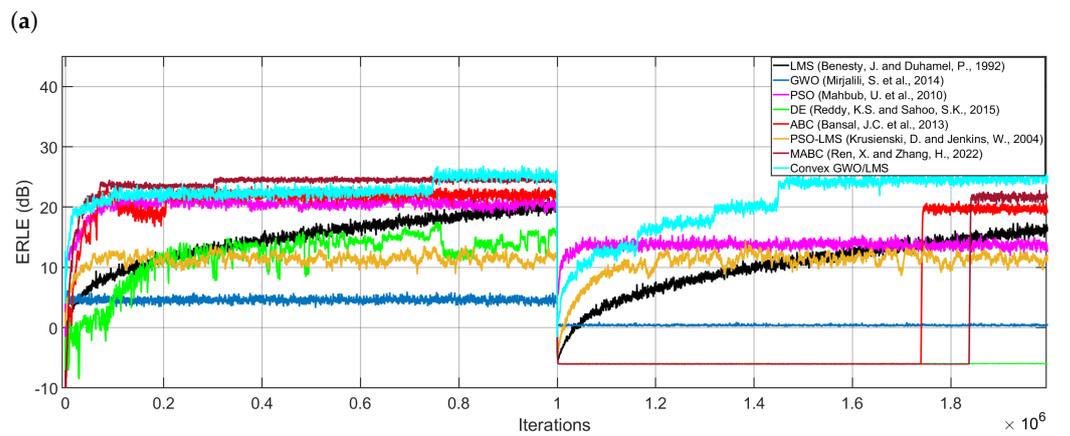
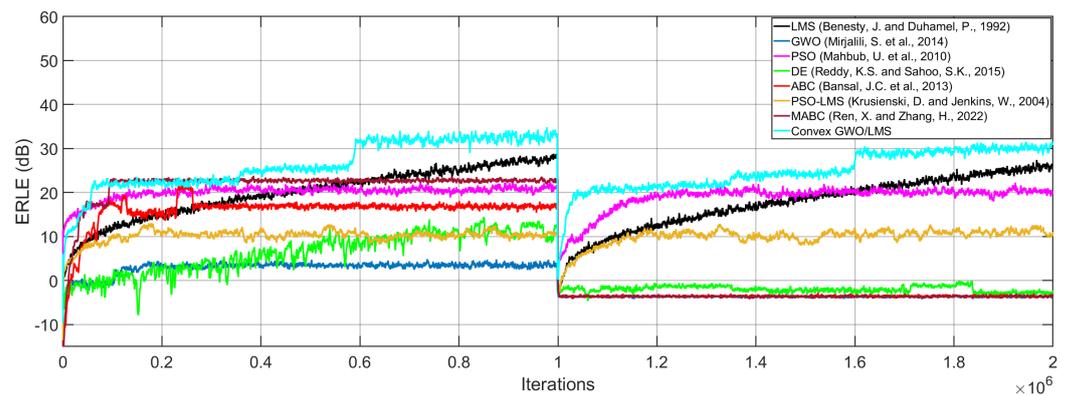
## 7. MABC

- Evaporation parameter = 0.1
- Pheromone = 0.6
- Lower bound =  $-1$
- Upper bound = 1
- Population size = 50
- Convergence factor =  $3 \times 10^{-5}$

As can be observed from Figure 7, the proposed convex GWO/LMS adaptive filter showed the best performance, in terms of ERLE level and convergence speed, by expending a large number of additions and multiplications, as shown in Table 1. In contrast, the LMS algorithm expended fewer additions and multiplications compared with the proposed algorithm at the cost of exhibiting a slow convergence speed. In general, the excessive number of additions and multiplications makes the implementation of the GWO adaptive filter in current embedded devices, such as DSP and FPGA devices, impractical since they have a limited number of these circuits. Here, our proposal intended to dynamically decrease the number of search agents, as shown in Figure 8. As a consequence, the number of multiplications and additions also reduced (Equation (19)). In this way, the implementation of our proposal in embedded devices can be feasible.

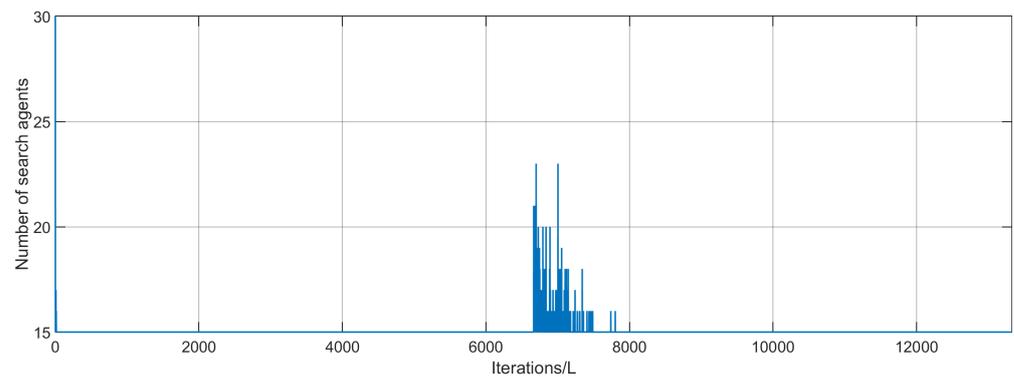
**Table 1.** Comparison between the proposed convex GWO/LMS system and existing approaches in terms of the number of additions and multiplications.

Algorithm	Multiplications	Additions
LMS [1]	6,000,118,333	6,000,118,333
GWO [6]	1,349,996,758,333	2,249,994,508,333
PSO [23]	1,500,036,249,900	1,500,036,249,900
DE [47]	149,999,625,000	299,999,250,000
ABC [48]	600,058,499,850	749,938,125,150
PSO-LMS [49]	903,077,742,300	906,037,734,900
MABC [50]	1,799,955,500,100	1,620,075,949,800
Convex GWO/LMS	73,599,043,327	46,560,966,659



(b)

**Figure 7.** ERLE learning curves obtained by simulating existing approaches and the proposed algorithm; (a) by shifting the acoustic path at the middle of iterations and (b) by multiplying the acoustic path by  $-1$  at the middle of iterations [1,15,23,48–51].



**Figure 8.** The number of search agents used during the adaptation process.

- *Statistical comparison between the proposed convex GWO/LMS and existing approaches* Statistical results were obtained with two different evaluations: average value of ERLE in dB and its corresponding standard deviation. The maximum number of iterations was set to 2,000,000 and each algorithm ran 10 times. The results are reported in Table 2.

**Table 2.** Comparison between the proposed convex GWO/LMS system and existing approaches in terms of average value of ERLE and standard deviation in dB.

Algorithm	Average Value	Standard Deviation
LMS [1]	14.7202	4.1761
GWO [6]	4.5653	0.3892
PSO [23]	20.2452	1.5622
DE [47]	11.7972	4.4434
ABC [48]	21.0656	3.4164
PSO-LMS [49]	11.2859	1.1497
MABC [50]	23.6927	3.0326
Convex GWO/LMS	22.7590	2.0259

As can be observed from Table 2, the proposed convex GWO/LMS achieved a good average ERLE level, in comparison with other existing algorithms. It should be noted that the MABC algorithm possessed the highest average value. Nonetheless, this algorithm presented a lower convergence speed, especially when abrupt changes occurred, as shown in Figure 7b. On the other hand, the GWO, PSO and PSO-LMS algorithms presented lower standard deviations in comparison with the proposed Convex GWO/LMS algorithm. Nonetheless, the proposed method achieved a higher average value.

#### 4. Pure Hardware Simulation

To adequately simulate the proposed convex GWO/LMS system, we made extraordinary efforts to develop compact, high-processing and high-precision neural arithmetic circuits, such as adder and multiplier, since these two circuits are highly demanded in the computation of the proposed algorithm, as shown in Table 1. Specifically, we developed, for the first time, a customized floating-point representation to perform additions and multiplications with high precision.

To compute the numbers in floating-point format, we established the format criteria of the input numbers  $u$  and  $v$  to be either added or multiplier, as follows:

1. In general terms, the numbers  $u$  and  $v$  are separated in integer and fractional digits. Specifically, the number of integer digits and the number of fractional digits can be chosen over a range  $(u_{g_0} \cdots u_{g_1} \cdots u_{g_m}, v_{g_0} \cdots v_{g_1} \cdots v_{g_m})$ , as shown in Figure 9. Here, we painted the digits with a specific color by using a variant of the SN P systems called coloured spikes to easily distinguish the units, tens, hundreds, etc., of the integer part and tenths, hundredths, thousandths, etc., of the fractional part. This strategy was also used to represent the digits of the results of the addition and multiplication operations.

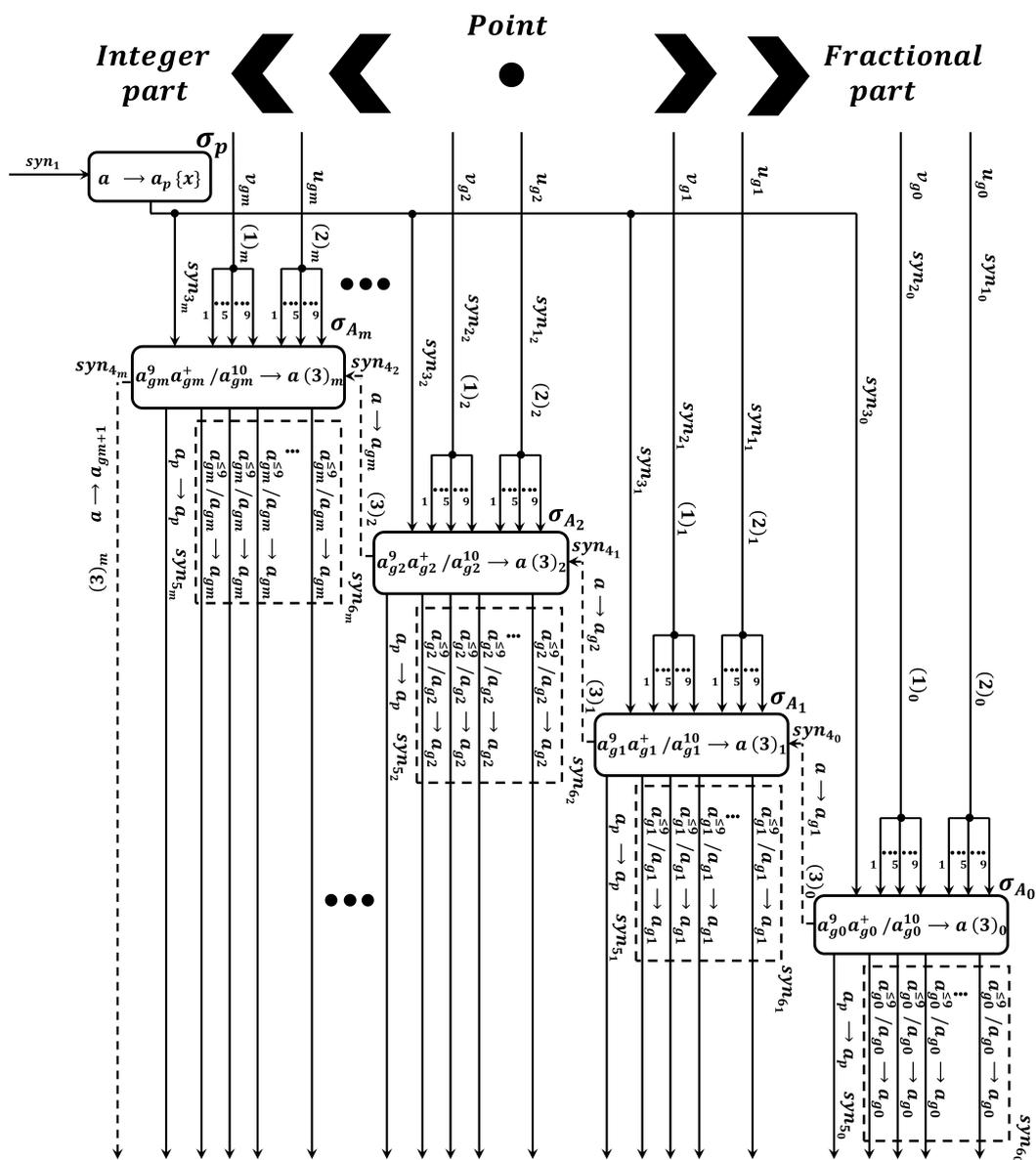


Figure 9. General structure of the proposed floating-point neural adder.

2. Here, each synaptic channel (1) and synaptic channel (2) has a set of dendritic branches. To perform customized floating-point addition, the integer and fractional digits of  $u$  and  $v$  were represented as the number of active dendritic branches, labeled as  $1, \dots, 9$ . In the case of calculating a customized floating-point multiplication, the integer and fractional digits of  $u$  are represented as the number of spikes denoted in the extended rule  $(a_u^p)^+ / a_u^p \rightarrow a_u^p$ . On the other hand, the integer and fractional digits of  $v$  activate the number of branches according to their value.
- *Parallel neural adder circuit  $\Pi_{add}$ .*  
 The proposed neural adder circuit  $\Pi_{add}$  has a set of neurons,  $\sigma_{A_0}, \dots, \sigma_{A_m}, \dots$ , and a neuron,  $\sigma_p$ . The set of neurons  $\sigma_A$  is in charge of computing the addition of two numbers, where each number is composed of an integer part and a fractional part, and neuron,  $\sigma_p$ , determines the position of the point to segment the number into an integer part and a fractional part, as shown in Figure 9.  
 The proposed neural adder circuit  $\Pi_{add}$  computes the addition as follows:  
 In the initial state, the neurons,  $\sigma_A$ , are empty. At this time, the dendritic branches of synaptic channels, (1) and (2), are activated according to the value of the digits,  $u$  and

$v$ , respectively. For example, if the value of a digit,  $v$  or  $u$ , is equal to five, then five dendritic branches are activated. Therefore, these dendritic branches allow the flow of five spikes towards a specific neuron,  $\sigma_A$ . Simultaneously, the neuron,  $\sigma_p$ , places the point to segment the number into integer digits and the fractional digits by setting the firing rule,  $a \rightarrow a_p\{X\}$ . This spiking rule implies that, if neuron  $\sigma_p$  receives a spike at any time, it fires and sends a spike to a specific neuron,  $\sigma_{A_x}$ . To do this, we used a variant of the SN P systems called target indications. In this way, the point was allocated according to the desired precision. Therefore, the point, which was represented as a spike, was stored in a specific neuron,  $\sigma_{A_x}$ . Once the neural circuit was configured, the partial additions of the spikes started.

Here, the addition of the numbers was performed in a single simulation step, since all neurons,  $\sigma_A$ , processed their respective input spikes simultaneously. Additionally, the carry spike was obtained when any neuron,  $\sigma_A$ , accumulated ten spikes. At this moment, the spiking rule,  $a^9a^+ / a^{10} \rightarrow a(3)$ , was set. After one simulation step, the result, represented by the remaining spikes in the soma of each neuron, is placed at the output synapses. In addition, neuron  $\sigma_{A_x}$  sends the spike point to the environment by enabling its spiking rule,  $a_p \rightarrow a_p$ .

In this work, we proved that the use of several variants of the SN P systems, such as coloured-spikes [36], rules on the synapses [37], target indications [51], extended channel rules [38], extended rules [39] and dendritic trunks [52] creates an ultra-compact and high performance circuit, instead of only using the soma as conventional SN P systems do. In particular, the proposed neural circuit required fewer simulation steps, neurons and synapses compared with the existing approach [34], as shown in Table 3.

**Table 3.** Comparison between the existing neural adder [34] and this work in terms of synapses/neurons and simulation steps. Here,  $n$  represents the number of digits of  $v$  and  $u$ . Adapted from [53].

Approach	[34]	This Work
Synapses	41 $n$	14 $n$
Neurons	12 $n$	$n$
Simulation steps	28 + ( $n/2 - 1$ )	1

- *Parallel neural multiplier circuit  $\Pi_{mul}$ .*

Since the multiplier is one of the most demanding in terms of processing and area consumption, a large number of techniques have been developed to minimize these factors. Recently, several authors have used SN P systems to create an efficient parallel multiplier circuit. However, the improvement of processing speed is still an issue since most of the studies improved the area consumption. The improvement of this factor potentially allows the development of high performance systems to support AEC systems in real-time. In addition, the development of a high-precision neural multiplier is still a challenging task, since this factor is especially relevant when metaheuristic algorithms are simulated. Here, we developed a neural multiplier that shows higher processing speeds, in comparison with existing approaches, by keeping the area consumption low. To achieve this, we reduced the processing time by using cutting-edge variants of the SN P systems, such as coloured-spikes [36], rules on the synapses [37], target indications [51], extended rules [39] and dendritic trunks [52]. Specifically, we used these variants to significantly improve the time expended in the computation of the partial products of the multiplication, in comparison with the most recent approach [35].

The proposed neural multiplier circuit  $\Pi_{mul}$  is composed of a set of neurons ( $\sigma_{A_0}, \dots, \sigma_{A_{n-j}}, \dots, \sigma_{A_{n-1}}, \dots, \sigma_{A_{2(n-j)}}, \dots, \sigma_{A_{2n-1}}$ ), and neuron,  $\sigma_{in}$ , as shown in Figure 10. In general terms, neurons,  $\sigma_A$ , perform the addition of the partial products, where

each partial product is computed by using dendritic branches. In particular, each neuron  $\sigma_A$  computes the partial product between a single digit of  $u$  and a digit of  $v$ , where the digits of  $u$  are represented as  $p$  spikes, which are generated by neuron  $\sigma_{in}$  when its spiking rule,  $(a_u^p)^+ / a_u^p \rightarrow a_u^p$ , is applied, and the value of each digit of  $v$  activates an equal number of dendritic branches.

The proposed neural multiplier circuit  $\Pi_{mul}$  performs the multiplication, as follows: At the initial simulation step, neurons,  $\sigma_A$ , are empty. At this time, neuron,  $\sigma_{in}$ , places the spike point by receiving a spike. Therefore, it fires and sends the spike point to a specific neuron,  $\sigma_{A_x}$ , using the target indications [51]. In this way, the digits of  $u$  or  $v$  are segmented into integer and fractional parts. Once the multiplier is configured,  $m \cdot n$  partial products are executed in parallel. To perform any partial product, neuron,  $\sigma_{in}$ , fires  $p$  spikes which are sent to its corresponding neuron,  $\sigma_A$ . The soma of this neuron receives many copies of the spikes,  $p$ , in function of the number of active dendritic branches. For example, if neuron multiplies  $3 \times 3$ , this implies that neuron,  $\sigma_{A_x}$ , receives three copies of three spikes by means of three dendritic branches. In this way, the neuron,  $\sigma_A$ , increases its potential of the soma by performing three additions. Therefore, the synaptic weights are not required since many approaches use them to perform partial products. Hence, the number of branched connections can be variable. In this way, the neuron  $\sigma_A$  enables the optimal number of synaptic connections. From an engineering perspective, we proposed the use of a variable number of forked connections, since the implementation of a very-large number of synaptic connections in advanced FPGAs creates critical routing problems. Once the result is obtained, neuron,  $\sigma_{in}$ , places the spike point according to the addition of the number of fractional digits, as in conventional multiplication. Therefore,  $\sigma_A$ , which received the spike point at the initial simulation, fired the point spike by applying its firing rule ( $a_p \rightarrow a_p$ ). As can be observed from Table 4, we achieved a significant improvement in terms of simulation steps, since only one simulation step was required to perform a multiplication of two numbers with any length. This aspect is relevant, especially when real-time AEC system simulations are required. Additionally, we reduced the number of synapses in comparison with the existing work.

**Table 4.** Comparison between the proposed neural multiplier and the existing neural multiplier [35] in terms of simulation steps, synapses and neurons. Where  $n$  denotes the number of digits of  $v$  and  $u$ . Adapted from [53].

Existing Neural Multiplier	[35]	This Work
Synapses	$9 \cdot n \cdot m$	$n \cdot m$
Neurons	$n$	$n$
Simulation steps	10	1

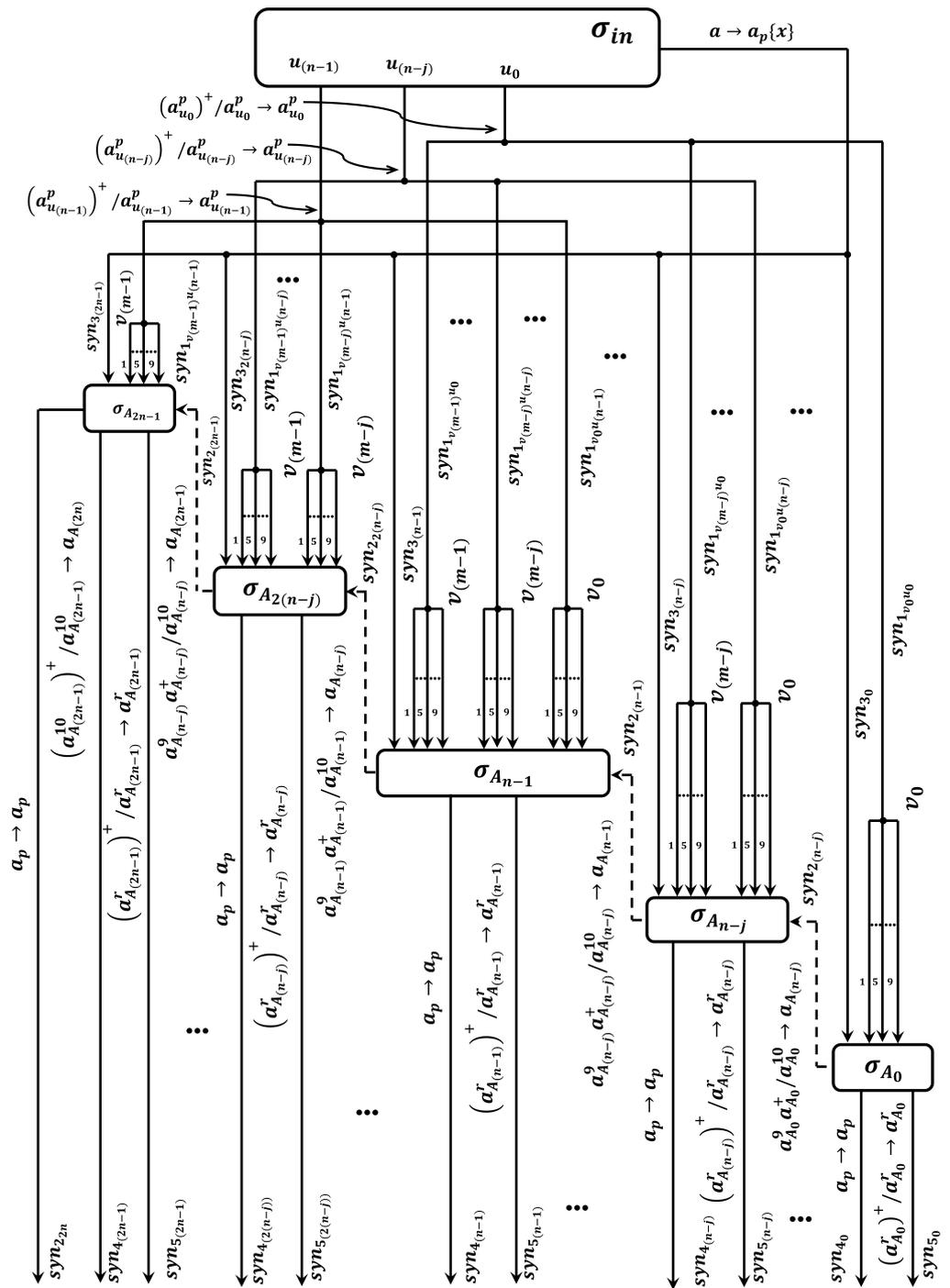
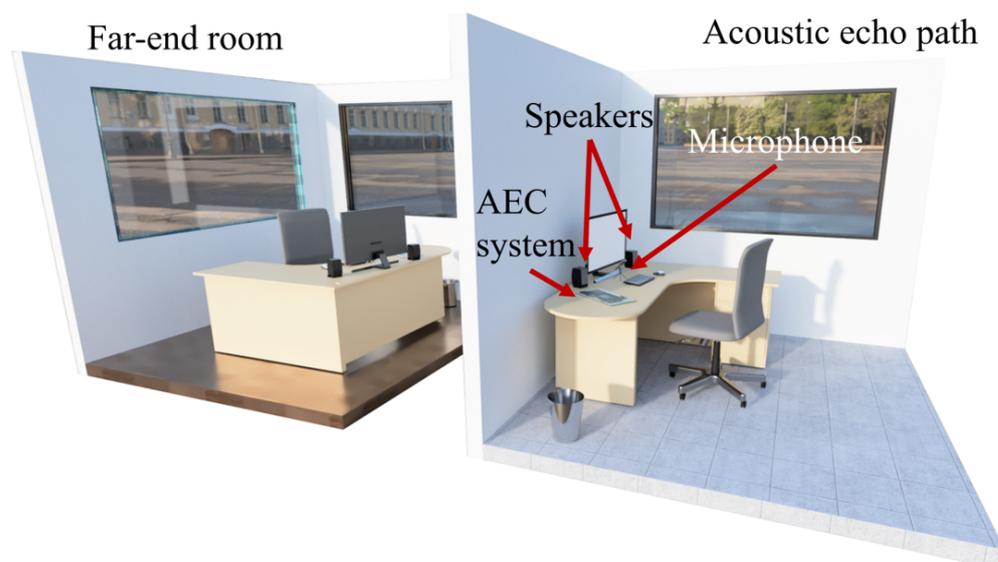


Figure 10. Structure of the neural multiplier.

#### 4.1. Experimental Results

To demonstrate the computational capabilities of the proposed convex GWO/LMS adaptive filter, we considered an arbitrary single-talk scenario, as shown in Figure 11.



**Figure 11.** Scheme of the AEC prototype.

Under this configuration, we used the proposed AEC system to perform the simulation of the proposed algorithm by using the experimental setup of Figure 11. Specifically, the proposed system has an AEC neural processor as its main core to cancel the echo signal and the background noise by simulating the proposed convex GWO/LMS adaptive filter. As can be observed from Figure 12, the AEC neural processor is composed of a control unit, CU, a set of processing cores,  $\alpha$ ,  $\beta$ ,  $\delta$ ,  $\omega$ , LMS, convex, and BRAMs. Figure 13 shows a sequence diagram to specify how each processing core computes specific parts of the proposed convex GWO/LMS adaptive filter. Here, we used the BRAMs to store  $L$  and  $N$  samples of the signals,  $x$ , and  $d$ , where  $L = N$ . In this way, we implemented the block processing scheme. Once these values are stored in their respective BRAMs, the computation of the proposed convex GWO/LMS adaptive filter starts. In this way, the AEC neural processor computes the new variant of the GWO algorithm and the LMS algorithm simultaneously. Specifically, we propose a new time-multiplexing control scheme to automatically update the number of search agents of the GWO algorithm over the processing time. Under this scheme, the number of search agents,  $\omega$ , which are divided into three parts, is enabled or disabled either by the processor,  $\alpha$ , or  $\beta$ , or  $\delta$ . It is important to keep in mind that processing cores,  $\alpha$ ,  $\beta$ ,  $\delta$  evaluate the response of their respective processors,  $\omega$ , simultaneously. According to this, the proposed time-multiplexing control scheme uses the signals,  $en\_w\_alpha$ ,  $en\_w\_beta$ , and  $en\_w\_delta$ , to enable or disable the number of search agents according to the simulation needs, as shown in Figure 12. Here, the use of the time-multiplexing control scheme allowed us to significantly decrease the number of buses to transfer the coefficients between the processing cores,  $\omega$ , and the processing cores,  $\alpha$ , or  $\beta$ , or  $\delta$ . This saving allowed us to implement a full connection between the processing cores,  $\alpha$ ,  $\beta$  and  $\delta$ . As a consequence, the evaluation of the searching point of each agent was performed by processing cores,  $\alpha$ ,  $\beta$  and  $\delta$  simultaneously.

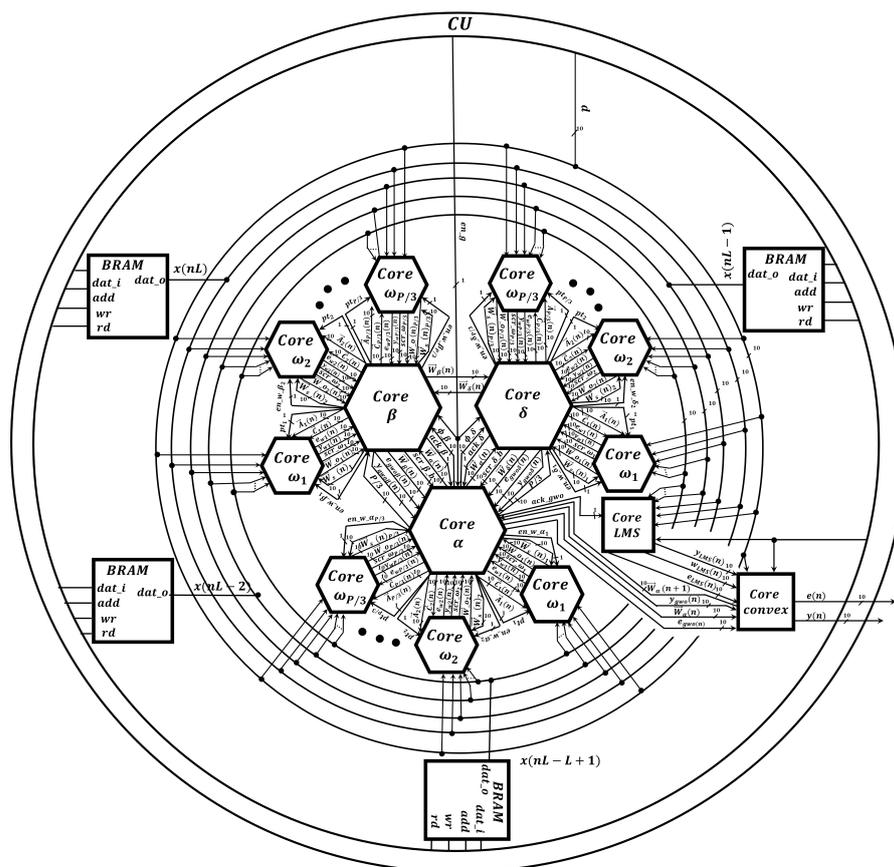


Figure 12. Scheme of the proposed AEC neural processor.

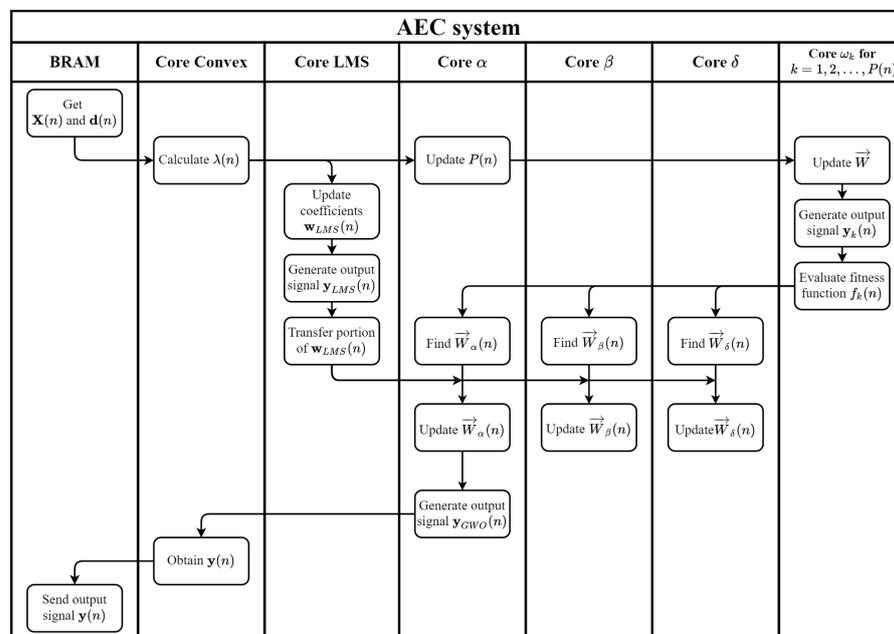


Figure 13. The sequential diagram to describe how the proposed convex GWO/LMS adaptive filter is executed by means of the processing cores.

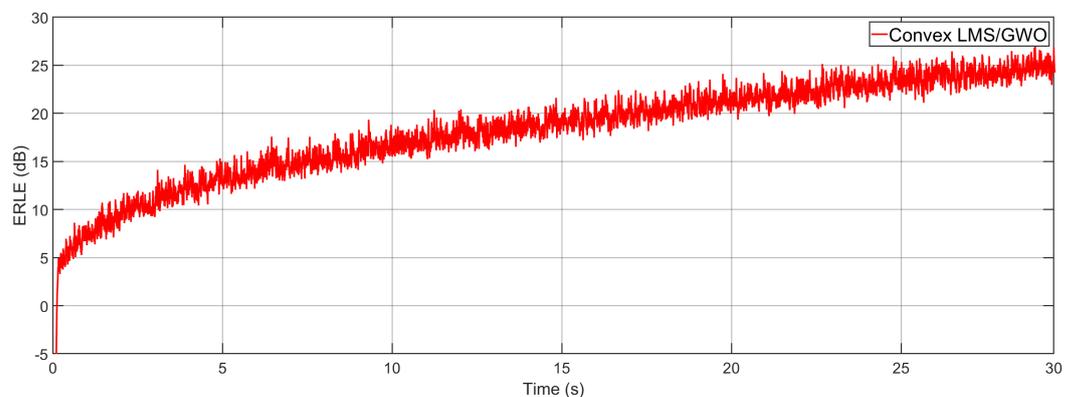
In this work, we used the proposed AEC neural processor to simulate the single-talk and double-talk scenarios by considering the following conditions:

- We employed 1024 adaptive filter coefficients and varied the search agents from 70 to 15.

- The filter and the block had the same length as the echo path.
- As input signals, we used an AR(1) process and speech sequence signals.
- The step-size of the LMS algorithm was set to  $\mu = 0.000001$  and the step-size of the convex algorithm was selected to be  $\mu_a = 15$
- The search agents were initialized using normally distributed random numbers and their positions were bounded between  $[-1, 1]$  over the filtering process.

#### 4.2. Single-Talk Scenario

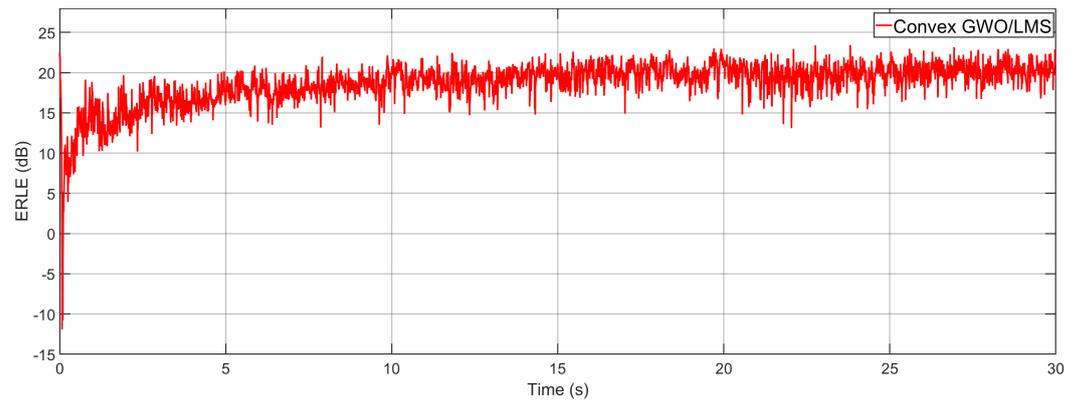
In this section, we demonstrate the computational capabilities of the proposed algorithm under a single-talk scenario. As can be observed from Figures 14 and 15, the proposed AEC neural processor, which simulated the proposed convex GWO/LMS algorithm, reached a good ERLE level by processing two different signals. To carry this out, we configured the AEC neural processor to support one  $\alpha$ , one  $\beta$ , one  $\delta$ , and 70  $\omega$  processing cores. Here, the most demanding core, in terms of area and processing speed, was the  $\omega$  processing core, since each one required 1000 neural multipliers and 1000 neural adders. Therefore, we physically implemented six  $\omega$  processing cores to simulate virtually 70  $\omega$  processing cores. In this way, we saved a large area consumption. In general terms, the implementation of these components required 420,380 LEs, which represented 79% of the total area of an Stratix IV GX EP4SGX530 FPGA. Furthermore, the AEC neural processor required 114.56  $\mu\text{s}$ , which was obtained by multiplying 14,320 clock cycles by the system clock period (8 ns) to simulate the proposed convex GWO/LMS algorithm. This time was calculated when all the search agents were used, i.e., by considering the worse case. However, the number of search agents decreased over the processing time. In the case of employing fifteen search agents, which represented the minimum number, only 1300 clock cycles were expended. Therefore, the processing time reduced from 114.56  $\mu\text{s}$  to 10.4  $\mu\text{s}$ . Therefore, the simulation of real-time AEC systems was guaranteed since the maximum latency was 125  $\mu\text{s}$ .



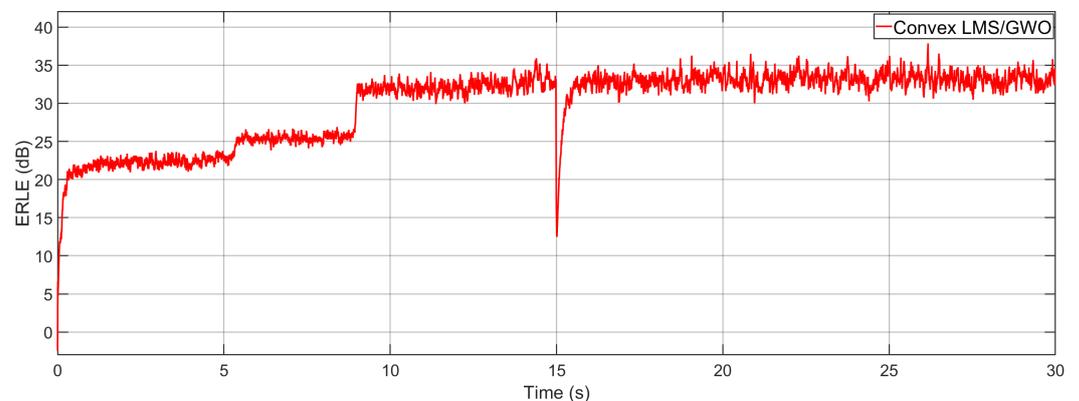
**Figure 14.** ERLE learning curve of the proposed convex GWO/LMS considering an AR(1) process as input signal.

#### 4.3. Double-Talk Scenario

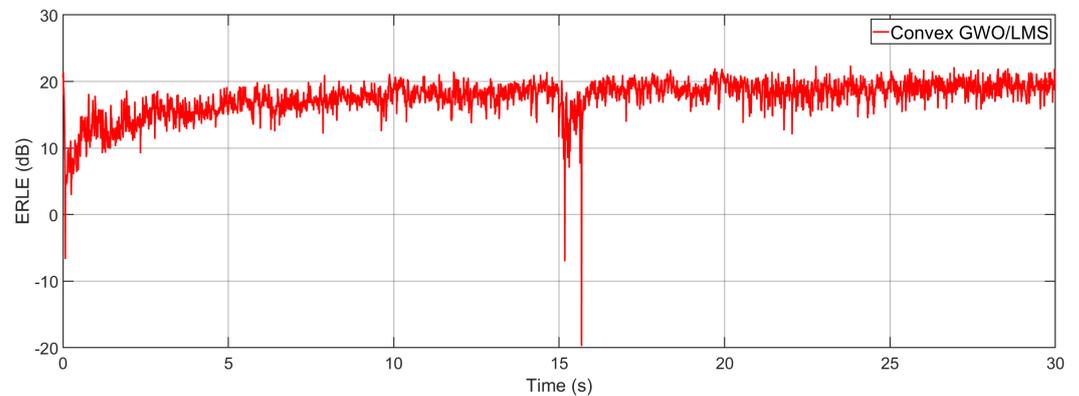
To perform the experiments under this configuration, we employed a double-talk detector circuit to avoid adaptation during periods of simultaneous far and near-end speech. It should be noted that the area consumption in the implementation of this circuit was negligible. Therefore, this implementation expended around 79% of the total area of an Stratix IV GX EP4SGX530 FPGA, as in the previous case. Figures 16 and 17 show the ERLE of the proposed Convex GWO/LMS algorithm by considering an AR(1) process and a speech sequence signal, respectively. As can be observed from the above figures, the proposed algorithm showed good tracking capabilities and achieved a good ERLE level. This aspect is relevant since these levels are required in the development of practical and real-world AEC applications.



**Figure 15.** ERLE learning curve of the proposed convex GWO/LMS considering a speech sequence signal as input signal.



**Figure 16.** ERLE learning curve of the proposed convex GWO/LMS considering an AR(1) process as input signal and a double-talk scenario.



**Figure 17.** ERLE learning curve of the proposed convex GWO/LMS considering a speech sequence signal as input signal considering a double-talk scenario.

## 5. Conclusions

In this work, we present, for the first time, the development of a high-speed and compact FPGA-based AEC neural processor to efficiently simulate a new convex GWO/LMS algorithm. Here, we grouped our contributions as follows:

- *From the AEC model point of view.*

Here, we made intensive efforts to reduce the computational cost of the AEC systems to be implemented in resource-constrained devices. In addition, we significantly increased the convergence properties of these systems by using a cutting-edge meta-heuristic swarm intelligence method, in combination with a gradient descent algorithm to be used in practical acoustic environments. Specifically, we present a new

variant of GWO algorithm along with the LMS algorithm. The use of this combination allowed us to guarantee a higher convergence rate and lower MSE level, in comparison to when gradient descent algorithms or metaheuristic SI methods were used separately. To improve the tracking capabilities of the conventional GWO algorithm, the proposed variant has new exploration capabilities, since the search space is dynamically adjusted. To make the implementation of the proposed variant of the GWO algorithm in embedded devices feasible, we used the block-processing scheme. In this way, the proposed convex GWO/LMS algorithm can be easily implemented in parallel hardware architectures. As a consequence, it can be simulated at high processing speeds. In addition, we significantly reduced the computational cost of the proposed convex GWO/LMS algorithm. To achieve this aim, we propose a method to dynamically decrease the population of a variant of the GWO algorithm over the filtering process.

- *From the SN P systems point of view.*  
Here, we present, for the first time, a compact and high-processing speed floating-point neural adder and multiplier circuit. We used cutting-edge variants of the SN P systems, coloured-spikes, rules on the synapses, target indications, extended channel rules, extended rules and dendritic trunks to create a customized floating-point neural adder and multiplier. Specifically, the proposed neural adder and multiplier exhibits higher processing speed, compared with existing SN P adders and multipliers, since both expend only one simulation step, which is the best improvement achieved until now.
- *From the digital point of view.*  
In this work, we present, for the first time, the development of a parallel hardware architecture to simulate a variable number of search agents by using the proposed time-multiplexing control scheme. In this way, we implemented the proposed GWO method properly, in which the number of search agents increase or decrease according to the simulation needs. In addition, the use of this scheme allowed us to exploit, to the maximum, the flexibility and scalability features of the GWO algorithm.

Finally, we carried out several experiments to prove that the proposed convex GWO/LMS algorithm, along with the new techniques inspired by biological neural processes, potentially allow the creation of practical and real-time AEC processing tools. Part of the future work is to develop new convex combinations, in which other meta-heuristic algorithms can be used in other adaptive filtering applications, such as active noise control, channel equalization and noise cancellers. In addition, new digital techniques will be explored to mimic bio-inspired behavior with high accuracy.

**Author Contributions:** Conceptualization, E.P.; Data curation, L.G. and H.M.P.; Formal analysis, G.S.; Funding acquisition, J.G.A. and J.C.S.; Investigation, A.V. and J.G.A.; Methodology, J.G.A. and G.S.; Resources, E.P., E.A. and A.V.; Software, E.P., E.A. and A.V.; Supervision, G.S. and J.C.S.; Validation, E.P. and E.A.; Writing—original draft, L.G. and H.M.P.; Writing—review & editing, H.M.P. All authors have read and agreed to the published version of the manuscript.

**Funding:** The authors would like to thank the Instituto Politécnico Nacional for the financial support.

**Institutional Review Board Statement:** Not applicable.

**Informed Consent Statement:** Not applicable.

**Data Availability Statement:** No new data were created or analyzed in this study. Data sharing is not applicable to this article.

**Acknowledgments:** The authors would like to thank the Consejo Nacional de Ciencia y Tecnología (CONACYT) and the IPN for the financial support to make this work.

**Conflicts of Interest:** The authors declare no conflict of interest.

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