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Multilayer Micromechanics Process with Thick Functional Layers (EPyC40) †

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Abstract: The EPyC process (Epi-Poly-Cycle) (by Robert Bosch GmbH) opens up unique opportunities for manufacturing complex 3D MEMS structures having high effectiveness in small space. EPyC40 is an EPyC process with up to 40 µm thick polysilicon layers and sacrificial silicon technique. For successful manufacturing a 40 µm EPyC the epitaxial polysilicon layer must be electrically and mechanically optimized. A vertical deep trench patterns the functional and sacrificial areas. A passivation must be deposited homogeneously and has to be tight and robust towards silicon-etching gases. For more than one cycle it is necessary to tailor the layer stress of the epitaxial polysilicon and the wafer-bow. The full process for stacking up 5 EPyC cycles with two 40 µm epitaxial polysilicon layers was investigated in detail. A true 3D MEMS device providing high z deflection by use of a vertical comb drive with 40 µm electrodes was built up successfully to prove the feasibility of the EPyC process.

Keywords: EPyC40; 3D MEMS; comb structure

1. Introduction

The possibilities for manufacturing of 3D MEMS with high freedom of movement, in particular in the z-direction with a small lateral extension of the component, are very limited [1–3]. The EPyC process is an innovative highly flexible MEMS-process and offers a wide range of application opportunities [4]. The special feature of the EPyC process is the use of silicon as a functional and sacrificial layer. This makes it possible to generate high volume sacrificial structures of up to 100 microns thickness. It is based on cyclic deposition of epitaxial poly-silicon and oxide. The silicon is structured to separate sacrificial silicon from functional silicon. The trenches are refilled with oxide and the functional structure is finally released using SF_6 plasma and gaseous XeF_2. The oxide passivation is cleaned off the surfaces with HF vapor phase etching. EPyC40 is an EPyC process with 40 µm thick poly-silicon layers. For successful manufacturing of a 40 µm EPyC the epitaxial poly-silicon layer must be electrically and mechanically optimized. A vertical deep trench with high aspect ratio is needed. The passivation must be deposited homogeneously and has to be tight and robust towards silicon-etching gases. For more than one cycle it is necessary to tailor the wafer bow. In this paper the complete process of a vertical comb structure with 40 µm high electrodes will be studied in all details. To build up the comb structure the EPyC process is cycled 5 times in total.

2. Vertical Comb Drive Realized by EPyC Process

The fabrication sequence of a vertical comb structure using a thick epitaxial polysilicon sacrificial layer is shown in Figure 1. The comb structure consists of 2 × 40 µm high electrodes (top and bottom), a wiring-layer of 1.5 µm, a spring of 1.5 µm and a top plate of 20 µm thickness.

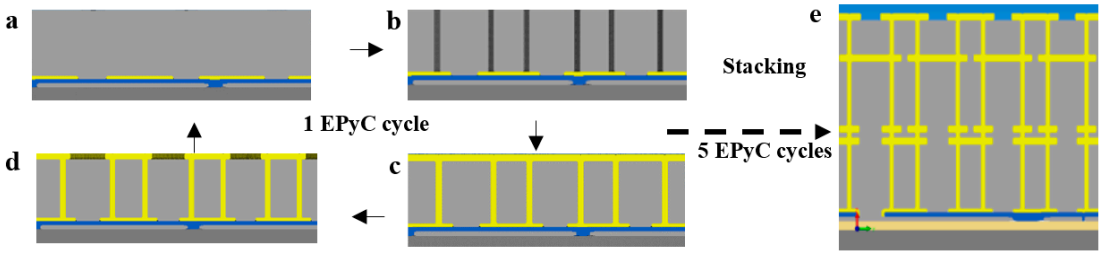

Figure 1. Process simulation of comb structure manufacturing process. (**a**) Epitaxial polysilicon growth (grey: silicon) and structuring (**b**) to separate functional from sacrificial silicon. (**c**) Refill of the deep trenches with homogenous and tight LPCVD TEOS based oxide (yellow: oxide) and (**d**) structuring of the oxide to define the etch access for silicon etching. (**e**) After stacking 5 EPyC cycles.

Starting from a standard 8 inch silicon substrate, a 2.5 µm thermal oxide is grown. The oxide is used as an insulator and a vertical etch stop during sacrificial etching. Onto this oxide a 5 µm thick n-insitu doped epitaxial polysilicon layer 1 (Epi1) is deposited. The Epi1 starts from a thin polysilicon seed layer and is grown in a single wafer cold wall reactor. The silicon layer is planarised chemical-mechanical polishing to a final thickness of 1.5 µm. To improve the conductivity of this layers a doping process with $POCl_3$ is used. A 1.4 µm single gap size mask defines buried interconnectors beneath the movable comb structure. The polysilicon layer is structured with a deep reactive ion etching process (DRIE). In the next step a 2.2 µm thick TEOS based oxide with good step coverage is deposited. This oxide acts as an insulator between the interconnectors and as lateral etch stop during sacrificial etching. The oxide is patterned by a CF_4 oxide RIE process to form contact holes to finish thefirst complete EPyC cycle (1.5 µm). Subsequently the second EPyC cycle follows with a 40 µm Epi. The optimized stack consists of two 20 µm insitu n-doped Epi layers (A) and two separate insitu n-doped LPCVD-silicon layers of 450 nm thickness (B). The layer sequence is B-A-B-A (Figure 2a). Thus top and bottom of each thick 20 µm layer is in direct contact to a thin highly doped poly-layer [5].

The 40 µm stack can thus be deposited with a very high charge carrier concentration of 10^{17}–10^{19} cm^{-3} as shown in Figure 2b. The structuring of 40 µm thick silicon-stack was performed by deep reactive ion etching (DRIE) a 1.4 µm single gap size mask was used. The DRIE-process optimized towards the high aspect ratio of ~1:28 showed only 600 nm one sided etch loss and minimal notching. The 2.5 µm TEOS based oxide as passiviation-2 is deposited with high homogeneity refilling the 40 µm deep trench with a smooth ~1 µm thick TEOS-film on each sidewall of the trench-gap as shown as Figure 2c. The passivation-2 oxide is patterned in one step by a CF_4 oxide RIE process to form etch access and electrical contacts.

The EPyC process is repeated 5 times to build up the comb structure. Therefore wafer-bow management and control very important. The bow must be nearly 0 µm after each EPyC cycle. We successfully built up a stack of 5 EPyCs (2 × 40 µm + 1 × 20 µm+ 2 × 1.5 µm). The wafer-bow was constantly monitored during the wafer-process (Figure 3).

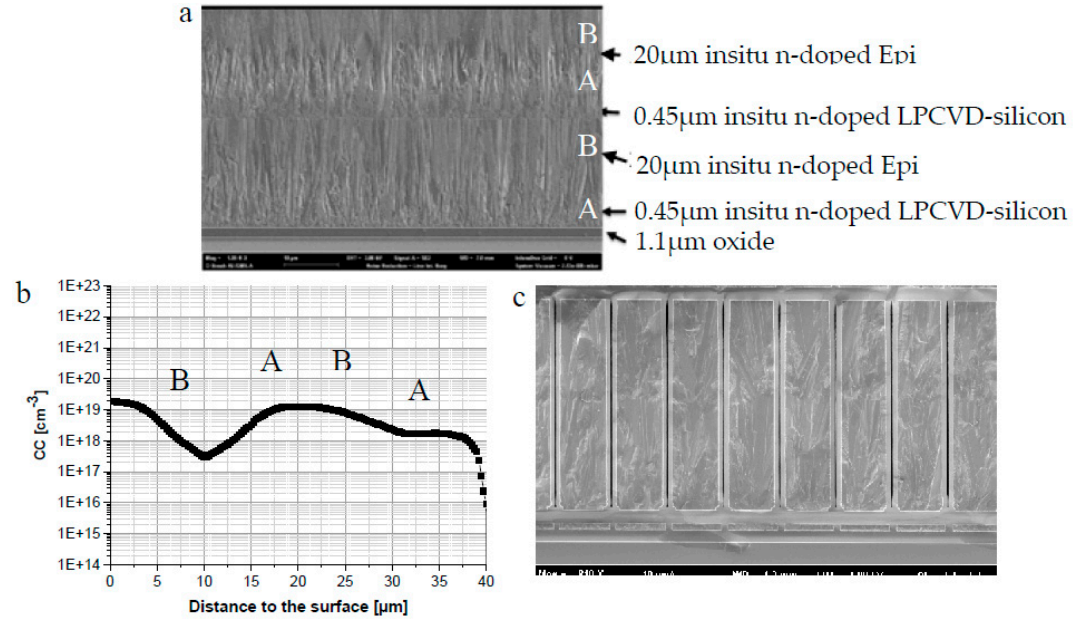

Figure 2. (**a**) SEM image of the 2 × 20 µm Epi with 450 nm n-doped LPCVD-silicon; (**b**) Spreading Resistance Profiling for the silicon-stack. (**c**) SEM picture of 40 µm refill trenches with 2.5 µm LPCVD TEOS (1 µm sidewall passivation).

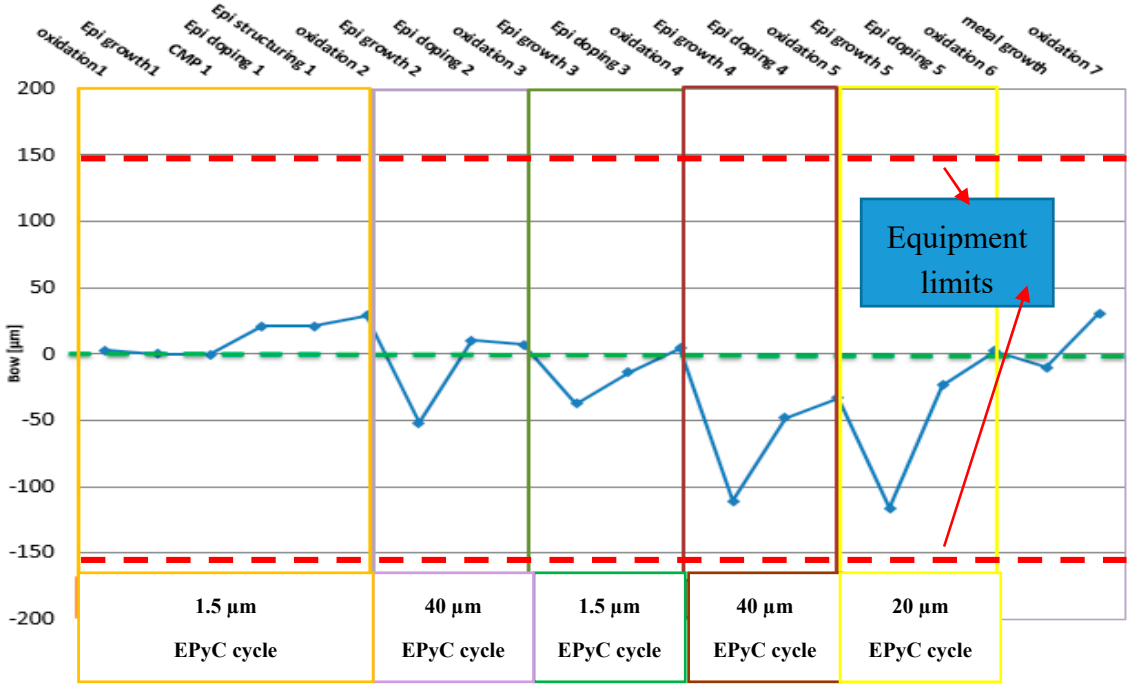

Figure 3. The propagation of the wafer-bow during the wafer-process of the comb structure. Each single EPyC and the full process with 5 EPyC cycles was managed to run nearly bow-neutral.

Figure 4a shows a SEM picture of the cross section of the successfully manufactured comb structure. The total thickness of the 5 stacked EPyC-layers (2 × 40 µm electrodes + 1 × 20 µm top plate + 2 × 1.5 µm spring and wiring) is 103 µm. In the end of the process a complex 3D sacrificial silicon structure was generated. High volumes combined with tiny buried channels had to be fully released. Therefore we used an optimized dry etching process using SF_6 plasma and XeF_2 gas [6] providing a very moderate etch time of only 15 min. Gaseous HF was used to clean the surface SiO_2 layer off the final comb structure. Figure 4b shows a SEM picture of the vertical comb electrodes after successful sacrificial silicon and oxide release.

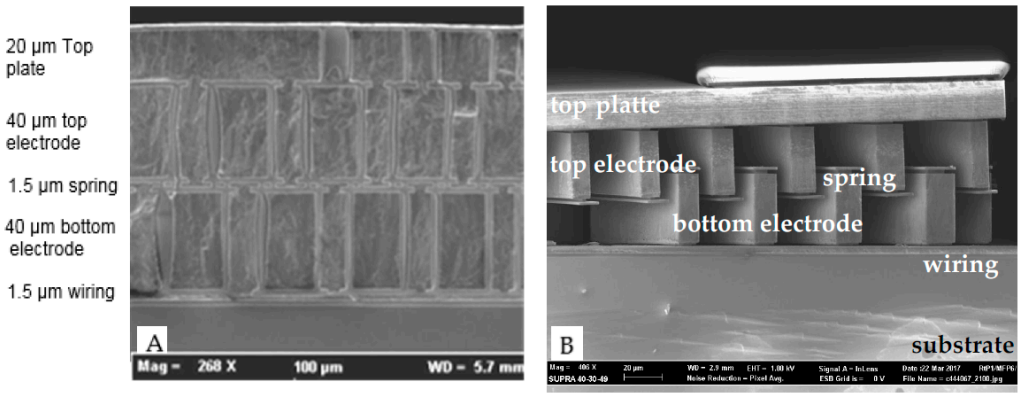

Figure 4. SEM of the 5 EPyC process; (**A**) after 5 EPyC deposition; (**B**) after successful Si-etching with SF_6/XeF_2 and oxide etching with HF-Vapour.

3. Conclusions

We successfully built up a vertical comb drive for large z deflection in 3D MEMS devices. We used the new EPyC40 process which combines thick epitaxial polysilicon layers with sacrificial silicon technology. The best mechanical and electrical properties of the 40 µm electrode layer were obtained by a combination of two 20 µm insitu n-doped epitaxial polysilicon layers with 450 nm insitu n-doped LPCVD-silicon interlayers. The charge carrier concentration in the silicon stack was as high as 10^{17}–10^{19} cm^{-3} determined by Spreading Resistance measurements. The DRIE process to pattern the thick layer was optimized towards the high aspect ratio showing only 600 nm one sided etch loss and minimal notching. A perfect refill of the 40 µm trenches was achieved by deposition of 2.5 µm LPCVD TEOS showing a smooth 1 µm TEOS film on both side-walls of the 40 µm deep trench. The feasibility to cycle the EPyC process was successfully demonstrated by stacking up 5 EPyC layers (2 × 40 µm + 1 × 20 µm+ 2 × 5 µm) on top of each other without process issues due to wafer bow. The final comb drive was released by an optimized dry etch process with SF_6 plasma and XeF_2 in only 15 min.

Conflicts of Interest: The authors declare no conflict of interest.

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