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Hardware-Aware Deep Learning

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Deadline for manuscript submissions:
closed (20 May 2023)

Message from the Guest Editors

One of the main factors that contributes to the success of deep learning (DL) is the mighty computing power provided by modern hardware, spanning from high-performance server systems to resource-limited edge devices. The edge side (e.g., embedded systems, IoT) demands not only extreme energy-efficiency but also real-time inference capability, which requires cross-stack techniques, including model compression, compilation, architecture and circuit design of AI chips, emerging devices, etc. On the cloud side, as the DL model size grows exponentially in the last two years (e.g., OpenAI GPT3, Google switch-transformer, etc.), how to efficiently support the training and inference of those immerse models is also an emerging research direction. Without lowering their hardware cost, however, incorporating them into the paradigm of machine learning as a service (MLaaS) will be infeasible. Therefore, the aforementioned concerns motivate the research of hardware-aware deep learning, for optimized energy, latency, and even security.

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Message from the Editor-in-Chief

As the world of science becomes ever more specialized, researchers may lose themselves in the deep forest of the ever increasing number of subfields being created. This open access journal *Applied Sciences* has been started to link these subfields, so researchers can cut through the forest and see the surrounding, or quite distant fields and subfields to help develop his/her own research even further with the aid of this multi-dimensional network.

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