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Nanoscale CMOS Devices and Their Applications

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Deadline for manuscript submissions:
closed (20 August 2023)

Message from the Guest Editor

Dear Colleagues,

The scaling of CMOS technology has been a primary driving force of the semiconductor industry, enabling more compact and faster integrated circuits. The technology has evolved from planar MOSFET to Tri-gate FinFET and then gate-all-around (GAA) structures with improved electrostatics. Design technology co-optimization enables further improvements in performance, power efficiency, and area density. There is no doubt that silicon CMOS technology still has strong vitality in the foreseeable future. However, it has become increasingly difficult to shrink transistors along the path of Moore's Law due to power, interconnection, and fabrication challenges. Innovations from low-dimensional materials, new device structures, monolithic 3D integration, cryogenic electronics, and alternative switching principles provide additional possibilities to sustain the scaling and improve energy efficiency. This Special Issue invites researchers and scientists to submit research papers, short communications, and review articles focusing on cutting-edge research and recent advances in nanoscale CMOS devices from fundamental research to applications.

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Message from the Editor-in-Chief

As the world of science becomes ever more specialized, researchers may lose themselves in the deep forest of the ever increasing number of subfields being created. This open access journal Applied Sciences has been started to link these subfields, so researchers can cut through the forest and see the surrounding, or quite distant fields and subfields to help develop his/her own research even further with the aid of this multi-dimensional network.

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