



FPGA-Based Deep Neural Network Accelerators Using Emerging Technologies

Guest Editor:

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Message from the Guest Editor

In this Special Issue, original research articles and reviews are welcome. Research areas may include (but not limited to) the following:

- Novel architecture for FPGA-based DNN accelerators;
- Hardware/software co-design for FPGA-based DNN accelerators;
- Resource/bandwidth optimizations for FPGA-based DNN accelerators;
- FPGA-based DNN accelerators using fast convolution algorithms;
- FPGA-based accelerators for sparse DNNs;
- FPGA-based DNN accelerators performing low-bit/mixed-bit quantization;
- FPGA-based DNN accelerators using approximate computing;
- Dynamically reconfigurable DNN accelerators;
- FPGA-based graph convolution neural network acceleration;
- FPGA-based spike neural network acceleration;
- FPGA-based transformer network acceleration;
- FPGA-based acceleration of other atypical convolutions/networks;
- Emerging applications of FPGA-based DNN accelerators.





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Message from the Editor-in-Chief

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