



High-Speed I/O Circuits and Architectures

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Deadline for manuscript
submissions:

closed (15 January 2022)

Message from the Guest Editors

A microprocessor with memory constituting a tiny computing system is now required to handle several hundreds of gigabits per second, and this is growing at a relentless rate. Similar trends are also occurring in longer-distance applications such as inter-server and long-haul communications. However, at the same time, the channel loss of electrical wires is becoming very significant as the required data rate increases, and I/O interfaces are facing many challenges. It will be tougher as the scaling ends because we will no longer be able to take advantage of faster transistors. The aim of this Special issue is to present circuit and architecture level techniques and to guide technology directions for the years to come. The topics to be covered in this Special Issue include but are not limited to the following:

- Design techniques for high-speed I/O transmitters, receivers, and transceivers;
- Building blocks for NRZ/PAM-N/DSP-based I/O transceivers;
- Low-power I/O circuit techniques;
- Memory interfaces;
- Clock generation/distribution/recovery circuits;
- Circuits and architectures for optical interconnect for computer communications





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Message from the Editor-in-Chief

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