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Software/Hardware Codesign for Embedded Multicore Systems

Guest Editor:

Dr. Michael Engel

Department of Computer Science, Faculty of Information Technology and Electrical Engineering, Norwegian University of Science and Technology, Høgskoleringen 1, 7491 Trondheim, Norway

Deadline for manuscript submissions:

closed (31 December 2020)

Message from the Guest Editor

This Special Issue calls for innovative work to design, analyze, optimize the use, and solve the challenges of using multicore systems using software/hardware codesign approaches.

Topics of interest include, but are not restricted to the following:

- HW/SW partitioning, interfaces and synthesis
- Handling heterogeneity in codesigned multicores
- Memory hierarchies, scratchpad, and caches in multicore systems
- Communication and synchronization for multicore systems
- Modeling, analysis, and multi-criteria optimizations of non-functional properties
- Security, dependability, and fault tolerance of SW/HW-codesigned multicores
- Automatic parallelization and compilation approaches for multicores
- SW/HW codesign for in- and near-memory computing
- Hypervisor and operating systems for multicores
- Architecture–compiler–operating system codesign
- Runtime adaptive and reconfigurable systems
- WCET/WCEC analysis for multicore systems
- Networks-on-Chip (NoCs) for codesigned multicore systems

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Design space exploration, virtual platforms, and cosimulation









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Editor-in-Chief

Prof. Dr. Flavio Canavero

Department of Electronics and Telecommunications, Politecnico di Torino, 10129 Torino, Italy

Message from the Editor-in-Chief

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