Hardware Accelerated Algorithms and Architectures for Various DSP Applications

Guest Editor:

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Deadline for manuscript submissions:
closed (30 June 2023)

Message from the Guest Editor

The main purpose of this Special Issue is to attract submissions on the development of high-performance signal processing algorithms and optimized hardware architectures required for various signal processing applications. Optimization at all levels of abstraction falls within the field of interest of this Special Issue, e.g., at the algorithm, register-transfer, and circuit levels.

The topics of interest include, but are not limited to:

• Models, methods, and architectures for accelerated computing
• Hardware architecture for digital signal processing algorithm
• Hardware design in edge/IoT computing
• Low power and high-performance design
• Hardware/software co-design
• High level synthesis
• Reconfigurable system design
• Interaction of CPU and FPGA components
• System on chip design
• High-speed algorithm and architecture
• Optimized design of digital communication systems
• Digital system design with reduced memory bandwidth

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Special Issue

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Message from the Editor-in-Chief

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