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RISC-V Architectures and Systems: Hardware and Software Perspectives

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Deadline for manuscript submissions:
closed (1 October 2022)

Message from the Guest Editors

This Special Issue aims to shed some light on some of the aforementioned topics, tackled by RISC-V-based initiatives and projects, by sharing the most recent and promising results with the research community.

Authors are invited to submit regular papers following the *JLPEA* submission guidelines, within the remit of this Special Issue call. Topics include but are not limited to:

- RISC-V processors, micro-architecture optimizations, and hardware accelerators;
- Edge computing and ISA extension (e.g., packed-SIMD, floating point, bit-manipulation);
- System integration, atomic memory operations, OS support (e.g., hypervisor), compiler and runtimes, containerization, and virtualization;
- Simulation and emulation, performance analysis tools, and methodologies,
- Quality assurance and reliability, design verification/validation, and security (secure architectures and cryptography).

Special Issue

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Message from the Editor-in-Chief

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Our aim is to encourage scientists to publish their experimental and theoretical results in as much detail as possible. There is no restriction on the length of the papers. Full experimental and/or methodical details must be provided.

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