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# **Statistical Integrated Circuit Design**

Guest Editor:

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Deadline for manuscript submissions: closed (15 December 2020)

# Message from the Guest Editor

Recent advances in electron device fabrication technology to obtain tiny, fast, and low-power integrated circuits (ICs) have caused continuous reduction in the feature size of the devices.

Therefore, at the nanometer geometries used in current technologies, investigating the statistical behavior of integrated devices becomes of paramount importance in IC design.

The aim of this Special Issue is to publish original research articles that cover recent advances in the theory and application of statistical design of ICs.

Potential topics include, but are not limited to, the following:

- Atomistic level device modeling;
- Device mismatch modeling;
- IC design strategies at schematic and layout level;
- The mathematical approach to stochastic process variations;
- Mathematical modeling and numerical methods for statistical simulation;
- The Montecarlo, quasi-Montecarlo, and non-Montecarlo techniques;
- Parametric yield estimation and minimization;
- Statistical timing analysis;
- Statistical simulation tools.





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### Message from the Editor-in-Chief

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