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Advanced Interconnect and Packaging

Guest Editor:

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Deadline for manuscript submissions:
closed (20 October 2022)

Message from the Guest Editor

Dear Colleagues,

Unlike transistors, the continuous downscaling of feature size in CMOS technology leads to a dramatic rise in interconnect resistivity and concomitant performance degradation. At nanoscale technology nodes, interconnect delay and reliability become the major bottleneck faced by modern integrated circuits. To resolve these interconnect problems, various emerging technologies including airgap, nanocarbon, optical, and through-silicon via (TSV) have been proposed and investigated. For example, by virtue of TSV technology, dies can be stacked to increase the integration density. More importantly, 3D integration and packaging also offer the most promising platform to implement “More-than-Moore” technologies, providing heterogenous materials and technologies on a single chip.

This Special Issue seeks to showcase research papers, communications, and review articles on new developments in advanced interconnect and packaging, i.e., on the design, modeling, fabrication, and reliability assessment of emerging interconnect and packaging technologies.

We look forward to receiving your submissions!

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Special Issue

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Message from the Editor-in-Chief

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